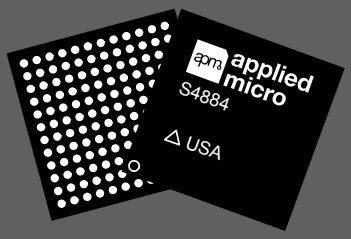
S4884

Serial 10M-2.7Gbps Multi-Rate

PRODUCT BRIEF



he S4884 transceiver device is a fully integrated CMOS transceiver utilizing a single fixed rate reference clock for multi-rate coverage of the 10 Mbps through 2.7 Gbps band. I2C/SPI accessible independent RX/TX data path rate control, with 10 Hz resolution, also allows for asymmetrical continuous rate operation. On-chip clock synthesis and clock recovery PLL components are contained in the S4884. The chip consists of a receive (RX) function that includes a clock and data recovery (CDR) unit and a DeMUX. The transmit (TX) function contains a MUX and clock synthesis unit (CSU) elements. The figure below shows a typical network application.

Features

- 12.5 mV Diff Input Sensitivity at $1x10^{-12}$ BER
- Receive and transmit operation with a single reference clock for 13 different data rates ranging from 10 Mbps to 2.7 Gbps.
- Frame / Boundary Detection and Byte Alignment for SONET/SDH and 8B/10B encoded protocols and Differential RX/TX Decoding/ Encoding
- Output Data De-Emphasis with Adjustable Swing and Phase Continuous Output Clocking
- Programmable Parallel Data Path (4/8/10-bit or 4-bit Redundant Data Mode) with Optional Parity & Programmable Auto Squelch Functionality
- Post Amp Offset Adjust, Loss of Signal with Run Length Detector, Signal Detect Input, Receive Signal Strength Indicator and RX/TX Lock Detect circuits
- Integrated PLL Loop Filter Components & I/O Terminations for a Compact Applications
- Dual REFCLK Inputs for Flexible CDR/CSU Reference Clocking and/or External Clean-Up
- Additional CDR & CSU Programmable Prescaler Clock Outputs for Down/Upstream Timing
- I2C & SPI Compatible Control Interfaces with Global Alarm Interrupt, Status, & Control
- Intelligent Power Down of Selected Features/ Functions for Power Restricted Applications
- 1.2 V & 3.3 V Power Supply Requirements
- Complies with Bellcore/ITU-T Specs for Jitter Tolerance/Transfer/Generation as well as the Related GE/FC/CPRI Specifications.
- JTAG (IEEE 1149.1-2001 compliant) & Dual Independent Pattern Generators/Checkers
- Less than 900 mW Typical Power Dissipation
- Standard and Green/RoHS Compliant Lead Free Package Options

Overview

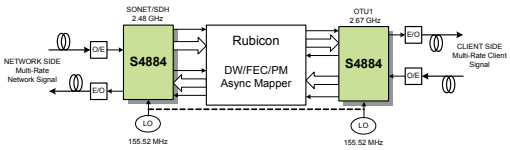
The S4884 transceiver implements multi-rate serialization/deserialization for a variety of protocols and transmission standards. This chip can be used to implement the front end of a variety of Clock/Data Recovery (CDR) and clock synthesis Serializer/Deserializer (SerDes) applications. The S4884 consists primarily of the serial receive interface and the serial transmit interface. The chip handles all of the functions of these two elements including offset adjustment, serial-to-parallel and parallel-to-serial conversion, clock generation, frame / boundary detection & word alignment (only for SONET/SDH and 10-bit 8B/10B based protocols), and system timing via an internal Clock Synthesizer Unit (CSU).

Many optional features provide the ultimate in flexibility for the S4884 device operation. The parallel interface ports have programmable bus width capability (4/8/10 bits wide with the option of running in a 4-bit Redundant Data Mode). Parity and bit/ polarity swap are also options on these interfaces. The device also expands its alarm and control flexibility when used with either of the supplied I2C or the SPI communication interfaces. Through these communication ports the user will have access to maskable interrupt alarms (that are summed into a pin accessible summary interrupt), as well as status registers, configuration and control bits. Both communication ports may also be used simultaneously for dedicated closed loop control via the faster SPI port while utilizing the I2C bus for initialization, configuration, and monitoring. The communication ports also expand the fixed rate use of the device so that any fixed rate (within 10 Hz) may be programmed into the device.

Supported Data Rates

- 10 Mbps: 10Base-X Ethernet
- 125 Mbps: 100Base-X Ethernet/Fast Ethernet
- 155.52 Mbps: STM-1/OC-3
- 200 Mbps: ESCON/SBCON
- 265.625 Mbps: 1/4 Fibre Channel
- 531.25 Mbps: 1/2 Fibre Channel
- 622.08 Mbps: STM-4/OC-12
- 1.0625 Gbps: Fibre Channel
- 1.25 Gbps: 1000Base-X Ethernet/ GigEthernet
- 1.485 Gbps: SMPTE 292M
- 2.125 Gbps: 2x Fibre Channel
- 2.488 Gbps: STM-16/OC-48
- 2.666 Gbps: OTU-1

S4884 System Block Diagram



For technical support inquiries, submit your product related questions to support@appliedmicro.com.

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