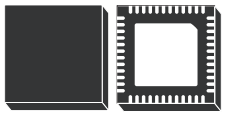
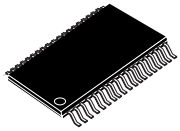
SCLT3-8BQ7, SCLT3-8BT8

Datasheet

Octal industrial digital input current limiter with serialized output



QFN-48L 7.0 x 7.0 x 0.9 mm



HTSSOP-38 package

Product label

Product status link

SCLT3-8BQ7, SCLT3-8BT8

Features

- Eight current-sinking digital inputs with serializer
- Enables inputs to meet type 1, 2 and 3 characteristic of IEC 61131-2 standard
- Adjustable and accurate input current limitation for low power and heat dissipation:
  - 2.35 mA typ for Type 1 and Type 3
- Integrated glitch and debounce filter with selectable delay time: 20 µs to 3 ms for EMC robustness
- 35 V reverse polarity capable
- SPI-Compatible Serial Interface 8-bit
  - Optional 16-bit mode with parity check, and diagnostics (temperature alarm, voltage alarms)
- Daisy-Chain SPI to reduce isolation channels
- 5 V voltage regulator
- Energyless Field-Side LED drivers for visual status indication
- Operating ambient temperature range from -40 °C to 105 °C
- Packages
  - HTSSOP-38 – 500 µm pitch
  - QFN-48L – 500 µm pitch
- **Complies with the following standards**:
  - IEC 61000-4-2 level 4: ±15 kV (air discharge)
  - IEC 61000-4-2 level 4: ±8 kV (contact discharge)
  - IEC 61000-4-5 Surge ±1 kV /42 Ω with minimum 1 kΩ pulse resistor at field inputs

Applications

Where current limitation is required in factory automation applications:

- Programmable logic controller
- Input modules
- CNC control
- Motor control

Description

The SCLT3 series is an octal industrial digital input IC which drastically reduces the power dissipation of the digital input modules. Its current-sinking inputs can be configured for Type 1, Type 2, or Type 3 inputs as per IEC 61131-2 with few external components.

The SCLT3 series includes a serial interface which translates, conditions and serializes the data to CMOS-compatible signals through SPI. Combining its daisy-chaining capability with its accurate current limitation, the SCLT3 series enhances the I/O module's density by cutting the power dissipation and reducing the number of optocouplers.

The SCLT3 series can be evaluated thanks to the STEVAL-IFP030V1 evaluation board. For detailed application guidelines refer to AN2846.

1 Circuit block diagram

Figure 1. Circuit block diagram

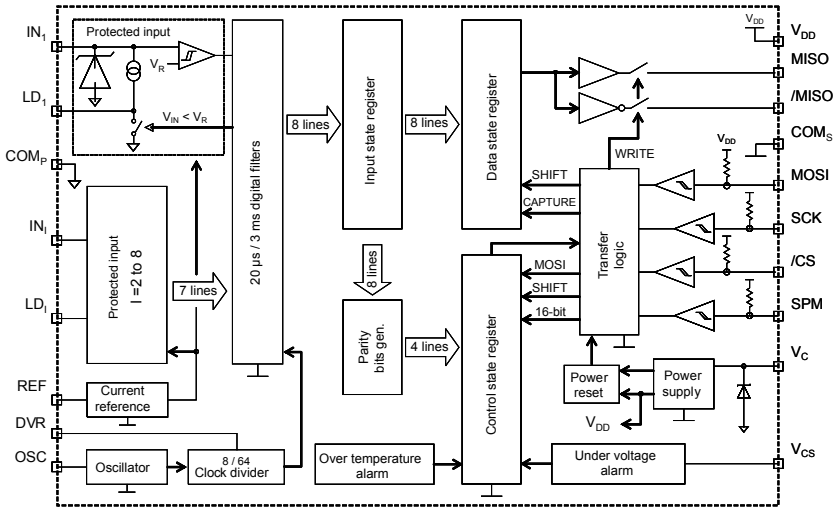
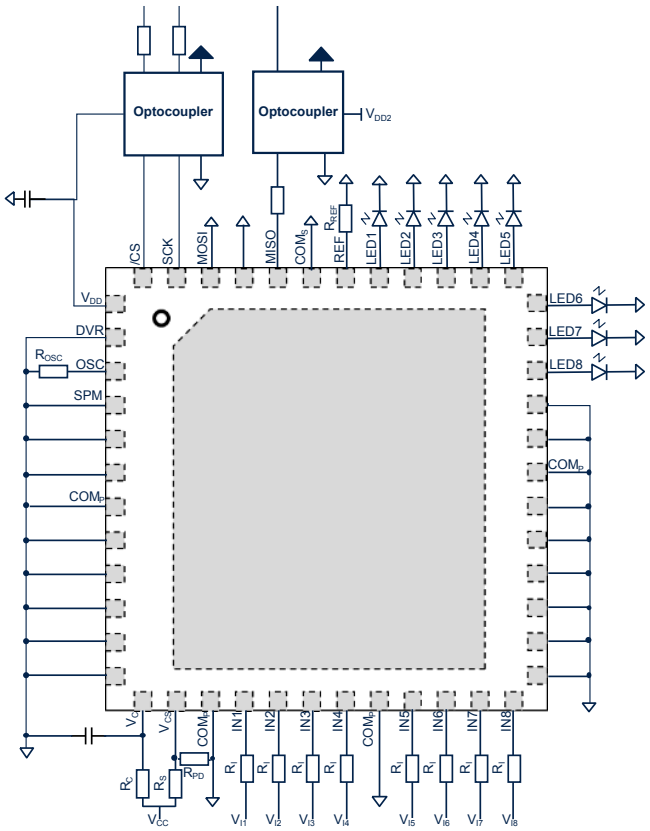


Figure 2. Typical application schematic



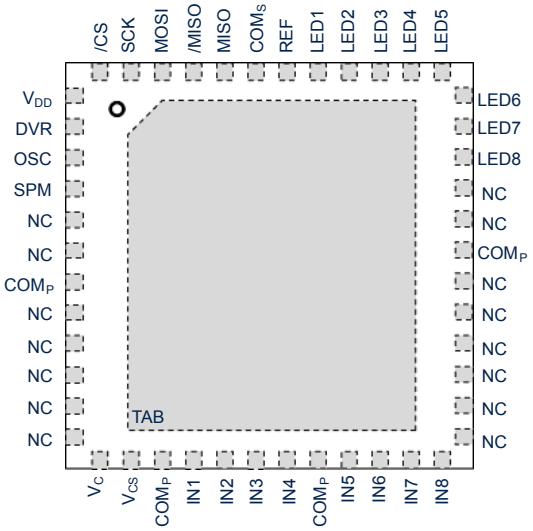
Note: In case of a LED not being used, the LED output pin must be connected to the ground COM_P to allow the input current to flow back to the ground.

1.1 I/O pin description

Table 1. **I/O pin description**

Symbol	Parameter		Pin # SCLT3-8BQ7	Pin # SCLT3-8BT8
IN_I	Power input	Logic input with current limitation, I = 1 to 8	16, 17, 18, 19, 21, 22, 23, 24	8 to 11, 13 to 16
LD_I	Power output	LED output driver with current regulation, I = 1 to 8	41, 40, 39, 38, 37, 36, 35, 34	27 to 20
V_C	Power input	24 V sensor power supply	13	5
V_{CS}	Signal input	24 V sensor power supply sensing input	14	6
COM_P	Ground	Power ground of power sensor supply	7, 15, 20, 31	4, 7, 12, 17
V_{DD}	Power output	5 V logic power supply	1	38
COM_S	Ground	Signal ground of logic / output section	43	30
REF	Signal input	Input current limiter reference setting	42	29
SPM	Signal input	SPI shift register length selector: • SPM to GND = 16 bits • SPM to V_{DD} = 8 bits	4	3
/CS	Logic input	SPI chip select signal	48	35
SCK	Logic input	SPI serial clock signal	47	34
MOSI	Logic input	SPI serial data input signal	46	33
DVR	Logic input	Divider ratio selector of the digital input filters (8 or 64 steps)	2	1
OSC	Signal input	Delay setting of the digital input filters	3	2
MISO	Logic output	SPI serial data output signal	44	31
/MISO	Logic output	Inverting SPI serial data output signal	45	32
TAB	Substrate	Exposed pad to be connected to COM_P	TAB	Expose pad
NC		Not connected (or to be connected to COM_P)	5, 6, 8, 9, 10, 11, 12, 25, 26, 27, 28, 29, 30, 32, 33	18, 19, 28, 36, 37

Figure 3. Pinout description of the QFN-48L 7x7 and HTSSOP-38 versions (top view)



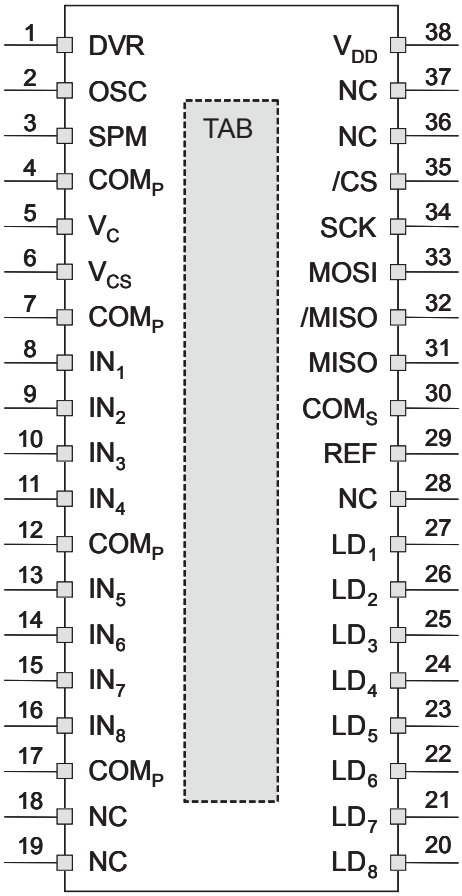


Figure 4. Switching characteristics for IEC61131-2 Type 1, 2, and 3 digital inputs (24 V DC)

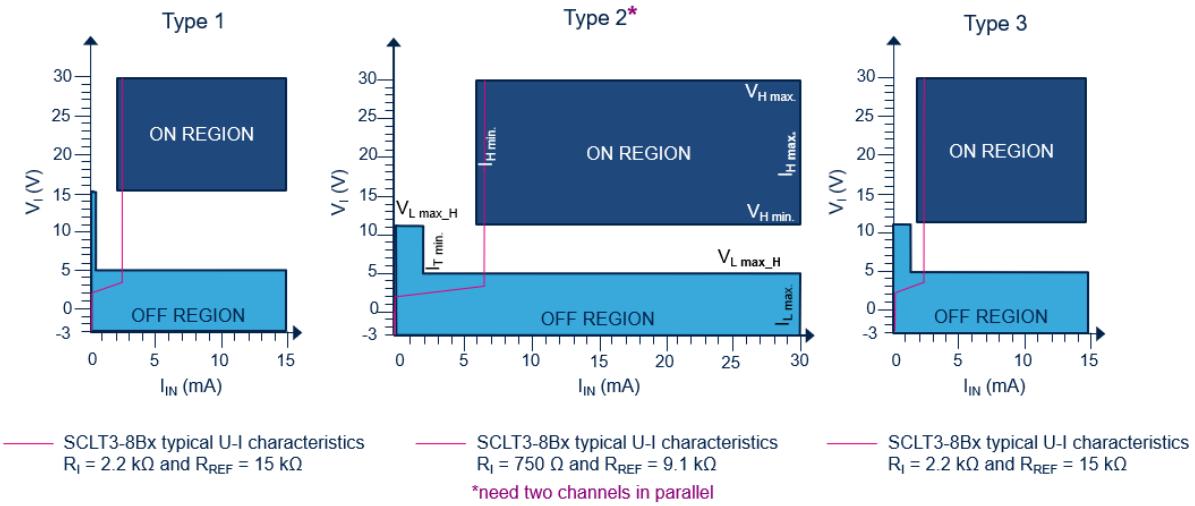


Table 2. IEC61131-2 Input characteristic limits

Symbol[1]	Type 1	Type 2	Type 3
$U_{L\ max\_H}$	15 V	11 V	11 V
$U_{L\ max\_L}$	5 V	5 V	5 V
$I_{L\ max.}$	15 mA	30 mA	15 mA
$I_{T\ min.}$	0.5 mA	2 mA	1.5 mA
$U_{H\ min.}$	15 V	11 V	11 V
$U_{H\ max.}$	30 V	30 V	30 V
$I_{H\ min.}$	2 mA	6 mA	2 mA
$I_{H\ max.}$	15 mA	30 mA	15 mA

1. *Symbol names are reported only on type 2 diagram for the sake of clarity.*

2 Characteristics

Table 3. Absolute maximum ratings

Symbol	Pin	Parameter name	Conditions	Value	Unit
V_{CC}	V_C	Bus power supply DC voltage	500 Ω < R_C < 2.2 kΩ	-35(1) to 35 (2)	V
V_C	V_C	Power supply voltage	R_C = 0 kΩ	-0.3 to 30	V
I_{CC}	V_C	Maximum bus power supply current		15	mA
V_{CS}	V_{CS}	Sensing bus power supply voltage		-0.3 to 6	V
I_{DD}	V_{DD}	Maximum output power supply current	R_C = 500 Ω	12	mA
V_I	IN_I	Input steady state voltage, I = 1 to 8	R_I = 2.2 kΩ	-35 to 35	V
I_{IN}	IN_I	Input forward current range		-20 to 10	mA
I_{OSC}	OSC	Maximum sourced oscillator current		120	µA
LV_I	SCK, /CS, MOSI	Logic input voltage		-0.3 to 6	V
T_{stg}		Storage temperature range		-40 to 150	°C
T_{amb}		Ambient temperature range		-40 to 105	°C

1. *A reverse polarization diode must be placed on V_{CC} in order to avoid leakage when -35 V is applied.*
2. *70 mm² of 35 µm thick copper is required for single layer FR4 PCB to have a low enough R_{th} and therefore keep SCLT3-8Bx device below its T_j(max).*

Table 4. Electromagnetic compatibility ratings

Symbol	Pin	Parameter name	Value	Unit
V_{PPB}	IN_I	Peak pulse voltage burst, IEC 61000-4-4(2)	4	kV
V_{PP}	IN_I	Peak pulse voltage surge, IEC 61000-4-5 (42 Ω), R_{IN} = 1 kΩ min(3)	1	kV
V_{PP}	V_C	Peak pulse voltage surge, IEC 61000-4-5 (2 Ω), R_C = 2.2 kΩ(3)	2.5	kV
V_{ESD}	IN_I	ESD protection, IEC 61000-4-2, per input, R_{IN} = 2.2 kΩ(4) Air discharge Contact discharge	15 8	kV

1. *Test set-up, see application Figure 2*
2. *Refer to AN2846 and AN3031 for test setup and measurement results.*
3. *For R_I, use a resistor able to withstand the surge (MELF resistor as example), else place bidirectional TVS between field input and GND with a low-power resistor in series for R_I. Against 1 kV / 42 Ω 1.2 / 50 µs surges, recommended TVS are SPT02-236DDB or SMAJ33CA.*
4. *The package of the resistor should be large enough to prevent the arcing across the two resistor pads. Arcing depends on the ESD level applied to the field input and the application's pollution degree.*

Table 5. Operating conditions

Symbol	Pin	Parameter name	Conditions	Value	Unit
V_{CC}	V_C	Bus power supply DC voltage	R_C > 500 Ω	15 to 35(1)	V
V_{DD}	V_{DD}	Internal logic power supply voltage		5	V
I_{DD}	V_{DD}	Internal logic power supply voltage	R_C > 500 Ω	10	mA
V_I	IN	Input repetitive steady state voltage	R_I = 2.2 kΩ(2)	-30 to 35	V
V_{LD}	LD_X	Maximum LED output voltage, X = 1 to 8		2.7	V
F_{IN} max.	IN	Maximum single input frequency 8-bit mode		20	kHz
F_{SCK} max.		Maximum SPI clock frequency		0.1 to 2	MHz
R_{OSC}	OSC	Filter oscillator resistance range		15 k to 1.5 M	Ω
LV	SCK, /CS, MOSI, MISO, /MISO	Logic input / output voltage		0 to 5.5	V
T_{amb}	All	Operating ambient temperature range	V_{CC} ≤ 30 V	-40 to 85	°C
			V_{CC} ≤ 24 V, $R_{th(j-a)}$ = 70 °C/W	-40 to 105	
T_j		Operating junction temperature range		-40 to 150	°C

1. *32 V in DC; 35 V during 0.5 s max*
2. $V_I = V_{IN} + R_I \times I_{IN}$

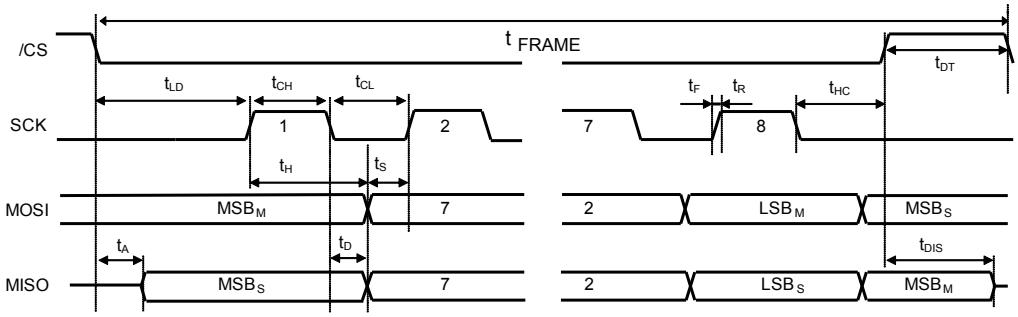
Table 6. DC electrical characteristics based on figure 2 (T_{amb} = 25 °C, V_{CC} = 24 V, V_{DD} = 5 V respect to COM ground pin; unless otherwise specified)

Symbol	Pin	Name	Conditions	Min.	Typ.	Max.	Unit
Input current limitation							
I_{LIM}	IN_X	Input current limit	V_{IN} = 5.5 to 26 V, R_I = 2.2 kΩ	2.10	2.35	2.60	mA
I_{ON}	LD_X	On state LED current	V_I = 11 V	2			mA
V_{TLH}	IN_X	Input threshold Low-to-High	x = 1 to 8, R_I = 0 Ω		4.3		V
V_{THL}	IN_X	Input threshold High-to-Low	x = 1 to 8, R_I = 0 Ω		3.3		V
V_{THYST}	IN_X	Input threshold hysteresis	x = 1 to 8, R_I = 0 Ω		1.0		V
Input digital filter							
t_{OSC}	OSC	Oscillator period	R_{OSC} = 51 kΩ	1.13		1.37	µs
			R_{OSC} = 82 kΩ	1.65		2.08	
			R_{OSC} = 150 kΩ	2.83		3.66	
			R_{OSC} = 1200 kΩ	21		28	
t_{FT}	IN_X	Filtering time	$D_{VR} = V_{DD}$	2 x 64 x t_{OSC}		3 x 64 x t_{OSC}	µs
			$D_{VR} = COM_S$	2 x 8 x t_{OSC}		3 x 8 x t_{OSC}	

Table 7. SPI electrical characteristics (T_{amb} = 25 °C, V_{CC} = 24 V, V_{DD} = 5 V respect to COM ground pin; unless otherwise specified)

Symbol	Pin	Name	Conditions	Min.	Typ.	Max.	Unit
F_{CK}	SCK	Clock frequency				2	MHz
t_S	MOSI	Data setup time	MOSI toggling to SCK rising	25			ns
t_D	MISO	Write out propagation time	SCK falling to MISO toggling, C_{OUT} = 10 pF			50	ns
t_{LD}	SCK	Enable lead time	/CK falling to SCK rising	80			ns
t_{HC}	SCK	Clock hold time	SCK falling to /CS rising	160			ns
t_{DT}	/CS	Transfer delay time	/CS rising to /CS falling			150	ns
t_H	MOSI	Data hold time	SCK rising to MOSI toggling	25			ns
t_{DIS}	MISO	Data output disable time	/CS rising to MISO disabled			200	ns
LV_{IH}	MOSI, SCK, /CS	Logic input high voltage	Share of V_{DD}			70	%
LV_{IL}		Logic input low voltage	Share of V_{DD}	30			%
LV_{OH}	MISO, /MISO	Logic output high voltage	I_{OH} = 3 mA	4	4.75		V
LV_{OL}		Logic output low voltage	I_{OL} = 3 mA		0.25	1	V
t_{RO}, t_{FO}	MISO, /MISO	MISO signal fall/rise time	I_{MISO} = 3 mA		20		ns
t_A	MISO	Output access time	/CS falling to MISO toggling		40	80	ns
D_UC_Y	SCK	Clock duty cycle		25		75	%

Figure 5. Time diagram



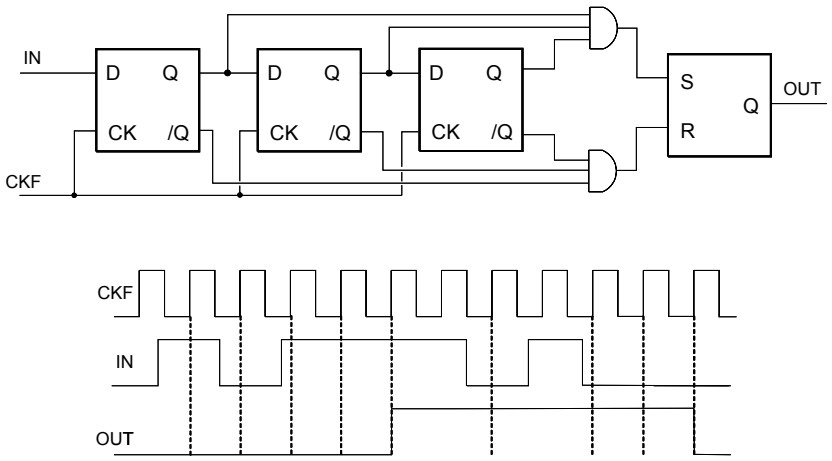
3 Functional description

3.1 Input digital glitch / debounce filter

In order to reduce glitches and noise at the inputs, a digital filter is implemented between the input state comparator and the input state register, making an analog RC filter unnecessary for most applications. Being placed in the front end of the module, this filter increases the transient immunity of the SCLT and its SPI logic circuitry.

The digital filter consists of a 2-step sampling circuit that is controlled by an oscillator as shown on Figure 6.

Figure 6. Two step digital filter placed after the analog section of the logic input



The filtering time t_{FT} is set by the external oscillator resistor and is a function of the oscillator period t_{CKF}:

- $2 \times t_{CKF} < t_{FT} < 3 \times t_{CKF}$
- t_{CKF} = Divider ratio x t_{OSC}

The clock divider ratio is set to 8 when the pin DVR is connected to COM_S or it is set to 64 when it is connected to V_{DD}.

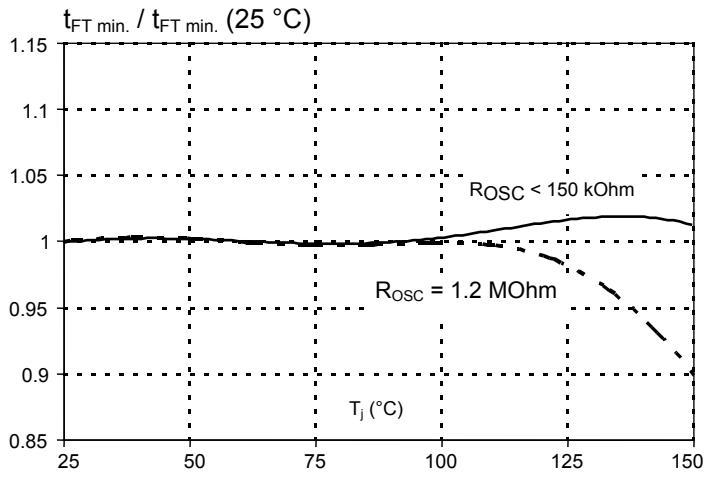
This delay time can be adjusted as shown on the Table 8.

Table 8. Typical setting of the digital glitch filter timings

Input speed		Fast				Medium		Slow	
Maximum input frequency (kHz) (1)		30		11.4		2.5		0.186	
Filter time (µs) (min/max)(2)	t_{FT}	18	33	45	88	210	400	2680	5380
CKF period (µs) (min/max)	t_{CKF}	9	11	23	29	106	133	1344	1792
Oscillator resistance (kΩ)	R_{OSC}	51		150		82		1200	
DVR connection		COM_S		COM_S		V_{DD}		V_{DD}	
Divider ratio		8		8		64		64	

1. *SPI sampling effect is not taken into account.*
2. *Custom resistor value can be used to set a particular filter time t_{FT}. For additional information about input signal frequency limitation and particular filter time settings, please refer to AN2846.*

Figure 7. Relative variation of minimum filter time t_{FT} versus junction temperature T_J



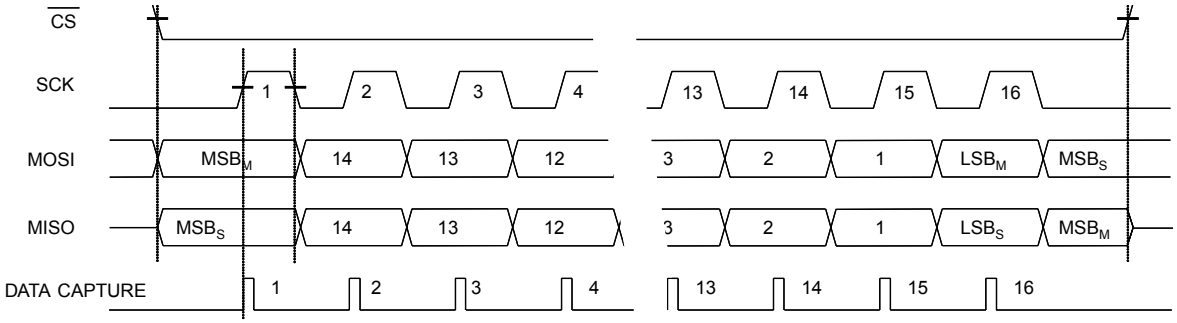
Related links

AN2846: SCLT3-8 - guidelines for use in industrial automation applications

3.2 Operation of the SCLT3-8Bx with SPI bus (C_{POL} = 0, C_{PHA} = 0)

The SPI bus master controller manages the data transfer with the chip select signal /CS and controls the data shift in the register with the clock SCK signal.

Figure 8. Serial data format frame



The transfer of the SCLT3-8Bx input states in the SPI registers starts when the chip select /CS signal falls and ends when this /CS is rising back.

The transfer of data out of the SCLT3-8Bx slave MISO output starts immediately when the chip select /CS goes low.

Then, the input MOSI is captured and presented to the shift register on each rising edge of the clock SCK. And the data are shifted in this register on each falling edge of the serial clock SCK, the data bits being written on the output MISO with the most significant bit first.

3.2.1 The serial data Input MOSI

This input signal MOSI is used to shift external data bits into the SCLT3-8Bx register from the most significant MSB bit to the lower significant one LSB. The data bits are captured by the SCLT3-8Bx on the rising edge of the serial clock signal SCK.

3.3 The SPI data transfer operation

3.3.1 The SPI data frame

The selected structure of the SPI is a 16-bit word in order to be able to implement the input state data and some control bits such as the UVA alarm, the 4 checksum bits and the two low and high state stop bits.

Depending on the biasing of the SPM pin, the data frame is 8-bits or 16-bits. When SPM is grounded, 16 bits are transmitted - 8 input data bits and 8 control bits. When SPM is connected to V_{DD}, only the 8 input data bits are transmitted.

3.3.2 The SPI data transfer

The SCLT3-8Bx transfers its 16 data bits through the SPI within one chip select Hi-Lo-Hi sequence. So, this length defines the minimum length that the shift register of the SPI master controller is able to capture: 16 bits.

The Table 8 shows the 16-bit mode way the data are transferred starting from the data bits, the control bits and ending by a stop bit.

Table 9. SPI data transfer organization versus SCLT3-8Bx input states with SPM = 0

Bit #	LSB	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
Control	High(1)	Low	PC4	PC3	PC2	PC1	/OTA	/UVA
Bit #	Bit 8	Bit 9	Bit 10	Bit 11	Bit 12	Bit 13	Bit 14	MSB
Data	IN 1	IN 2	IN 3	IN 4	IN 5	IN 6	IN 7	IN 8(2)

1. *Last OUT*
2. *First OUT*

3.4 Control bit signals of the SPI transferred data frame

3.4.1 The power bus voltage monitoring

The UVA circuit generates the alarm /UVA that is active low when the power bus voltage is lower than the activation threshold V_{CON}, 17 V typical, and it is disabled high when the power bus voltage rises above the threshold V_{COFF}, 18 V typical.

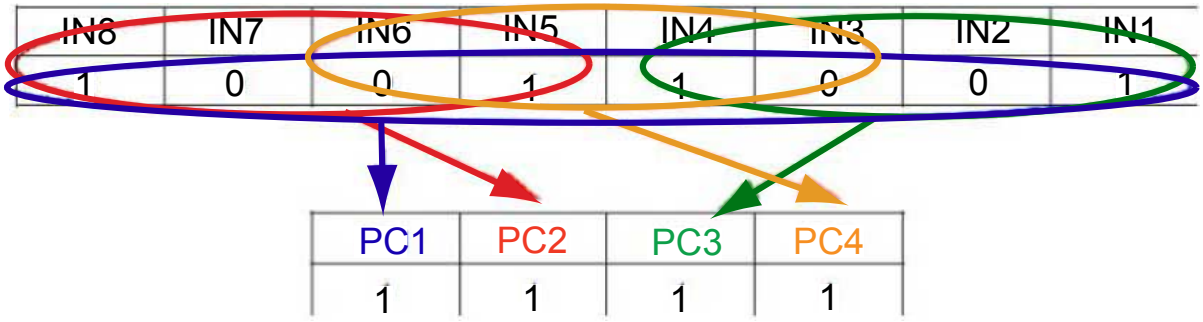
3.4.2 The over temperature alarm

The alarm signal /OTA is enabled, low state active, when the junction temperature is higher than the activation threshold T_{ON}, 150 °C typical, and it is disabled when the junction temperature falls below the threshold T_{OFF}, 140 °C typical.

3.4.3 The parity checksum bits calculation and transfer

The aim of the parity checksum bit is to detect one error in the transferred SPI word. Several parity checksum bits are generated and transmitted through the SPI on the control bit #2 to #5. In order to calculate parity bit, “exclusive NOR” operations are performed as follow:

Figure 9. SCLT3-8Bx parity bit calculation example



3.5 Loss of V_{CC} power supply

The operation of the SCLT3-8Bx is extended below the levels required in the IEC 61131-2 standard to allow the implementation of the under voltage alarm UVA as described the SPI control bit section.

If there is no more power feeding on the V_{CC} input, the SCLT3-8Bx chip goes to sleep mode, and the MISO output is forced in low state during SPI transfer attempt. The last SPI control data bit is a stop bit placed normally in high state all time: the loss of power supply is detected by checking its state: if low, the output is disabled by the internal power reset POR.

This POR signal is active in low state when V_C is less than 9 V or the internal power supply V_{DD} is less than 3.25 V.

Table 10. Logic state of the SPI output versus the power loss signal POR and the SPI chip select /CS

POR	/CS	MISO	/MISO	SPI status
1	1	Z	Z	Normal with no communication
1	0	1	0	Normal with communication
1	0	0	1	Normal with communication
0	1	Z	Z	Power loss with no communication
0	0	0	1	Power loss with communication attempt

Figure 10. Logic status of the SCLT3-8Bx power supply

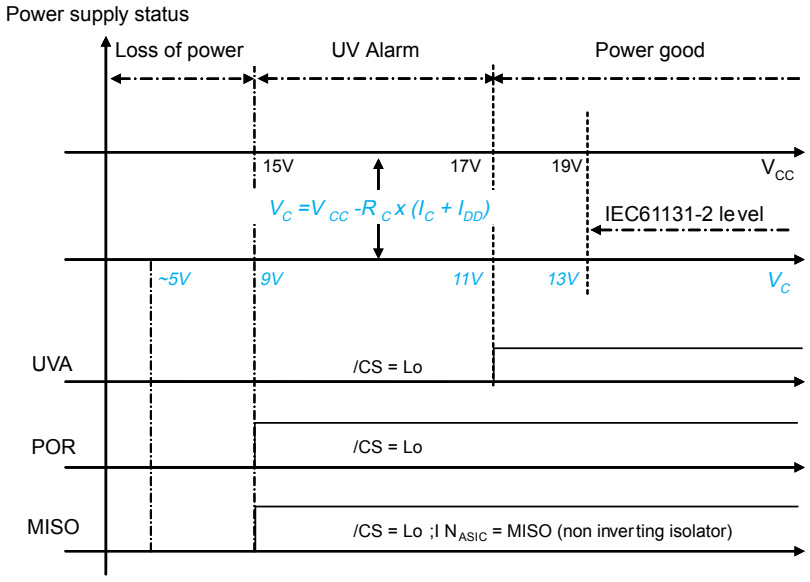
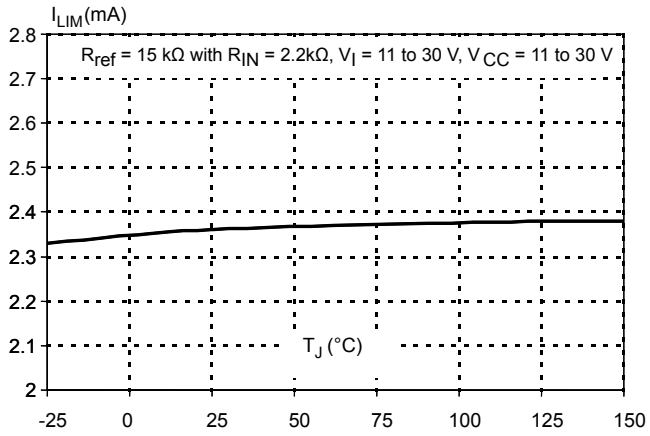


Figure 11. **Typical limiting current I_{LIM} versus junction temperature T_j**



3.6 Type 2 sensor inputs

The input current (6 mA min) of Type 2 input requires the use of two inputs of SCLT3-8Bx in parallel. The current of each channel is set to 3.5 mA by setting R_{REF} to 9.1 kΩ. The effective current is then 7 mA nominal. The proper voltage drop across the input resistor is maintained by reducing the input resistance from 2.2 kΩ to 0.75 kΩ.

Figure 12. **SCLT3-8Bx - Type 2 input configuration**

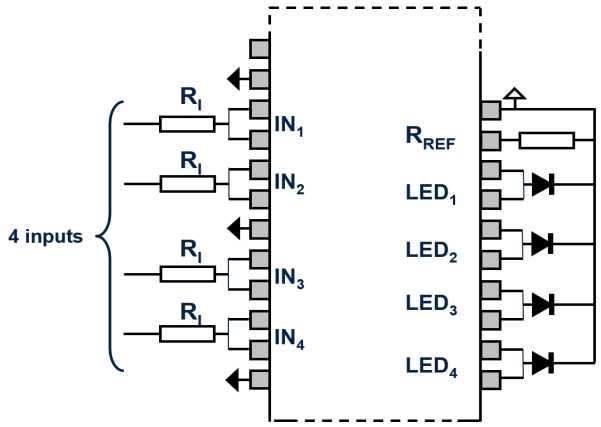
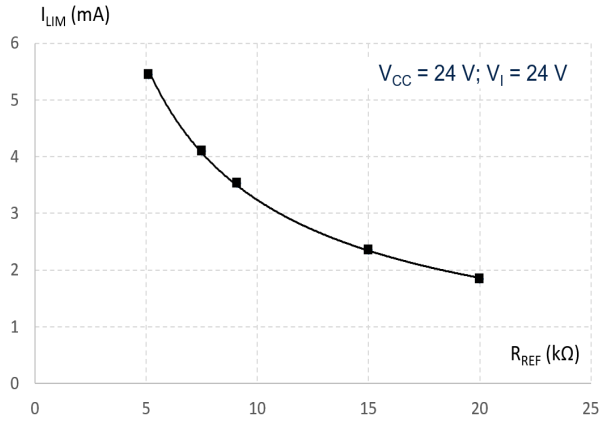


Figure 13. **Typical limiting current I_{LIM} versus R_{REF}**



Note: On the Figure 12 for greater robustness against surges, place a 1.5 kΩ resistor on each channel and connect them in parallel to get equivalent resistance value of 0.75 kΩ.

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 QFN-48L 7.0 x 7.0 mm package information

Figure 14. QFN-48L 7.0 x 7.0 mm package outline

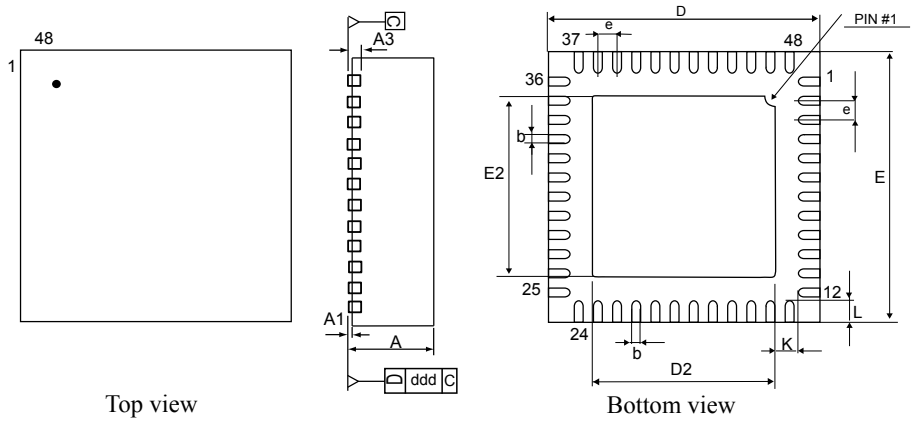


Table 11. QFN-48L 7.0 x 7.0 mm package mechanical data

Ref.	Dimensions					
	Millimeters			Inches(1)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.80	0.90	1.00	0.0315	0.0354	0.0394
A1		0.02	0.05		0.0008	0.0020
A3		0.203			0.008	
b	0.18	0.25	0.30	0.0071	0.0100	0.0118
D		7.00			0.275	
E		7.00			0.275	
e		0.50			0.019	
D2	5.00	5.15	5.25	0.197	0.203	0.206
E2	5.00	5.15	5.25	0.197	0.203	0.206
K	0.20			0.008		
L	0.30	0.40	0.50	0.011	0.015	0.019

1. *Values in inches are converted from mm and rounded to 4 decimal digits.*

Figure 15. Footprint recommendations

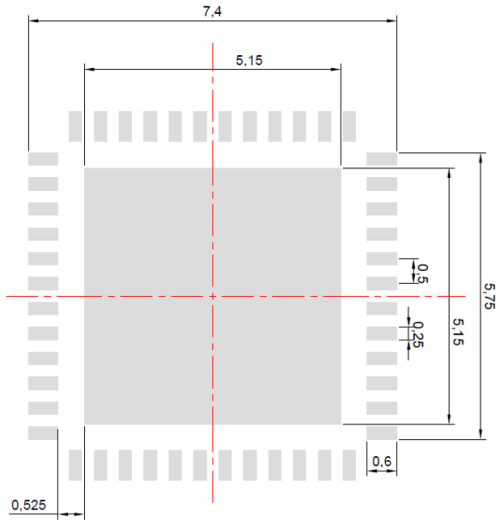
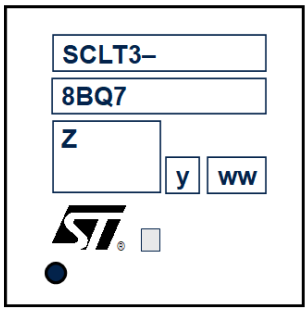


Figure 16. Marking



Dot indicates pin 1

ST logo

ECOPACK grade

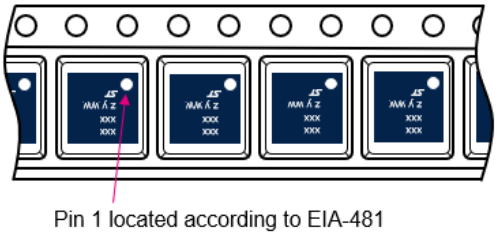
Z = manufacturing location and traceability information

yww = datecode

y = year

ww = week

Figure 17. Package orientation in reel



Pin 1 located according to EIA-481

Note: Pocket dimensions are not on scale. Only pin 1 mark must be used to orient the component for its placement on a PCB.

Figure 18. Tape and reel orientation

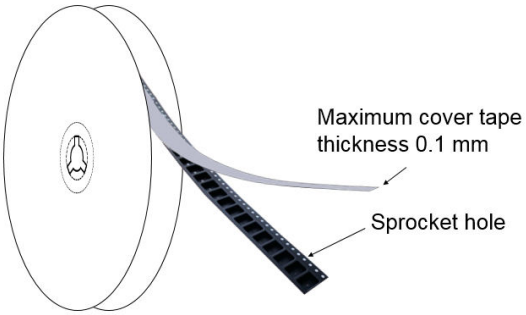


Figure 19. 13” reel dimensions values (mm)

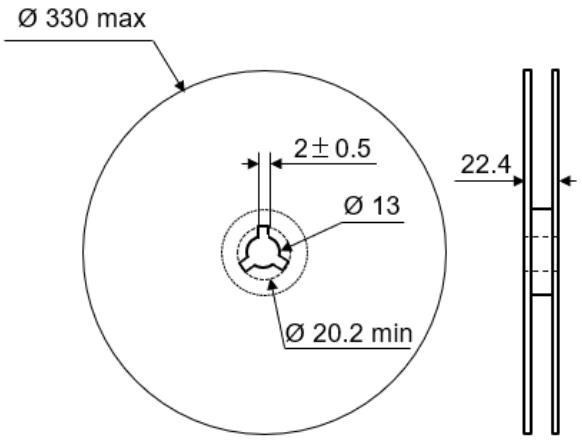


Figure 20. Inner box dimension values

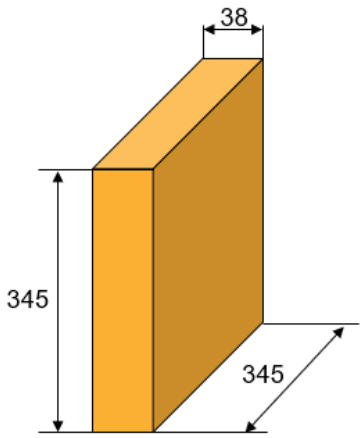
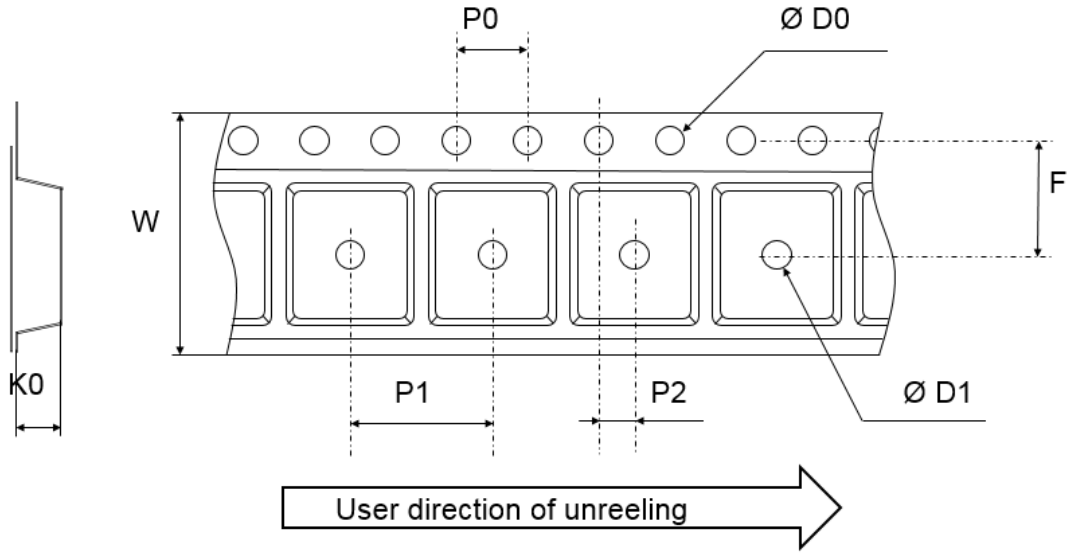


Figure 21. **Tape outline**



Note: Pocket dimensions are not on scale
Pocket shape may vary depending on package

Table 12. **Tape dimension values**

Ref.	Dimensions		
	Millimeters		
	Min.	Typ.	Max.
D0	1.50	1.55	1.60
D1	1.50		
F	7.40	7.50	7.60
K0	1.00	1.10	1.20
P0	3.90	4.00	4.10
P1	11.90	12.00	12.10
P2	1.90	2.00	2.10
W	15.70	16.00	16.30

4.2 HTSSOP-38 package information

Figure 22. **HTSSOP-38 package outline**

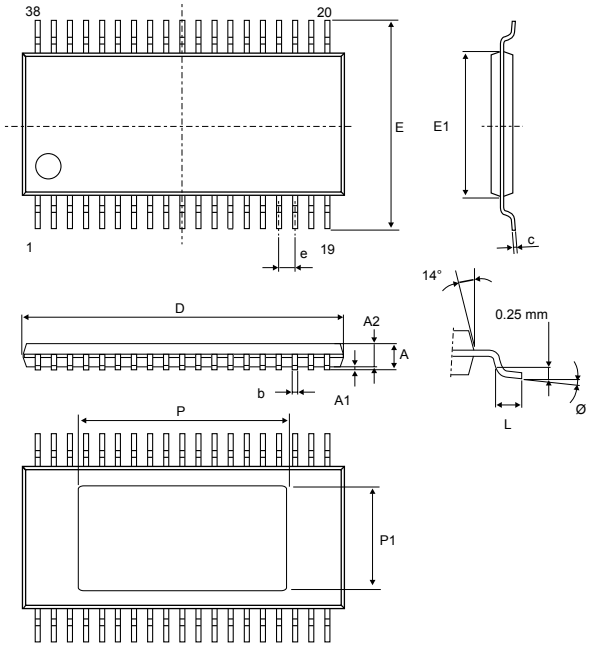


Table 13. **HTSSOP-38 package mechanical data**

Ref.	Dimensions					
	Millimeters			Inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.10			0.043
A1	0.05		0.15	0.002		0.006
A2	0.85	0.90	0.95	0.033	0.035	0.037
b	0.17		0.27	0.007		0.011
c	0.09		0.20	0.003		0.008
D	9.60	9.70	9.80	0.378	0.382	0.386
E1	4.30	4.40	4.50	0.169	0.173	0.177
e		0.50			0.020	
E		6.40			0.252	
L	0.50	0.60	0.70	0.020	0.024	0.027
P	6.40	6.50	6.60	0.252	0.256	0.260
P1	3.10	3.20	3.30	0.122	0.126	0.130
Ø	0°		8°	0°		8°

1. *Values in inches are converted from mm and rounded to 4 decimal digits.*

Figure 23. Footprint recommendations

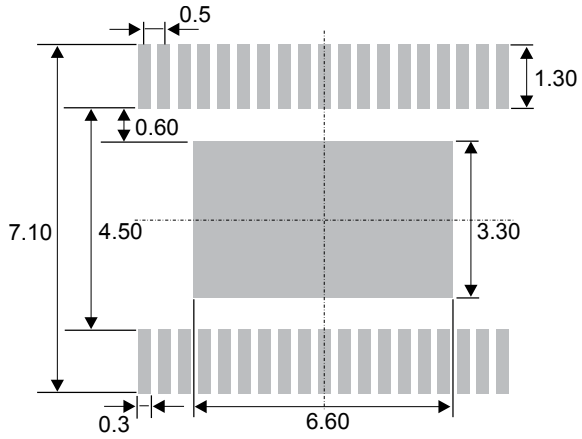
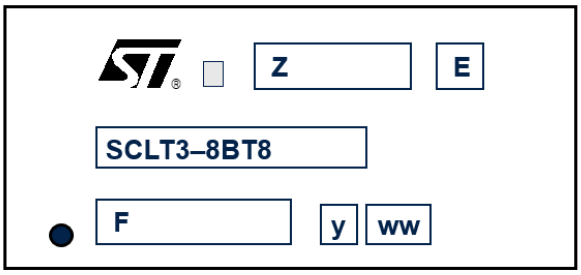
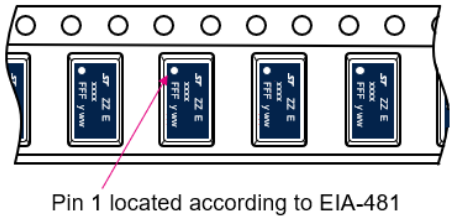


Figure 24. Marking



Dot indicates pin 1
ST logo
ECOPACK grade
E = eco level
F = traceability information
Z = manufacturing location and traceability information
yww = datecode
y = year
ww = week

Figure 25. Package orientation in reel



Pin 1 located according to EIA-481

Note: Pocket dimensions are not on scale.
Only pin 1 mark must be used to orient the component for its placement on a PCB.

Figure 26. Tape and reel orientation

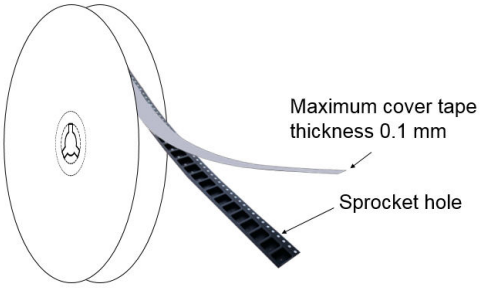


Figure 27. 13” reel dimensions values (mm)

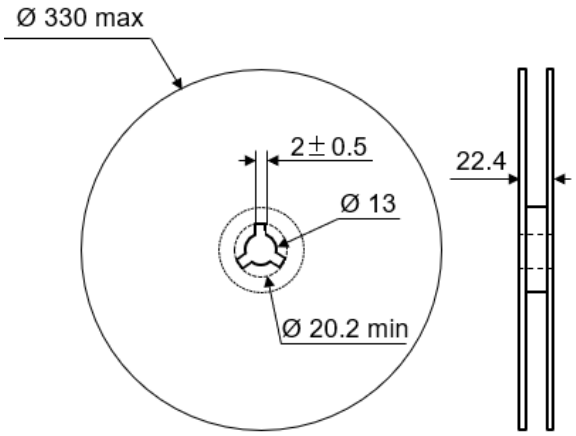


Figure 28. Inner box dimension values

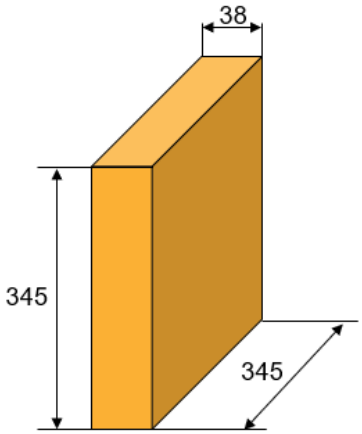
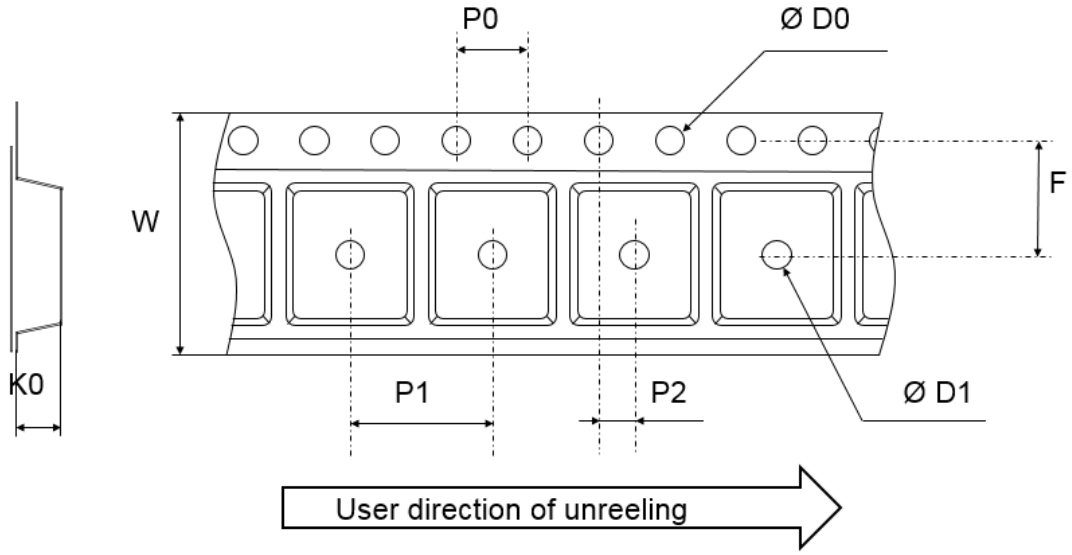


Figure 29. **Tape outline**



Note: Pocket dimensions are not on scale
Pocket shape may vary depending on package

Table 14. **Tape dimension values**

Ref.	Dimensions		
	Millimeters		
	Min.	Typ.	Max.
D0	1.50	1.55	1.60
D1	1.50		
F	7.40	7.50	7.60
K0	1.40	1.50	1.60
P0	3.90	4.00	4.10
P1	11.90	12.00	12.10
P2	1.90	2.00	2.10
W	15.70	16.00	16.30

5 Ordering information

Figure 30. **Ordering information scheme**

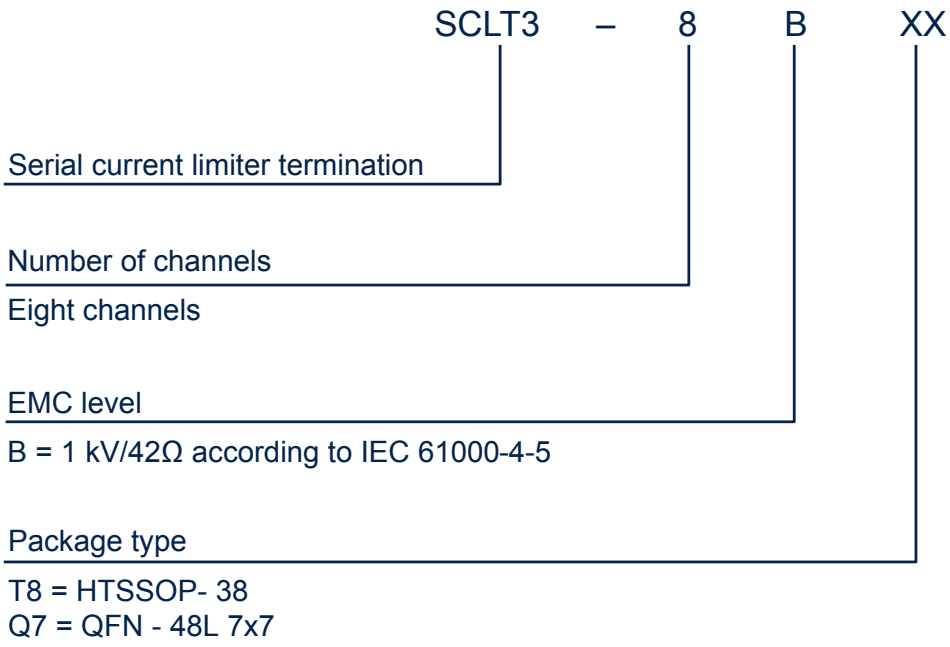


Table 15. **Ordering information**

Order code	Marking[1]	Package	Weight	Base qty.	Delivery mode
SCLT3-8BT8-TR	SCLT3-8BT8	HTSSOP-38	114 mg	2500	Tape and reel
SCLT3-8BT8	SCLT3-8BT8	HTSSOP-38	114 mg	50	Tube
SCLT3-8BQ7-TR	SCLT3-8BQ7	QFN-48L 7.0 x 7.0	130 mg	2500	Tape and reel

1. *The marking can be rotated to differentiate assembly location.*

Revision history

Table 16. **Document revision history**

Date	Revision	Changes
29-Jul-2016	1	Initial release.
12-Nov-2015	2	Updated *Table 4*.
05-Dec-2016	3	Added part number previously included in the datasheet DocID15191. Updated document accordingly. Minor text changes.
07-Oct-2021	4	Updated Figure 2.
03-Jan-2022	5	Updated Section 5 Ordering information.
12-Jun-2023	6	Updated *Features*, *Descrition*, *Application*, Figure 2, Figure 4, Table 6, Table 7, Section 3.1, Section 4.1 QFN-48L 7.0 x 7.0 mm package information and Section 4.2 HTSSOP-38 package information.
24-Aug-23	7	Updated Table 2.