

74HC74

Dual D Flip-Flop with Set and Reset

High-Performance Silicon-Gate CMOS

The 74HC74 is identical in pinout to the LS74. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device consists of two D flip-flops with individual Set, Reset, and Clock inputs. Information at a D-input is transferred to the corresponding Q output on the next positive going edge of the clock input. Both Q and \bar{Q} outputs are available from each flip-flop. The Set and Reset inputs are asynchronous.

Features

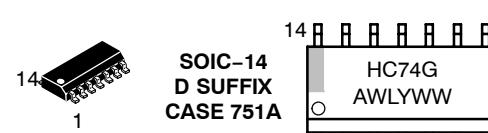
- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the JEDEC Standard No. 7A Requirements
- ESD Performance: HBM > 2000 V; Machine Model > 200 V
- Chip Complexity: 128 FETs or 32 Equivalent Gates
- Pb-Free Packages are Available



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MARKING DIAGRAMS



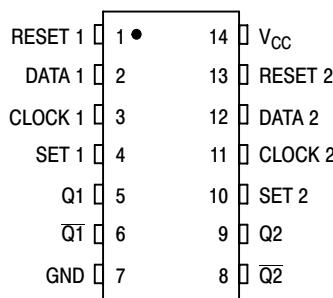
HC74 = Device Code
A = Assembly Location
L, WL = Wafer Lot
Y = Year
W, WW = Work Week
G or ■ = Pb-Free Package

(Note: Microdot may be in either location)

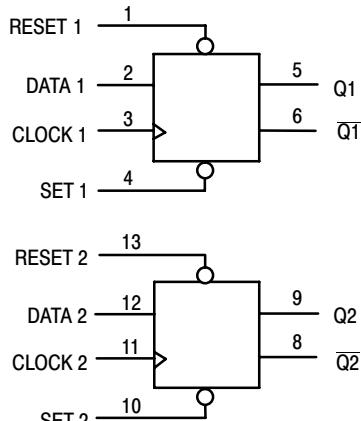
ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

PIN ASSIGNMENT



LOGIC DIAGRAM



FUNCTION TABLE

| Inputs | | | | Outputs | |
|--------|-------|-------|------|-----------|----|
| Set | Reset | Clock | Data | Q | Q̄ |
| L | H | X | X | H | L |
| H | L | X | X | L | H |
| L | L | X | X | H* | H* |
| H | H | ✓ | H | H | L |
| H | H | ✓ | L | L | H |
| H | H | L | X | No Change | |
| H | H | H | X | No Change | |
| H | H | ✓ | X | No Change | |

*Both outputs will remain high as long as Set and Reset are low, but the output states are unpredictable if Set and Reset go high simultaneously.

MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|------------------|---|-------------------------------|------|
| V _{CC} | DC Supply Voltage (Referenced to GND) | –0.5 to +7.0 | V |
| V _{in} | DC Input Voltage (Referenced to GND) | –0.5 to V _{CC} + 0.5 | V |
| V _{out} | DC Output Voltage (Referenced to GND) | –0.5 to V _{CC} + 0.5 | V |
| I _{in} | DC Input Current, per Pin | ±20 | mA |
| I _{out} | DC Output Current, per Pin | ±25 | mA |
| I _{CC} | DC Supply Current, V _{CC} and GND Pins | ±50 | mA |
| P _D | Power Dissipation in Still Air, SOIC Package† TSSOP Package† | 500 450 | mW |
| T _{stg} | Storage Temperature | –65 to +150 | °C |
| T _L | Lead Temperature, 1 mm from Case for 10 Seconds (SOIC or TSSOP Package) | 260 300 | °C |

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

†Derating — SOIC Package: –7 mW/°C from 65° to 125°C
TSSOP Package: –6.1 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Min | Max | Unit | |
|------------------------------------|--|--|------------------|---------------------------|----|
| V _{CC} | DC Supply Voltage (Referenced to GND) | 2.0 | 6.0 | V | |
| V _{in} , V _{out} | DC Input Voltage, Output Voltage (Referenced to GND) | 0 | V _{CC} | V | |
| T _A | Operating Temperature, All Package Types | –55 | +125 | °C | |
| t _r , t _f | Input Rise and Fall Time (Figures 1, 2, 3) | V _{CC} = 2.0 V V _{CC} = 3.0 V V _{CC} = 4.5 V V _{CC} = 6.0 V | 0 0 0 0 | 1000 600 500 400 | ns |

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

| Symbol | Parameter | Test Conditions | V _{CC} (V) | Guaranteed Limit | | | Unit |
|-----------------|--|--|--------------------------|---------------------------|---------------------------|---------------------------|------|
| | | | | –55 to 25°C | ≤ 85°C | ≤ 125°C | |
| V _{IH} | Minimum High-Level Input Voltage | V _{out} = 0.1 V or V _{CC} – 0.1 V I _{out} ≤ 20 µA | 2.0 3.0 4.5 6.0 | 1.5 2.1 3.15 4.2 | 1.5 2.1 3.15 4.2 | 1.5 2.1 3.15 4.2 | V |
| V _{IL} | Maximum Low-Level Input Voltage | V _{out} = 0.1 V or V _{CC} – 0.1 V I _{out} ≤ 20 µA | 2.0 3.0 4.5 6.0 | 0.5 0.9 1.35 1.8 | 0.5 0.9 1.35 1.8 | 0.5 0.9 1.35 1.8 | V |
| V _{OH} | Minimum High-Level Output Voltage | V _{in} = V _{IH} or V _{IL} I _{out} ≤ 20 µA | 2.0 4.5 6.0 | 1.9 4.4 5.9 | 1.9 4.4 5.9 | 1.9 4.4 5.9 | V |
| | | V _{in} = V _{IH} or V _{IL} I _{out} ≤ 2.4 mA I _{out} ≤ 4.0 mA I _{out} ≤ 5.2 mA | 3.0 4.5 6.0 | 2.48 3.98 5.48 | 2.34 3.84 5.34 | 2.2 3.7 5.2 | |
| V _{OL} | Maximum Low-Level Output Voltage | V _{in} = V _{IH} or V _{IL} I _{out} ≤ 20 µA | 2.0 4.5 6.0 | 0.1 0.1 0.1 | 0.1 0.1 0.1 | 0.1 0.1 0.1 | V |
| | | V _{in} = V _{IH} or V _{IL} I _{out} ≤ 2.4 mA I _{out} ≤ 4.0 mA I _{out} ≤ 5.2 mA | 3.0 4.5 6.0 | 0.26 0.26 0.26 | 0.33 0.33 0.33 | 0.4 0.4 0.4 | |
| I _{in} | Maximum Input Leakage Current | V _{in} = V _{CC} or GND | 6.0 | ±0.1 | ±1.0 | ±1.0 | µA |
| I _{CC} | Maximum Quiescent Supply Current (per Package) | V _{in} = V _{CC} or GND I _{out} = 0 µA | 6.0 | 2.0 | 20 | 80 | µA |

NOTE: Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input t_r = t_f = 6.0 ns)

| Symbol | Parameter | V _{CC} (V) | Guaranteed Limit | | | Unit |
|--|--|--------------------------|-----------------------|-----------------------|------------------------|------|
| | | | –55 to 25°C | ≤ 85°C | ≤ 125°C | |
| f _{max} | Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4) | 2.0 3.0 4.5 6.0 | 6.0 15 30 35 | 4.8 10 24 28 | 4.0 8.0 20 24 | MHz |
| t _{PLH} , t _{PHL} | Maximum Propagation Delay, Clock to Q or \bar{Q} (Figures 1 and 4) | 2.0 3.0 4.5 6.0 | 100 75 20 17 | 125 90 25 21 | 150 120 30 26 | ns |
| t _{PLH} , t _{PHL} | Maximum Propagation Delay, Set or Reset to Q or \bar{Q} (Figures 2 and 4) | 2.0 3.0 4.5 6.0 | 105 80 21 18 | 130 95 26 22 | 160 130 32 27 | ns |
| t _{TLH} , t _{THL} | Maximum Output Transition Time, Any Output (Figures 1 and 4) | 2.0 3.0 4.5 6.0 | 75 30 15 13 | 95 40 19 16 | 110 55 22 19 | ns |
| C _{in} | Maximum Input Capacitance | — | 10 | 10 | 10 | pF |

NOTE: For propagation delays with loads other than 50 pF, and information on typical parametric values, see Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

| C _{PD} | Power Dissipation Capacitance (Per Flip-Flop)* | Typical @ 25°C, V _{CC} = 5.0 V | | pF |
|-----------------|--|---|----|----|
| | | 32 | 32 | |

* Used to determine the no-load dynamic power consumption: P_D = C_{PD} V_{CC}²f + I_{CC} V_{CC}. For load considerations, see Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

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TIMING REQUIREMENTS (Input $t_r = t_f = 6.0$ ns)

| Symbol | Parameter | V _{CC} (V) | Guaranteed Limit | | | Unit |
|------------|--|--------------------------|---------------------------|---------------------------|---------------------------|------|
| | | | – 55 to 25°C | ≤ 85°C | ≤ 125°C | |
| t_{su} | Minimum Setup Time, Data to Clock (Figure 3) | 2.0 3.0 4.5 6.0 | 80 35 16 14 | 100 45 20 17 | 120 55 24 20 | ns |
| t_h | Minimum Hold Time, Clock to Data (Figure 3) | 2.0 3.0 4.5 6.0 | 3.0 3.0 3.0 3.0 | 3.0 3.0 3.0 3.0 | 3.0 3.0 3.0 3.0 | ns |
| t_{rec} | Minimum Recovery Time, Set or Reset Inactive to Clock (Figure 2) | 2.0 3.0 4.5 6.0 | 8.0 8.0 8.0 8.0 | 8.0 8.0 8.0 8.0 | 8.0 8.0 8.0 8.0 | ns |
| t_w | Minimum Pulse Width, Clock (Figure 1) | 2.0 3.0 4.5 6.0 | 60 25 12 10 | 75 30 15 13 | 90 40 18 15 | ns |
| t_w | Minimum Pulse Width, Set or Reset (Figure 2) | 2.0 3.0 4.5 6.0 | 60 25 12 10 | 75 30 15 13 | 90 40 18 15 | ns |
| t_r, t_f | Maximum Input Rise and Fall Times (Figures 1, 2, 3) | 2.0 3.0 4.5 6.0 | 1000 800 500 400 | 1000 800 500 400 | 1000 800 500 400 | ns |

ORDERING INFORMATION

| Device | Package | Shipping [†] |
|-------------|-------------------|-----------------------|
| 74HC74D | SOIC-14 | 55 Units / Rail |
| 74HC74DG | SOIC-14 (Pb-Free) | |
| 74HC74DR2 | SOIC-14 | 2500 / Tape & Reel |
| 74HC74DR2G | SOIC-14 (Pb-Free) | |
| 74HC74DTR2 | TSSOP-14* | |
| 74HC74DTR2G | TSSOP-14* | |

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*This package is inherently Pb-Free.

SWITCHING WAVEFORMS

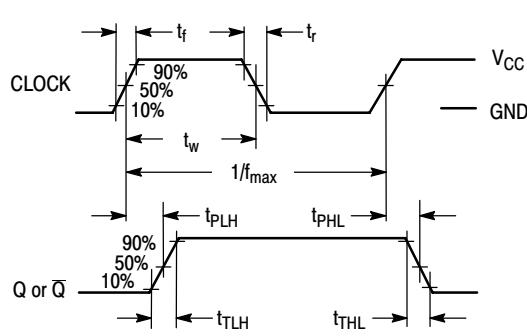


Figure 1.

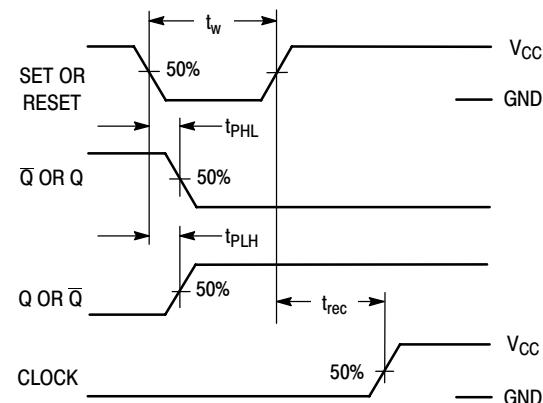


Figure 2.

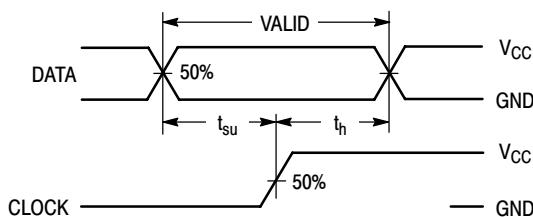
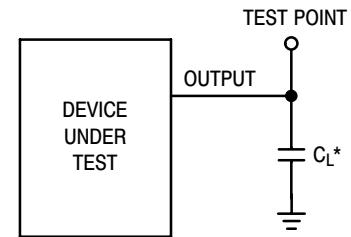


Figure 3.



*Includes all probe and jig capacitance

Figure 4.

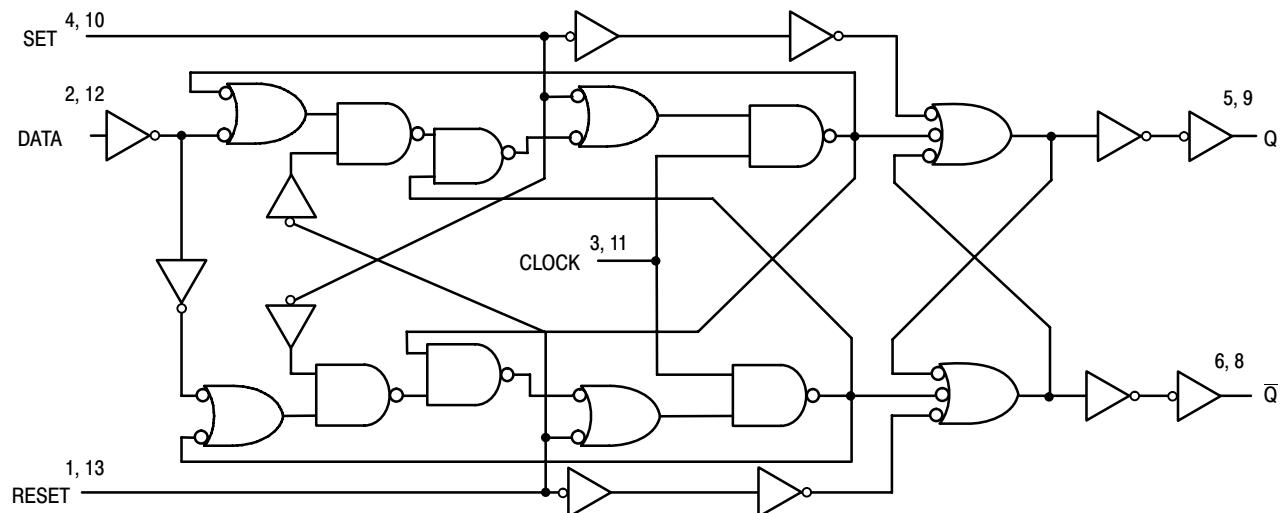
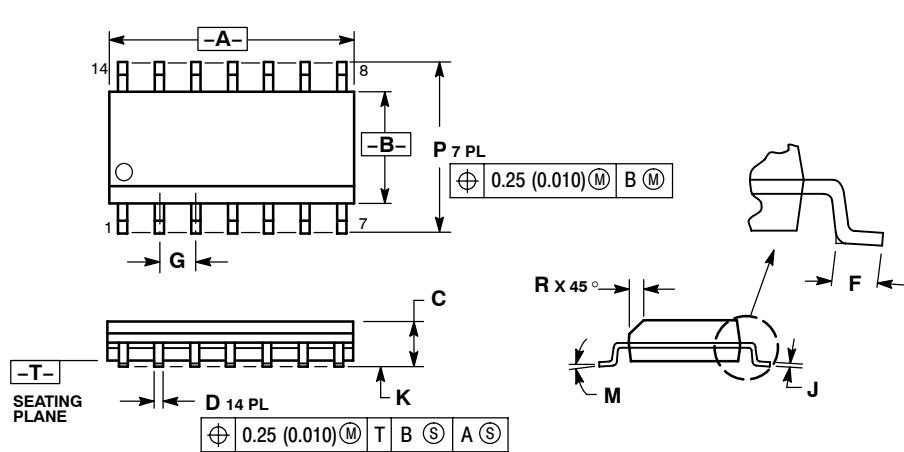


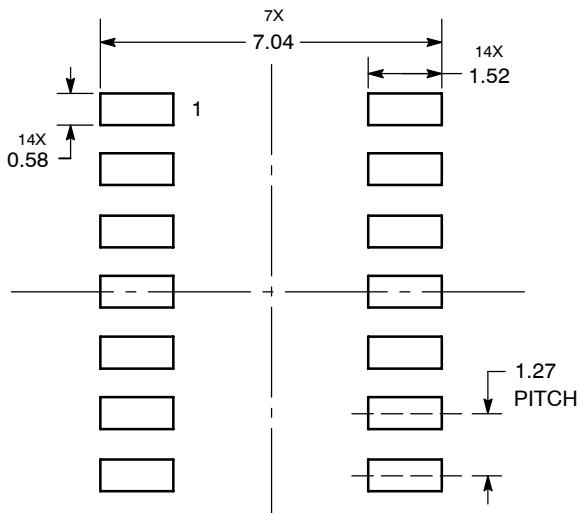
Figure 5. EXPANDED LOGIC DIAGRAM

PACKAGE DIMENSIONS

SOIC-14
CASE 751A-03
ISSUE H



SOLDERING FOOTPRINT*

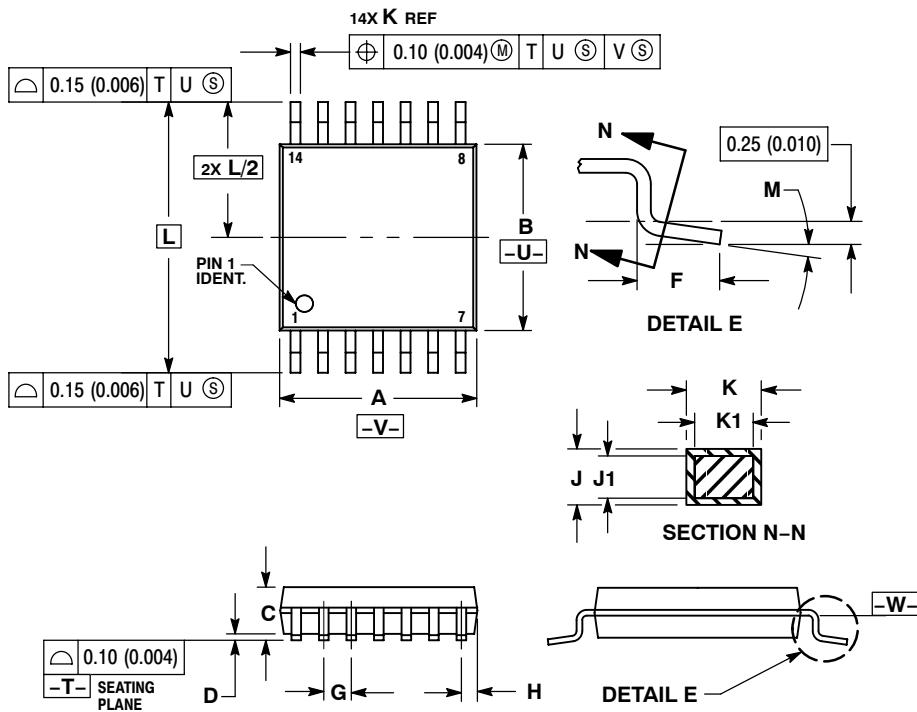


DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|--------|-------|
| | MIN | MAX | MIN | MAX |
| A | 8.55 | 8.75 | 0.337 | 0.344 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.054 | 0.068 |
| D | 0.35 | 0.49 | 0.014 | 0.019 |
| F | 0.40 | 1.25 | 0.016 | 0.049 |
| G | 1.27 | BSC | 0.050 | BSC |
| J | 0.19 | 0.25 | 0.008 | 0.009 |
| K | 0.10 | 0.25 | 0.004 | 0.009 |
| M | 0° | 7° | 0° | 7° |
| P | 5.80 | 6.20 | 0.228 | 0.244 |
| R | 0.25 | 0.50 | 0.010 | 0.019 |

PACKAGE DIMENSIONS

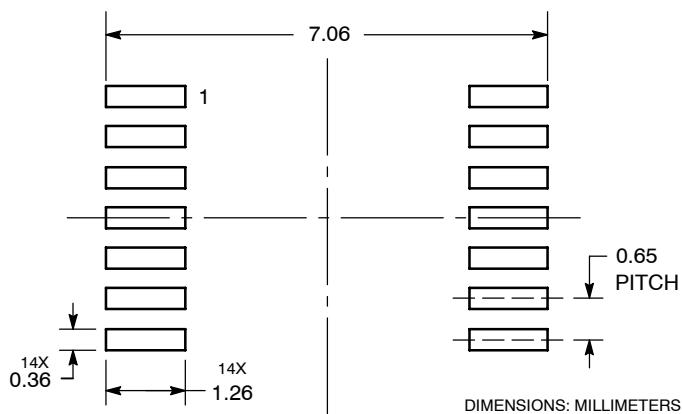
TSSOP-14
CASE 948G-01
ISSUE B

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|--------|-------|
| | MIN | MAX | MIN | MAX |
| A | 4.90 | 5.10 | 0.193 | 0.200 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | --- | 1.20 | --- | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 | BSC | 0.026 | BSC |
| H | 0.50 | 0.60 | 0.020 | 0.024 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 | BSC | 0.252 | BSC |
| M | 0 ° | 8 ° | 0 ° | 8 ° |

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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