

Philips Semiconductors

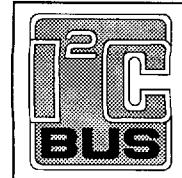
Objective specification

I²C-bus programmable modulator for negative video modulation and FM sound

TDA8720T; TDA8720M

FEATURES

- Video amplifier with clamping circuit, white clip circuit and automatic gain control circuit which allows handling of video signals between 0.7 and 1.4 V (p-p)
- FM sound modulator
- Asymmetrical and symmetrical RF outputs
- Symmetrical RF oscillator covering more than 20 channels with only a few external components
- I²C-bus receiver for frequency setting and test-mode selection
- Phase-locked-loop frequency synthesizer
- On-chip power supply regulator.



APPLICATIONS

- Video recorders
- Video generators
- Cable converters.

GENERAL DESCRIPTION

The TDA8720 is a programmable modulator which has been designed to generate an RF TV channel from a baseband video signal and a baseband audio signal in applications of negative video and FM sound standards.

It is especially suitable for video generators, video recorders and cable converters. The picture carrier frequency is set exactly to the correct channel frequency by a PLL synthesizer which is programmed in accordance with the I²C-bus format.

QUICK REFERENCE DATA

$V_{DD} = 5$ V and $T_{amb} = 25$ °C after the IC has reached thermal equilibrium; unless otherwise specified.

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|--------------------|---|--|------|------|--------|------------------------|
| V_{DDA}, V_{DDD} | analog and digital supply voltage | | 4.5 | 5.0 | 5.5 | V |
| I_{DD} | total supply current | | 41 | 51 | 61 | mA |
| f_{SYN} | synthesizer frequency range | | — | — | 900.25 | MHz |
| $V_{19(p-p)}$ | video input voltage level (peak-to-peak value) | | 0.7 | 1.0 | 1.4 | V |
| V_{RF} | RF output voltage level asymmetrical on a $75\ \Omega$ load | $f = 471.25$ MHz | 75 | 78 | 82 | $\text{dB}\mu\text{V}$ |
| | | $f = 663.25$ MHz | 73 | 76 | 80 | $\text{dB}\mu\text{V}$ |
| m | video modulation depth | colour bars pattern | — | 83 | — | % |
| $V_{1(rms)}$ | maximum audio input voltage level (RMS value) | before pre-emphasis filter | — | 0.5 | — | V |
| Δf | FM deviation in audio subcarrier | $f = 400$ Hz; $V_1 = 0.5$ V(RMS); before pre-emphasis filter | — | 25 | — | kHz |

ORDERING INFORMATION

| EXTENDED TYPE NUMBER | PACKAGE | | | |
|----------------------|---------|--------------|----------|---------|
| | PINS | PIN POSITION | MATERIAL | CODE |
| TDA8720T | 20 | SO20L | plastic | SOT163A |
| TDA8720M | 20 | SSOP20 | plastic | SOT266A |

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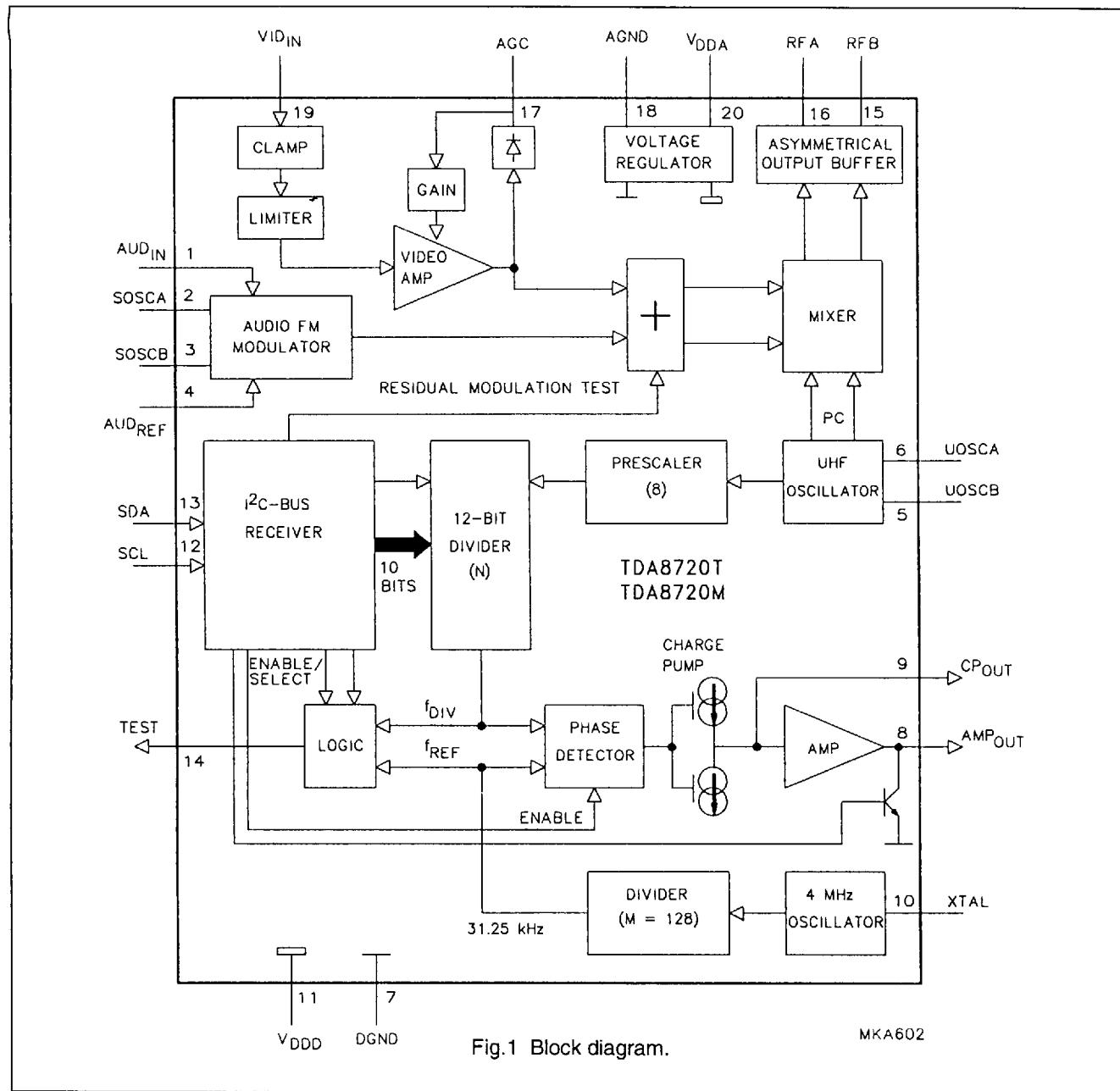


Fig. 1 Block diagram.

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PINNING

| SYMBOL | PIN | DESCRIPTION |
|--------------------|-----|---|
| AUD _{IN} | 1 | audio input |
| SOSCA | 2 | sound oscillator A |
| SOSCB | 3 | sound oscillator B |
| AUD _{REF} | 4 | audio reference input |
| UOSCB | 5 | UHF oscillator B |
| UOSCA | 6 | UHF oscillator A |
| DGND | 7 | digital ground |
| AMP _{OUT} | 8 | tuning amplifier output |
| CP _{OUT} | 9 | charge pump output |
| XTAL | 10 | crystal oscillator |
| V _{DDD} | 11 | digital supply voltage |
| SCL | 12 | serial clock (I ² C bus) |
| SDA | 13 | serial data (I ² C bus) |
| TEST | 14 | test output |
| RFB | 15 | RF output B |
| RFA | 16 | RF output A |
| AGC | 17 | automatic gain control of video amplifier |
| AGND | 18 | analog ground |
| VID _{IN} | 19 | video input |
| V _{DDA} | 20 | analog supply voltage |

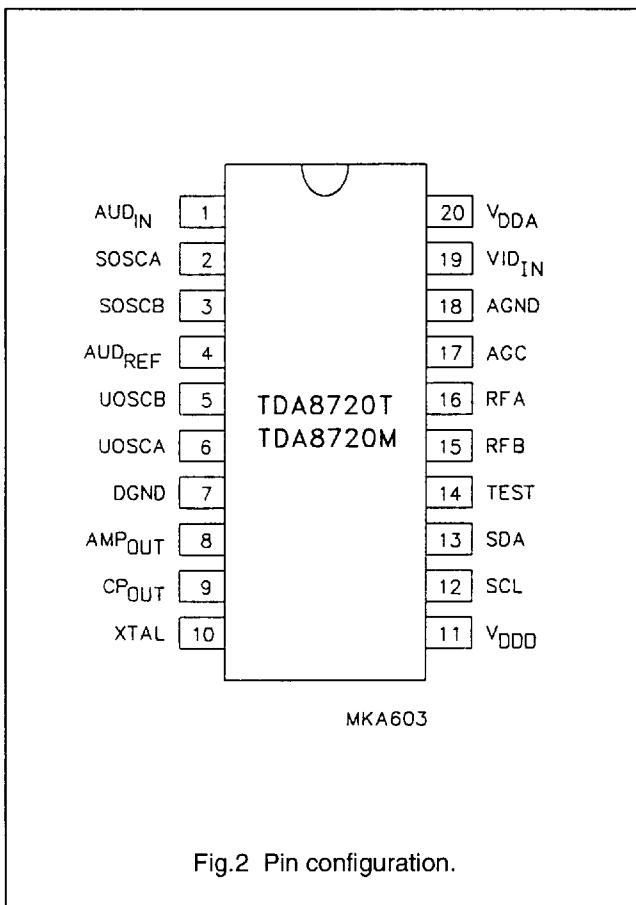


Fig.2 Pin configuration.

I²C-bus programmable modulator for negative video modulation and FM sound

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FUNCTIONAL DESCRIPTION

The TDA8720 is a programmable modulator which can be divided into two main blocks:

- a modulator for negative video modulation and FM sound TV standards
- a programmable PLL frequency synthesizer

The video part of the modulator consists of:

- a clamping circuit which sets the internal reference voltage level to the bottom of the synchronizing pulse.
- a limiter which clips strong signals higher than 1.5 V to avoid overmodulation.
- a peak white detector which measures the amplitude of the top white level and then controls the gain of the video amplifier. The capacitor for the detector, C17 (see Fig.5) is external and may therefore be adapted in the application.
- a video amplifier with variable gain which delivers a constant amplitude when the external video signal is within the range 0.7 to 1.4 V.

The audio part of the modulator consists of an FM sound modulator. The frequency of the sound subcarrier is set in the application by external components C3, L3 and R3 (see Fig.5).

The RF part of the modulator consists of:

- an oscillator which operates at the required picture carrier frequency. The range of the oscillator is determined by the application. In our reference measuring set-up, we guarantee a range of 471.25 to 663.25 MHz, (channel 21 to channel 45 of G standard) with L5, C5, C6 and D5 (see Fig.5).

- an RF mixer which combines the video signal and the sound subcarrier to build a baseband TV channel. The baseband signal is then mixed with the oscillator signal to produce the RF TV channel. The mixer has two outputs which can be used as either two independent asymmetrical outputs or as one symmetrical output.

The channel frequency is set by a programmable PLL frequency synthesizer.

The PLL frequency synthesizer controls the oscillator frequency in accordance with the following formula:

$$f_{\text{OSC}} = 8 \times N \times f_{\text{REF}}$$

Where:

- f_{OSC} is the local oscillator frequency
- N is a 12-bit dividing number (10 bits are programmable)
- f_{REF} is the crystal frequency (f_{XTAL}) divided by 128.

The circuit therefore allows a minimum step of 250 kHz internally and a software controlled step of 1 MHz because only 10 bits are programmable. When the PLL loop is locked, both inputs of the phase comparator are equal. This produces the following formula :

$$f_{\text{DIV}} = f_{\text{OSC}} / 8 / N = f_{\text{XTAL}} / 128 = f_{\text{REF}}$$

During the test mode operation, f_{DIV} and f_{REF} can be monitored on the Test output pin (pin 14).

Software information

The synthesizer is controlled via a two-wire I²C-bus receiver. For programming, the address byte (C8 in Hex format) has to be sent first. One or two data bytes are then used to set the 10 programmable bits of the dividing number N and the test bits (see Table 1).

Table 1 Data format.

| BYTE | MSB | | | | | | | | LSB | |
|-------------|-----|------|-------|-------|----------|----|----|----|-----|--|
| address C8 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | ACK | |
| data byte 1 | 0 | b11 | b10 | b9 | b8 | b7 | b6 | b5 | ACK | |
| data byte 2 | 1 | test | test1 | test2 | not used | b4 | b3 | b2 | ACK | |

Where: ACK is the acknowledge bit, and bits b2 to b11 are the 10 programmable bits of N. b1 = 0, b0 = 1 are set by internal hardware.

test, test1 and test2 are 3 bits used for test purpose (see Table 5).

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The bits b2 to b11 are programmable and represent the integer part of the frequency in MHz. b1 and b0 are fixed internally to 0 and 1 respectively to obtain the added 0.25 MHz, common to most TV channels (see Table 2).

Table 2 Structure of the dividing number N.

| BITS | b11 | b10 | b9 | b8 | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|------------------|-----|-----|-----|----|----|----|----|----|----|----|-----|------|
| frequency in MHz | 512 | 256 | 128 | 64 | 32 | 16 | 8 | 4 | 2 | 1 | 0.5 | 0.25 |

Note to Table 2

Bits b1 and b0 are not programmable

$$f_{osc} = 512 \times b11 + 256 \times b10 + \dots + b2 \times 1 + 0.25 \text{ (in MHz)}$$

Table 3 Dividing number N to program channel 21 = 471.25 MHz.

| BITS | b11 | b10 | b9 | b8 | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|------------------|-----|-----|-----|----|----|----|----|----|----|----|----|------|
| value | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 1 |
| frequency in MHz | 0 | 256 | 128 | 64 | 0 | 16 | 0 | 4 | 2 | 1 | 0 | 0.25 |

Note to Table 3

Bits b1 and b0 and their values 0 and 1 are not programmable

Table 4 Content of the data bytes to program channel 21 = 471.25 MHz.

| BYTE | MSB | | | | | | | | LSB | |
|-------------|-----|---|---|---|---|---|---|---|-----|-----|
| address C8 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | ACK |
| data byte 1 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | ACK |
| data byte 2 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | ACK |

It is possible to change only one data byte. The circuit will recognize which one is received with the value of MSB, 0 for data byte 1 and 1 for data byte 2. It is possible to change the frequency by 1 MHz using data byte 2. It is relatively simple to increment the channel frequency when its frequency width is 8 MHz by simply incrementing data byte 1.

Table 5 Test modes.

| TEST | TEST 1 | TEST 2 | OPERATIONAL MODE |
|------|--------|--------|-------------------------|
| 0 | 0 | X | normal operation |
| 0 | 1 | X | balance test |
| 1 | 0 | 0 | f_{REF} output |
| 1 | 0 | 1 | high impedance test |
| 1 | 1 | 0 | f_{DIV} output |
| 1 | 1 | 1 | phase detector disabled |

Where X = 0 or 1

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The high impedance mode may be used to control the RF tank circuit to test the oscillator with an external tuning voltage. In this mode, the phase detector is disabled and the external transistor of the tuning amplifier is switched OFF. The AMP output (pin 8) is LOW (<200 mV).

In the balance test mode, overmodulation is present in the RF mixer to allow the measurement of the parasitic residual modulation.

In the f_{REF} and f_{DIV} modes, the reference frequency (f_{REF}) in the phase comparator or the divided RF oscillator frequency (f_{DIV}) is available at the test pin.

In the phase detector disabled mode, it is possible to measure the leakage current at the input of the tuning amplifier (pin 9).

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

| SYMBOL | PARAMETER | MIN. | MAX. | UNIT |
|--------------------|--------------------------------------|------|----------|------|
| V_{DDA}, V_{DDD} | analog and digital supply voltage | -0.3 | +6 | V |
| V_{DDA}, V_{DDD} | analog and digital operating voltage | 4.5 | 5.5 | V |
| T_{sig} | storage temperature | -40 | +125 | °C |
| V_{max} | maximum voltage on all pins | -0.3 | V_{DD} | V |
| T_{amb} | operating ambient temperature | -10 | +80 | °C |

THERMAL RESISTANCE

| SYMBOL | PARAMETER | THERMAL RESISTANCE |
|--------------|--|--------------------|
| $R_{th j-a}$ | from junction to ambient in free air SOT163A SOT266A | 85 K/W 120 K/W |

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CHARACTERISTICS $V_{DDA} = V_{DDD} = 5$ V; $T_{amb} = 25$ °C; measured in circuit of Fig.5; unless otherwise specified.

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|--------------------------------|---|---|--------|------|--------|------|
| Supply | | | | | | |
| V_{DDA}, V_{DDD} | supply voltage | | 4.5 | 5.0 | 5.5 | V |
| I_{DDA}, I_{DDD} | supply current | | 41 | 51 | 61 | mA |
| Video characteristics | | | | | | |
| I_{19} | input current (AC) | $V_{19} = 2.6$ V | — | 11 | — | µA |
| $V_{19(p-p)}$ | input voltage level (peak-to-peak value) | | 0.7 | 1.0 | 1.4 | V |
| m | modulation depth | see Fig.3 | 76 | 83 | 89 | % |
| S/N video | signal-to-noise ratio | note 1 | 45 | 48 | — | dB |
| G_{diff} | differential gain | note 2 | — | 4 | 8 | % |
| Φ_{diff} | differential phase | note 2 | — | 4 | 8 | deg |
| Audio characteristics | | | | | | |
| Z_1 | input impedance | | 35 | 70 | 105 | kΩ |
| $V_{1(rms)}$ | maximum audio input voltage level (RMS value) | before pre-emphasis | — | 0.5 | — | V |
| Δm | modulation deviation | $f_{AUD} = 400$ Hz; $V_1 = 0.5$ V (RMS); before pre-emphasis filter | 20 | 25 | 30 | kHz |
| THD | total harmonic distortion | $\Delta f = 50$ kHz; $f_{AUD} = 6.3$ kHz | — | 1.8 | 3.0 | % |
| S/N audio | signal-to-noise ratio | CCIR filter 468 - 3; $f_{AUD} = 1$ kHz; $V_1 = 0.5$ V (RMS); before pre-emphasis filter | 42 | 52 | — | dB |
| SVR | sound carrier relative to picture carrier (sync RMS) | no audio signal; FM = 5.5 MHz; pin 19 connected to ground via 10 kΩ resistor | -18 | -14 | -10 | dB |
| Channel characteristics | | | | | | |
| f_{RF} | frequency range | related to tank circuit; see Fig.5 | 471.25 | — | 663.25 | MHz |
| f_{step} | frequency step | | — | 1 | — | MHz |
| $V_{15, 16}$ | output voltage level at pins 15 and 16; pin 19 connected to ground via 10 kΩ resistor; asymmetrical output loaded with 75 Ω | $f = 471.25$ MHz | 75 | 78 | 82 | dBµV |
| | | $f = 663.25$ MHz | 73 | 76 | 80 | dBµV |
| N_{SPO} | spurious noise outside channel | note 3 | — | -62 | — | dBc |
| N_{SPI} | spurious noise inside channel | | — | -50 | — | dBc |
| RF_{sh} | RF second harmonic level | asymmetrical output | — | -30 | — | dBc |
| SC_{th} | sound carrier third harmonic level | | — | -57 | — | dBc |
| IM | chrominance beat | note 4 | — | -62 | -58 | dBc |

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| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|--|---|---|------|-----------|--------|---------|
| Synthesizer characteristics | | | | | | |
| f_{XTAL} | crystal frequency | | — | 4 | — | MHz |
| f_{REF} | reference frequency | | — | 31.25 | — | kHz |
| f_{SYNT} | synthesizer frequency | | — | — | 900.25 | MHz |
| Charge pump output (pin 9) | | | | | | |
| I_9 | output current | | — | ± 100 | — | μA |
| V_9 | output voltage | in lock | 1.5 | — | 2.5 | V |
| I_{IL} | off-stage leakage current | $V_9 = 2$ V; test = 1; test1 = 1; test2 = 1 | — | — | 10 | $n A$ |
| Amplifier output (pin 8) | | | | | | |
| G | amplifier current gain | $V_9 = 2$ V; $I_8 = 10 \mu A$ | — | 4000 | — | |
| V_8 | output saturation voltage | $V_9 = 0$ V; test = 1; test1 = 0; test2 = 1 | — | 140 | 200 | mV |
| I²C-bus receiver characteristics | | | | | | |
| V_{IH} | HIGH level Input voltage SDA and SCL | | 3 | — | 5.5 | V |
| V_{IL} | LOW level Input voltage SDA and SCL | | 0 | — | 1.5 | V |
| I_{IH} | HIGH level Input current SDA and SCL | $V_{IH} = 5$ V; $V_{DDA}, V_{DDD} = 0$ to 5 V | — | — | +10 | μA |
| I_{IL} | LOW level Input current SDA and SCL | $V_{IL} = 0$ V; $V_{DDA}, V_{DDD} = 0$ to 5 V | -10 | — | — | μA |
| V_{OL} | LOW level output voltage SDA during acknowledge pulse | $I_{IL} = 3$ mA | — | — | 0.4 | V |

Notes

1. Signal-to-noise ratio: ratio between the CCIR 17 line bar amplitude and the RMS value of the noise on a black line (line 22 or 335). Measurement is unweighted.
2. The differential phase and gain are measured for G standard on CCIR 330 line.
3. Except for the harmonics of the RF oscillator frequency and the combinations between the RF oscillator and the sound oscillator frequency; $(f_{RF} + 2f_s, 2f_{RF} + f_s, \dots)$.
4. Chrominance beat: measured with a video signal of 1 V(p-p) with a chrominance carrier of 400 mV(p-p) filtered around 1.07 MHz with the filter illustrated in Fig.4. Following this method the chrominance beat can be seen on a spectrum analyser.

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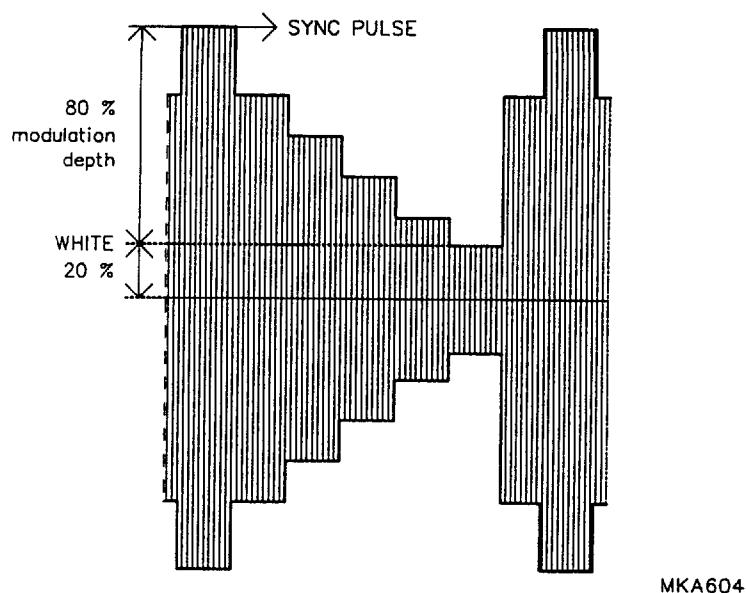


Fig.3 Modulation depth.

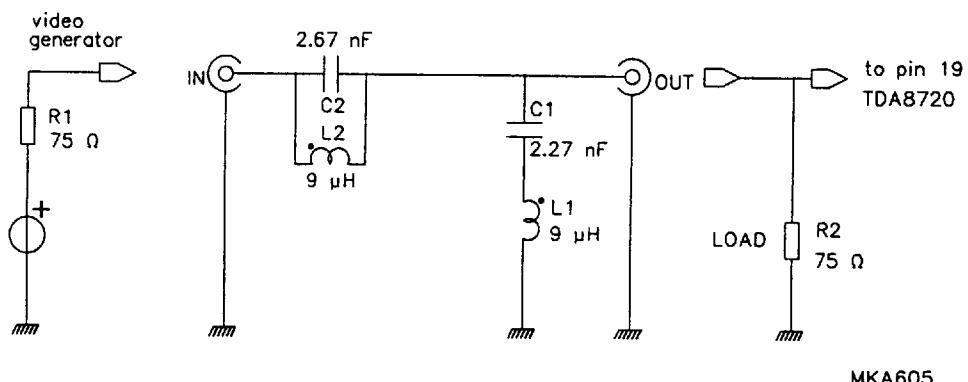


Fig.4 Schematic of video filter for chrominance-beat measurement.

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be completely safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

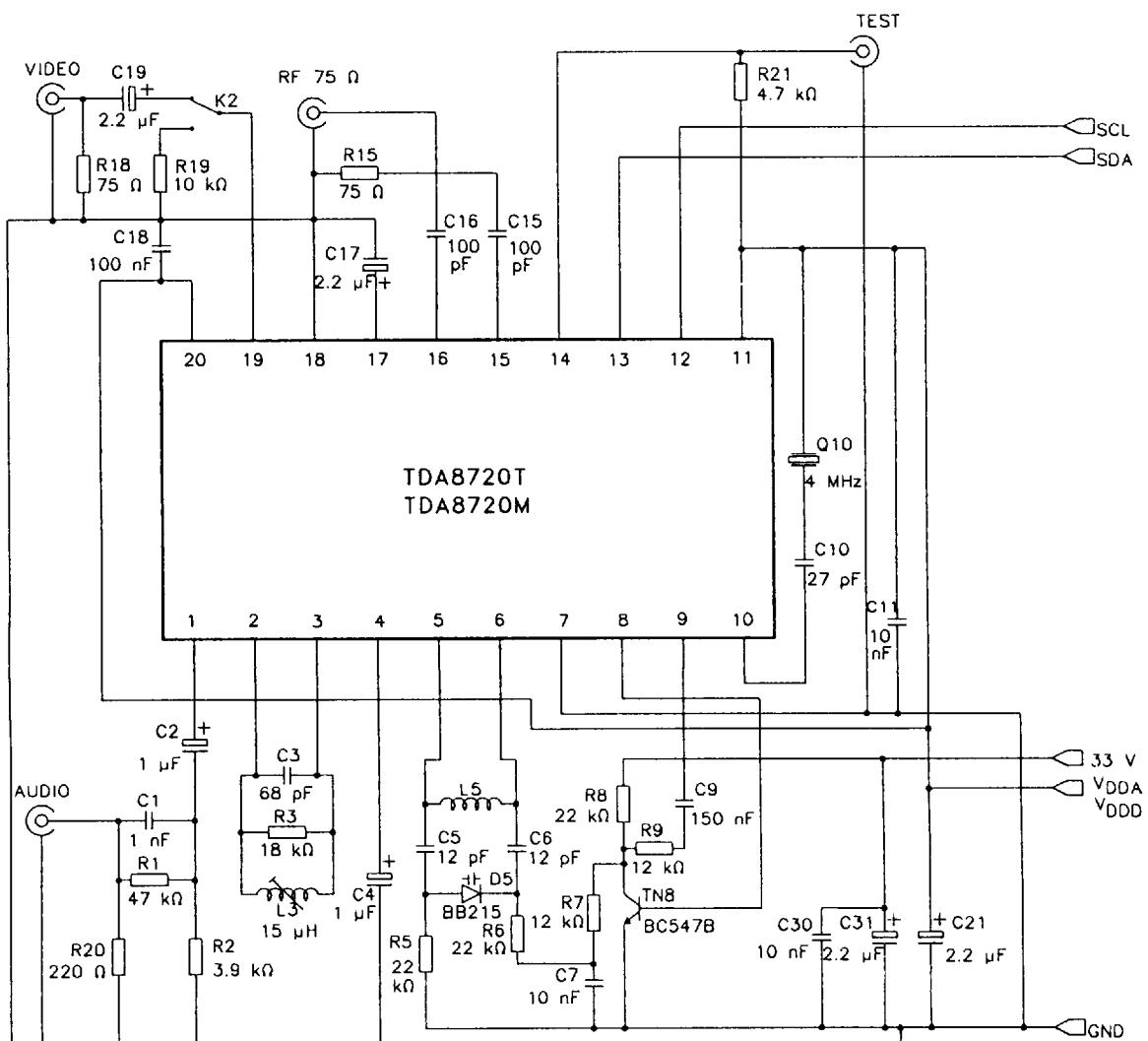
Every pin withstands the ESD test in accordance with MIL-STD-883C category B (2000 V).

Every pin withstands the ESD test in accordance with Philips Semiconductors Machine Model 0 Ω, 200 pF (200 V).

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APPLICATION INFORMATION



K2 : Switches the video input to input signal or to ground via a 10 kΩ resistor.

MKA606

L3 : To be adjusted for correct sound carrier (5.5 MHz for PAL G).

L5 : Air coil, 2.5 turns diameter 2 mm.

Fig.5 Reference measuring set-up for a G standard application.

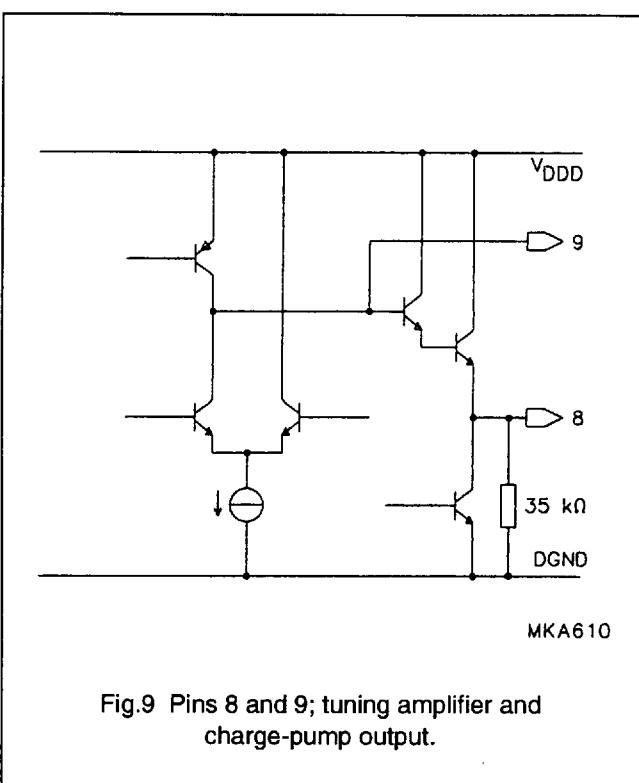
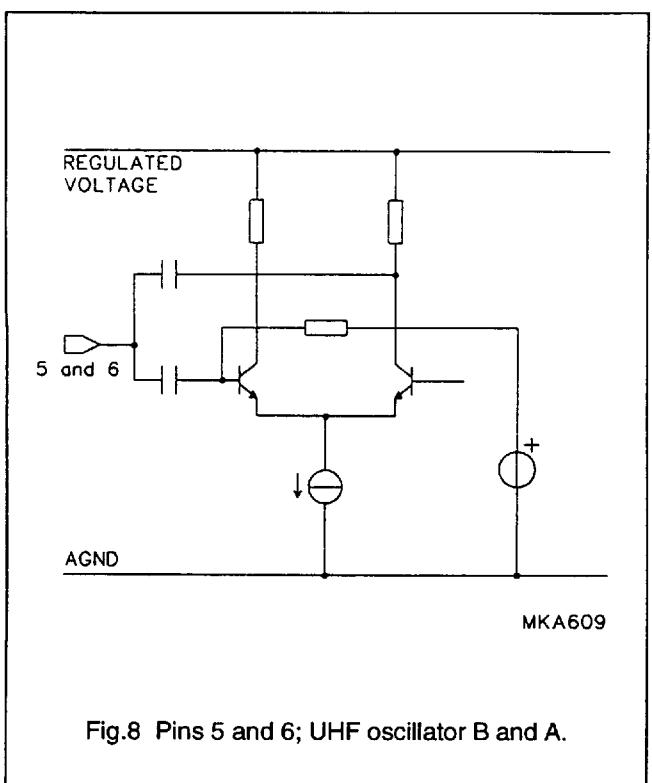
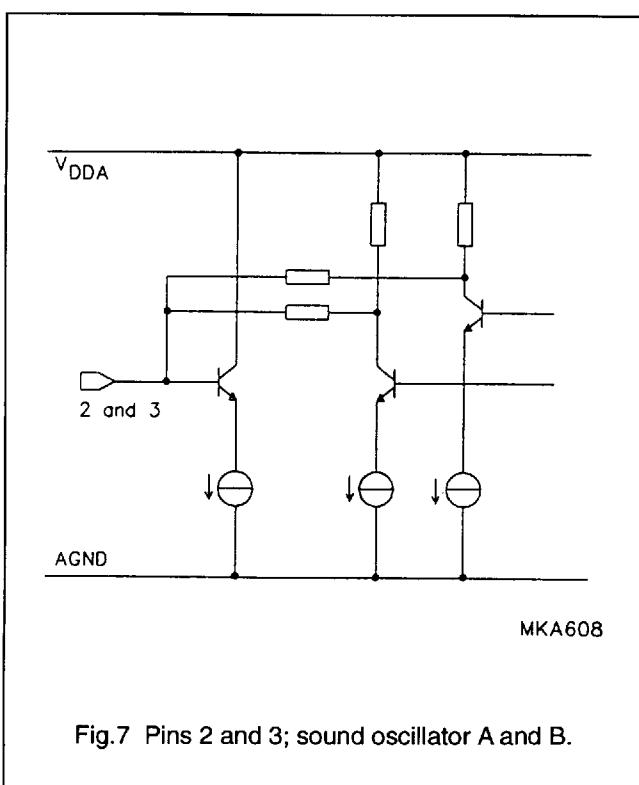
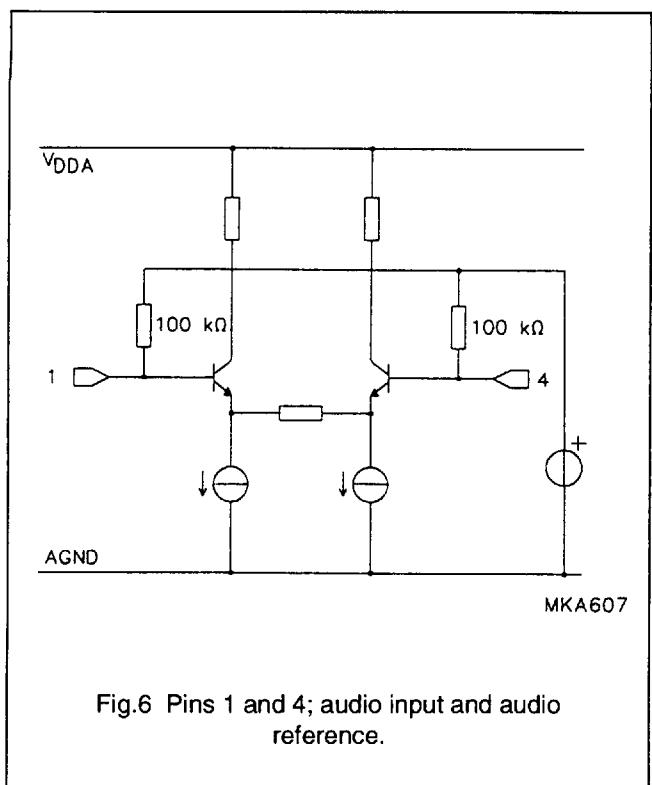
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INTERNAL PIN CONFIGURATION



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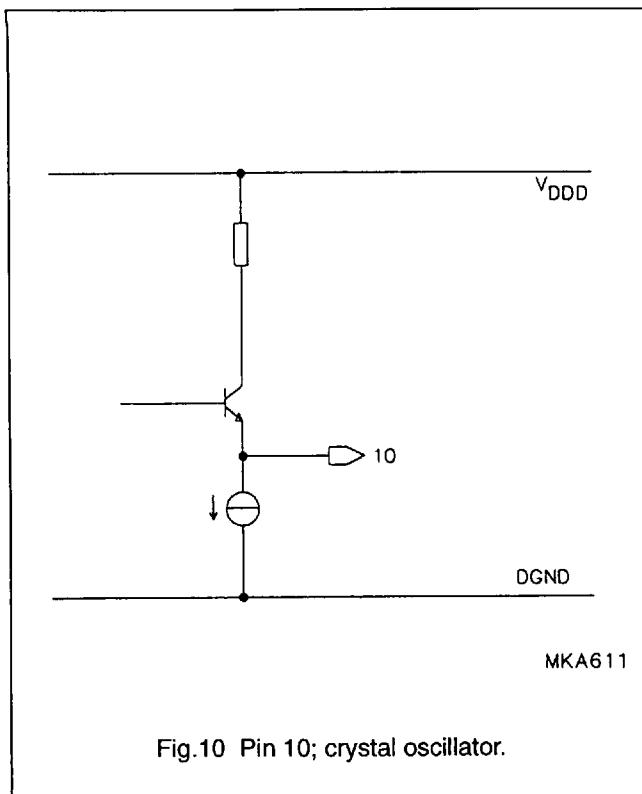
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Fig.10 Pin 10; crystal oscillator.

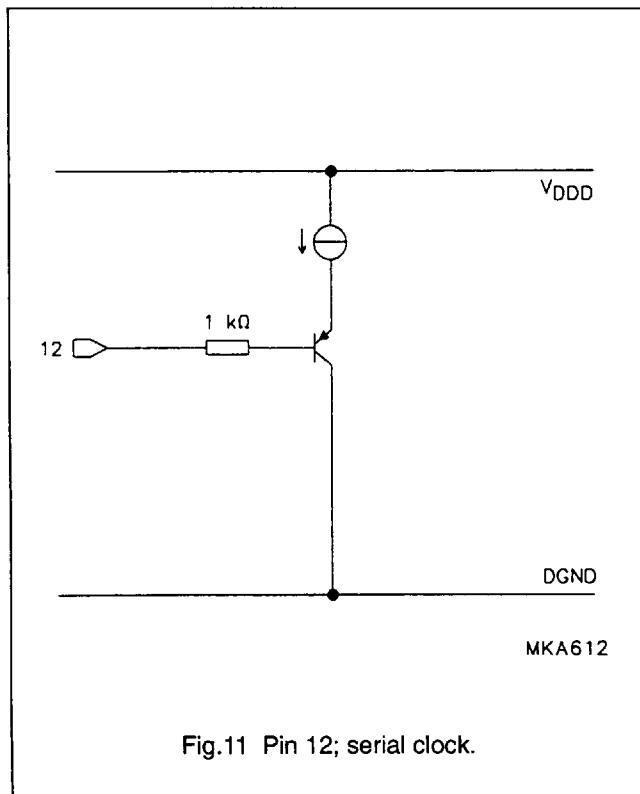


Fig.11 Pin 12; serial clock.

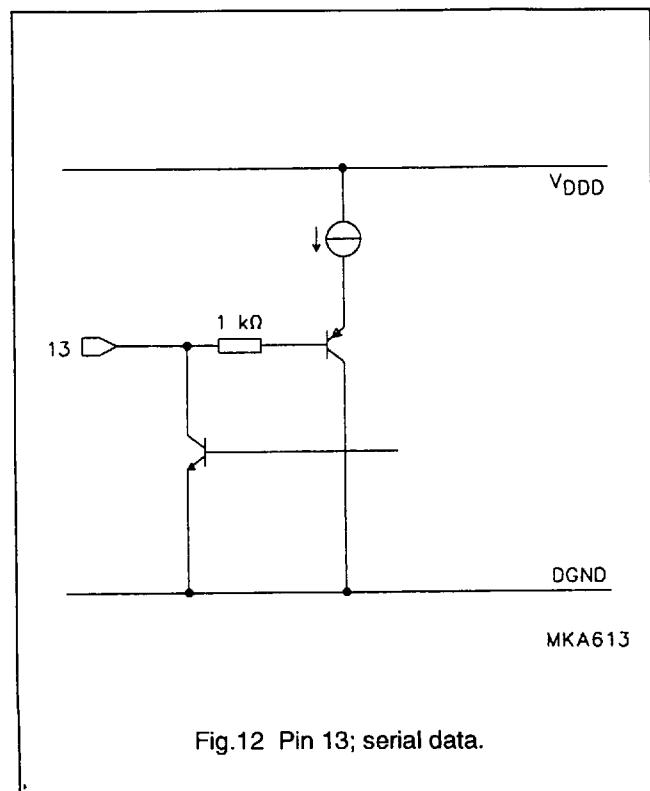


Fig.12 Pin 13; serial data.

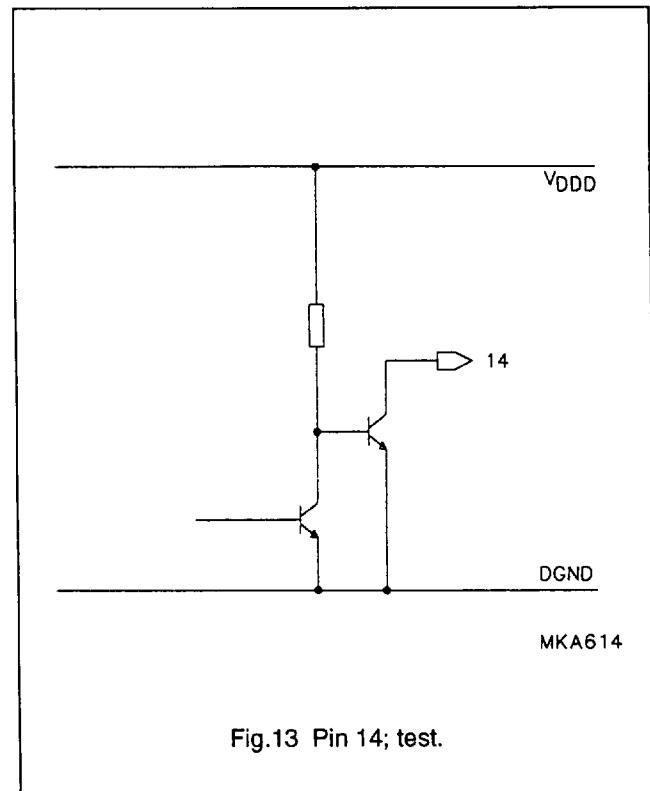


Fig.13 Pin 14; test.

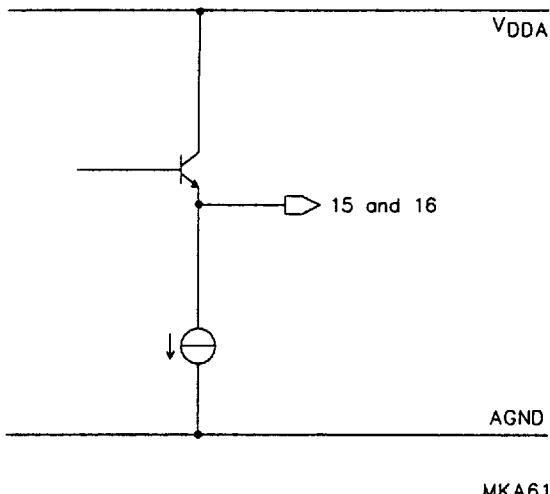
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Fig.14 Pins 15 and 16; RFA and RFB output.

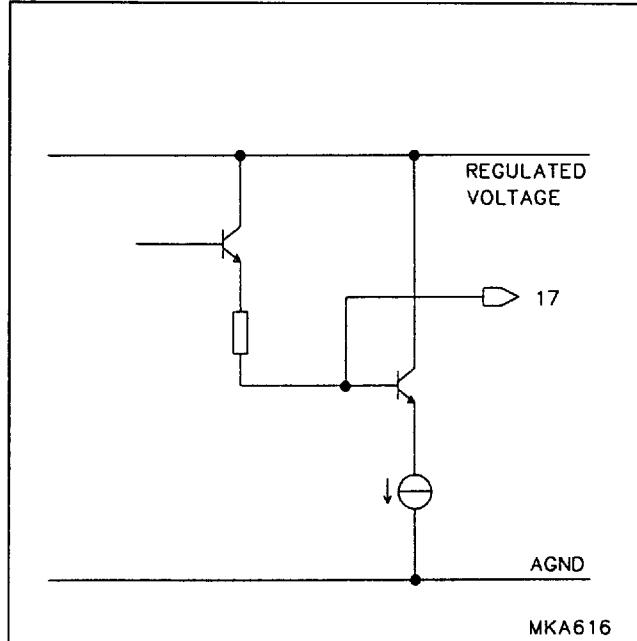


Fig.15 Pin 17; AGC

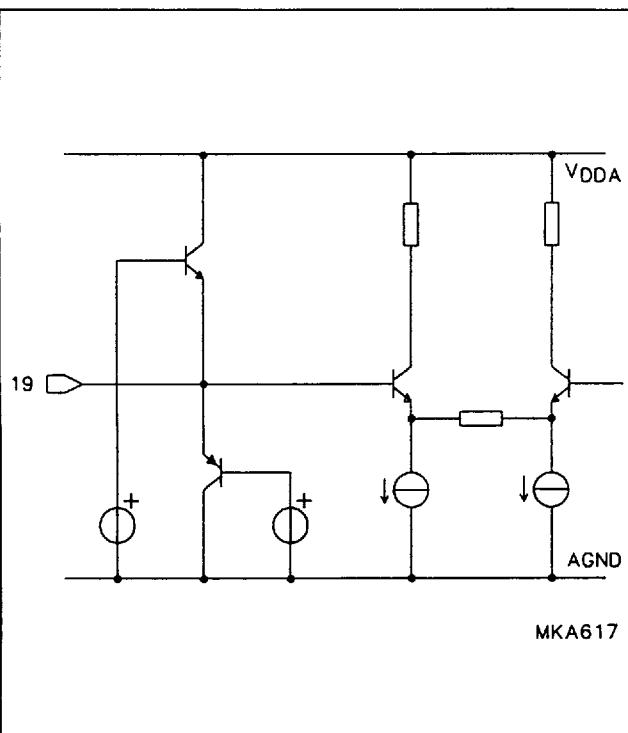
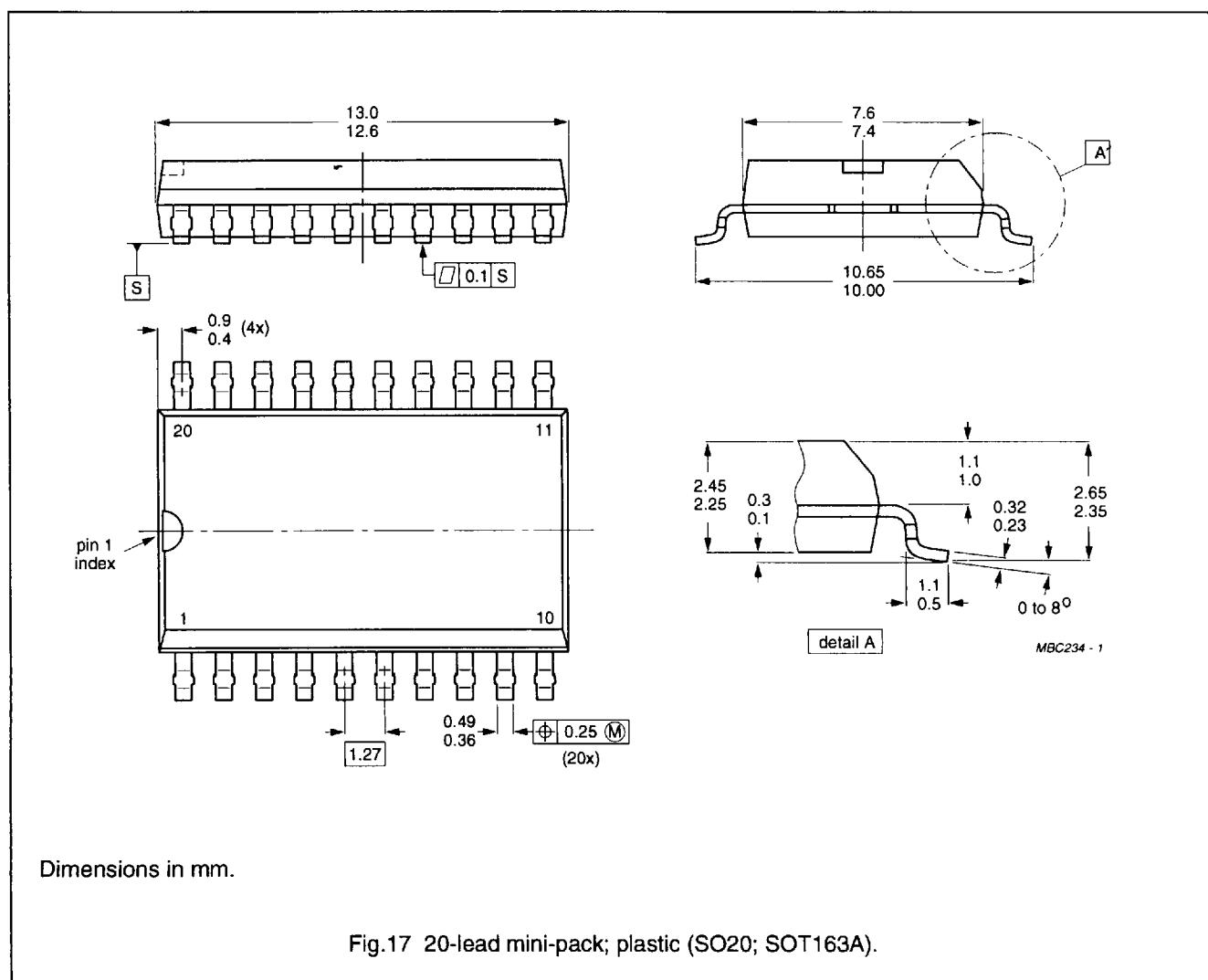


Fig.16 Pin 19; video input.

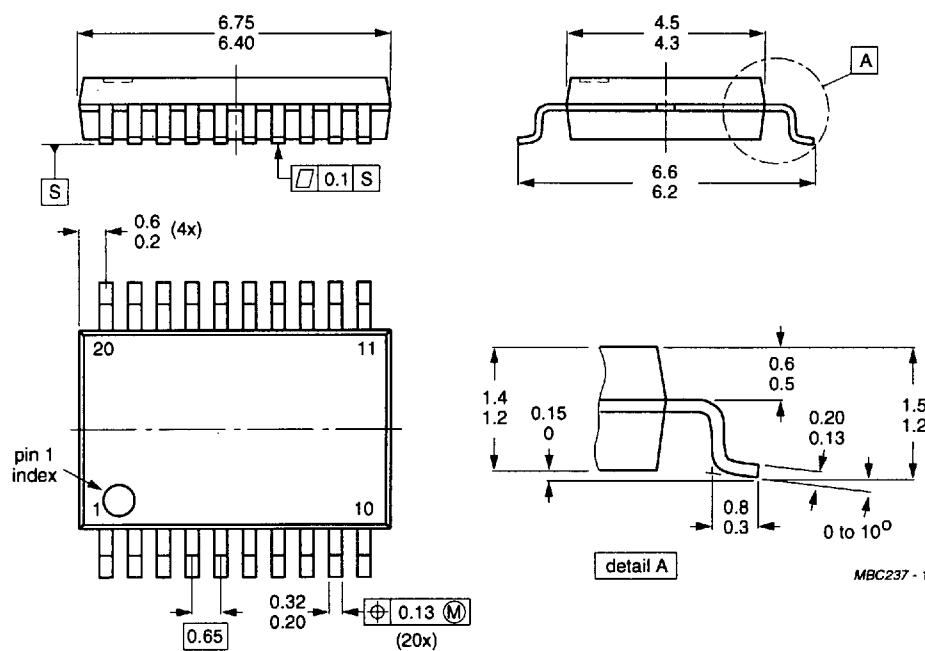
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**I²C-bus programmable modulator for
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Dimensions in mm.

Fig.18 20-lead shrink mini-pack; plastic (SSOP20; SOT266A).

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SOLDERING

Plastic mini-packs

By WAVE

During placement and before soldering, the component must be fixed with a droplet of adhesive. After curing the adhesive, the component can be soldered. The adhesive can be applied by screen printing, pin transfer or syringe dispensing.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder bath is 10 s, if allowed to cool to less than 150 °C within 6 s. Typical dwell time is 4 s at 250 °C.

A modified wave soldering technique is recommended using two solder waves (dual-wave), in which a turbulent wave with high upward pressure is followed by a smooth laminar wave. Using a mildly-activated flux eliminates the need for removal of corrosive residues in most applications.

By SOLDER PASTE REFLOW

Reflow soldering requires the solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the substrate by screen printing, stencilling or pressure-syringe dispensing before device placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt, infrared, and vapour-phase reflow. Dwell times vary between 50 and 300 s according to method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 min at 45 °C.

REPAIRING SOLDERED JOINTS (BY HAND-HELD SOLDERING IRON OR PULSE-HEATED SOLDER TOOL)

Fix the component by first soldering two, diagonally opposite, end pins. Apply the heating tool to the flat part of the pin only. Contact time must be limited to 10 s at up to 300 °C. When using proper tools, all other pins can be soldered in one operation within 2 to 5 s at between 270 and 320 °C. (Pulse-heated soldering is not recommended for SO packages.)

For pulse-heated solder tool (resistance) soldering of VSO packages, solder is applied to the substrate by dipping or by an extra thick tin/lead plating before package placement.

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| Data sheet status | |
|---|---|
| Objective specification | This data sheet contains target or goal specifications for product development. |
| Preliminary specification | This data sheet contains preliminary data; supplementary data may be published later. |
| Product specification | This data sheet contains final product specifications. |
| Limiting values | |
| Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability. | |
| Application information | |
| Where application information is given, it is advisory and does not form part of the specification. | |

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

PURCHASE OF PHILIPS I²C COMPONENTS

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.