



VND1NV04 VNN1NV04 / VNS1NV04

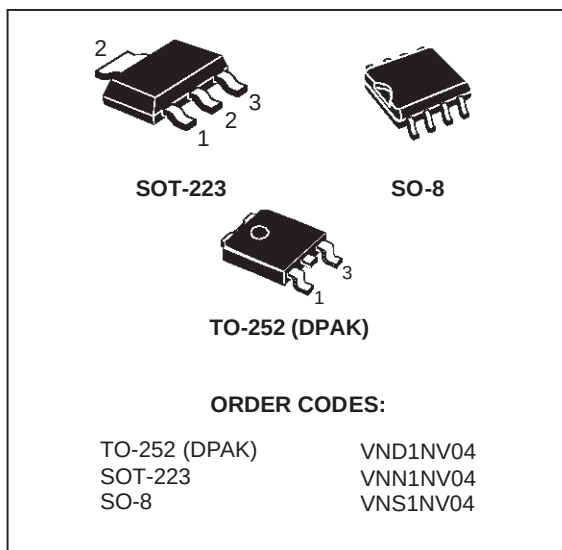
“OMNIFET II”:
FULLY AUTOPROTECTED POWER MOSFET

TYPE	$R_{DS(on)}$	I_{lim}	V_{clamp}
VND1NV04 VNN1NV04 VNS1NV04	250 mΩ	1.7 A	40 V

- LINEAR CURRENT LIMITATION
- THERMAL SHUT DOWN
- SHORT CIRCUIT PROTECTION
- INTEGRATED CLAMP
- LOW CURRENT DRAWN FROM INPUT PIN
- DIAGNOSTIC FEEDBACK THROUGH INPUT PIN
- ESD PROTECTION
- DIRECT ACCESS TO THE GATE OF THE POWER MOSFET (ANALOG DRIVING)
- COMPATIBLE WITH STANDARD POWER MOSFET

DESCRIPTION

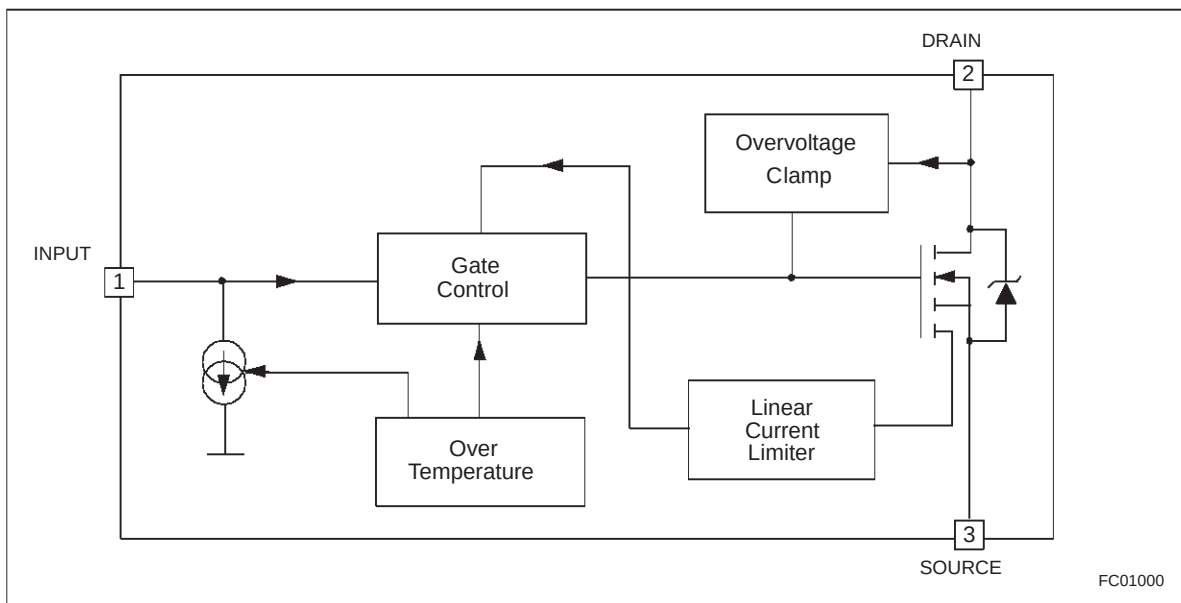
The VND1NV04, VNN1NV04, VNS1NV04 are monolithic devices designed in STMicroelectronics VIPower M0-3 Technology, intended for replacement of standard Power



MOSFETS from DC up to 50KHz applications. Built in thermal shutdown, linear current limitation and overvoltage clamp protect the chip in harsh environments.

Fault feedback can be detected by monitoring the voltage at the input pin.

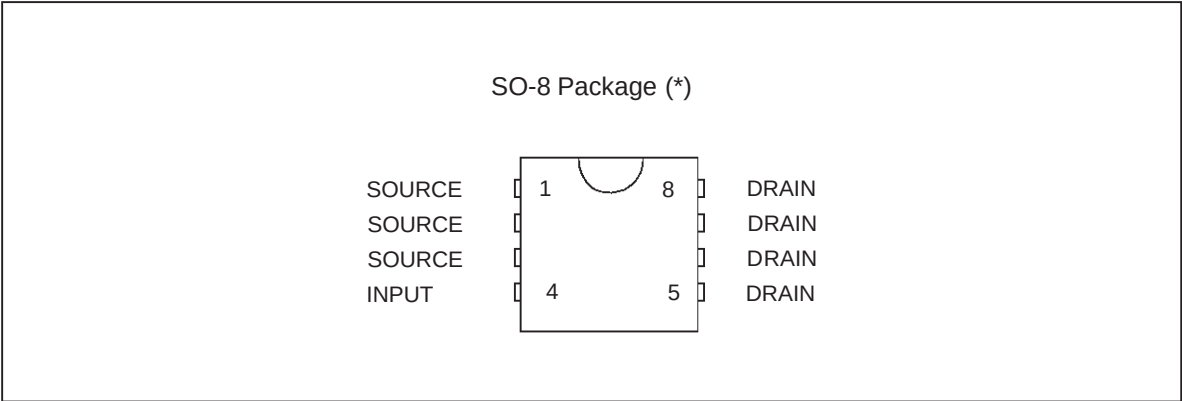
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATING

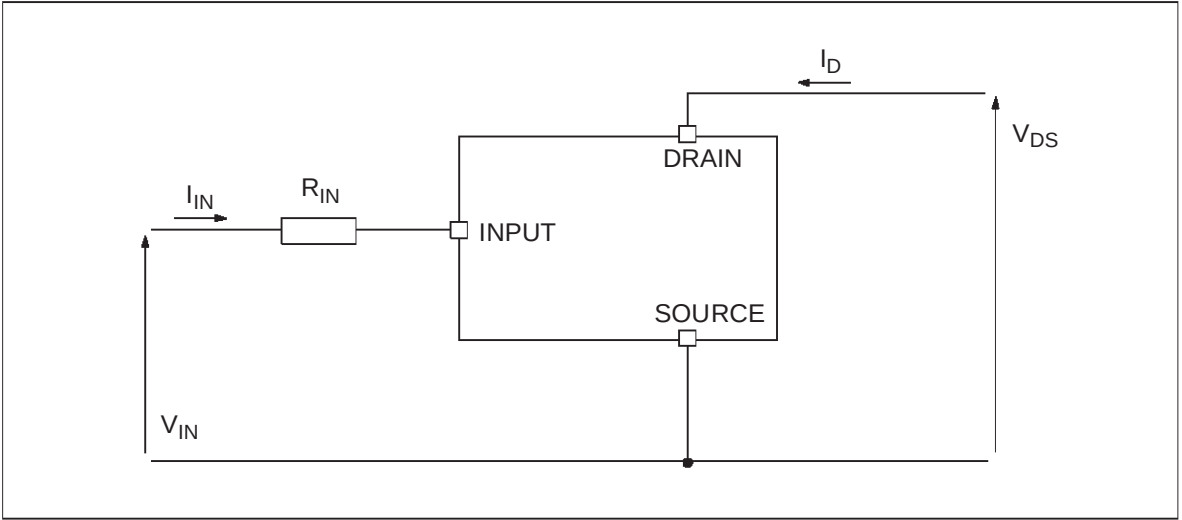
Symbol	Parameter	Value			Unit
		SOT-223	SO-8	DPAK	
V_{DS}	Drain-source Voltage ($V_{IN}=0V$)	Internally Clamped			V
V_{IN}	Input Voltage	Internally Clamped			V
I_{IN}	Input Current	+/-20			mA
$R_{IN\ MIN}$	Minimum Input Series Impedance	330			Ω
I_D	Drain Current	Internally Limited			A
I_R	Reverse DC Output Current	-3			A
V_{ESD1}	Electrostatic Discharge ($R=1.5K\Omega$, $C=100pF$)	4000			V
V_{ESD2}	Electrostatic Discharge on output pin only ($R=330\Omega$, $C=150pF$)	16500			V
P_{tot}	Total Dissipation at $T_c=25^{\circ}C$	7	8.3	35	W
T_j	Operating Junction Temperature	Internally limited			$^{\circ}C$
T_c	Case Operating Temperature	Internally limited			$^{\circ}C$
T_{stg}	Storage Temperature	-55 to 150			$^{\circ}C$

CONNECTION DIAGRAM (TOP VIEW)



(*) For the pins configuration related to SOT-223 and DPAK see outline at page 1.

CURRENT AND VOLTAGE CONVENTIONS



THERMAL DATA

Symbol	Parameter		Value			Unit
			SOT-223	SO-8	DPAK	
$R_{thj-case}$	Thermal Resistance Junction-case	MAX	18		3.5	°C/W
$R_{thj-lead}$	Thermal Resistance Junction-lead	MAX		15		°C/W
$R_{thj-amb}$	Thermal Resistance Junction-ambient	MAX	70 (*)	65(*)	54 (*)	°C/W

(*) When mounted on a standard single-sided FR4 board with 50mm² of Cu (at least 35 µm thick) connected to all DRAIN pins.

ELECTRICAL CHARACTERISTICS (-40°C < T_j < 150°C, unless otherwise specified)**OFF**

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{CLAMP}	Drain-source Clamp Voltage	$V_{IN}=0V$; $I_D=0.5A$	40	45	55	V
V_{CLTH}	Drain-source Clamp Threshold Voltage	$V_{IN}=0V$; $I_D=2mA$	36			V
V_{INTH}	Input Threshold Voltage	$V_{DS}=V_{IN}$; $I_D=1mA$	0.5		2.5	V
I_{ISS}	Supply Current from Input Pin	$V_{DS}=0V$; $V_{IN}=5V$		100	150	µA
V_{INCL}	Input-Source Clamp Voltage	$I_{IN}=1mA$ $I_{IN}=-1mA$	6 -1.0	6.8	8 -0.3	V
I_{DSS}	Zero Input Voltage Drain Current ($V_{IN}=0V$)	$V_{DS}=13V$; $V_{IN}=0V$; $T_j=25°C$ $V_{DS}=25V$; $V_{IN}=0V$			30 75	µA

ON

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$R_{DS(on)}$	Static Drain-source On Resistance	$V_{IN}=5V$; $I_D=0.5A$; $T_j=25°C$ $V_{IN}=5V$; $I_D=0.5A$			250 500	mΩ

VND1NV04 / VNN1NV04 / VNS1NV04

ELECTRICAL CHARACTERISTICS (continued) ($T_j=25^\circ\text{C}$, unless otherwise specified)

DYNAMIC

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$g_{fs}^{(**)}$	Forward Transconductance	$V_{DD}=13\text{V}$; $I_D=0.5\text{A}$		2		S
C_{OSS}	Output Capacitance	$V_{DS}=13\text{V}$; $f=1\text{MHz}$; $V_{IN}=0\text{V}$		90		pF

SWITCHING

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$t_{d(on)}$	Turn-on Delay Time	$V_{DD}=15\text{V}$; $I_D=0.5\text{A}$ $V_{gen}=5\text{V}$; $R_{gen}=R_{IN\ MIN}=330\Omega$ (see figure 1)		70	200	ns
t_r	Rise Time			170	500	ns
$t_{d(off)}$	Turn-off Delay Time			350	1000	ns
t_f	Fall Time			200	600	ns
$t_{d(on)}$	Turn-on Delay Time	$V_{DD}=15\text{V}$; $I_D=0.5\text{A}$ $V_{gen}=5\text{V}$; $R_{gen}=2.2\text{K}\Omega$ (see figure 1)		0.25	1.0	μs
t_r	Rise Time			1.3	4.0	μs
$t_{d(off)}$	Turn-off Delay Time			1.8	5.5	μs
t_f	Fall Time			1.2	4.0	μs
$(di/dt)_{on}$	Turn-on Current Slope	$V_{DD}=15\text{V}$; $I_D=1.5\text{A}$ $V_{gen}=5\text{V}$; $R_{gen}=R_{IN\ MIN}=330\Omega$		5.0		A/ μs
Q_i	Total Input Charge	$V_{DD}=12\text{V}$; $I_D=0.5\text{A}$; $V_{IN}=5\text{V}$ $I_{gen}=2.13\text{mA}$ (see figure 5)		5.0		nC

SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$V_{SD}^{(*)}$	Forward On Voltage	$I_{SD}=0.5\text{A}$; $V_{IN}=0\text{V}$		0.8		V
t_{rr}	Reverse Recovery Time	$I_{SD}=0.5\text{A}$; $di/dt=6\text{A}/\mu\text{s}$		205		ns
Q_{rr}	Reverse Recovery Charge	$V_{DD}=30\text{V}$; $L=200\mu\text{H}$		100		μC
I_{RRM}	Reverse Recovery Current	(see test circuit, figure 2)		0.75		A

PROTECTIONS ($-40^\circ\text{C} < T_j < 150^\circ\text{C}$, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I_{lim}	Drain Current Limit	$V_{IN}=5\text{V}$; $V_{DS}=13\text{V}$	1.7		3.5	A
t_{dlim}	Step Response Current Limit	$V_{IN}=5\text{V}$; $V_{DS}=13\text{V}$		2.0		μs
T_{jsh}	Overtemperature Shutdown		150	175		$^\circ\text{C}$
T_{jrs}	Overtemperature Reset		135			$^\circ\text{C}$
I_{gf}	Fault Sink Current	$V_{IN}=5\text{V}$; $V_{DS}=13\text{V}$; $T_j=T_{jsh}$	10	15	20	mA
E_{as}	Single Pulse Avalanche Energy	Starting $T_j=25^\circ\text{C}$; $V_{DD}=24\text{V}$ $V_{IN}=5\text{V}$; $R_{gen}=R_{IN\ MIN}=330\Omega$; $L=50\text{mH}$ (see figures 3 & 4)	55			mJ

(**) Pulsed: Pulse duration = 300 μs , duty cycle 1.5%

PROTECTION FEATURES

During normal operation, the INPUT pin is electrically connected to the gate of the internal power MOSFET through a low impedance path.

The device then behaves like a standard power MOSFET and can be used as a switch from DC up to 50KHz. The only difference from the user's standpoint is that a small DC current I_{SS} (typ. 100 μ A) flows into the INPUT pin in order to supply the internal circuitry.

The device integrates:

- OVERVOLTAGE CLAMP PROTECTION:

internally set at 45V, along with the rugged avalanche characteristics of the Power MOSFET stage give this device unrivalled ruggedness and energy handling capability. This feature is mainly important when driving inductive loads.

- LINEAR CURRENT LIMITER CIRCUIT:

limits the drain current I_D to I_{lim} whatever the INPUT pin voltages. When the current limiter is active, the device operates in the linear region, so power dissipation may exceed the capability of the heatsink. Both case and junction temperatures increase, and if this phase lasts long enough, junction temperature may reach the overtemperature threshold T_{jsh} .

- OVERTEMPERATURE AND SHORT CIRCUIT PROTECTION:

these are based on sensing the chip temperature and are not dependent on the input voltage. The location of the sensing element on the chip in the power stage area ensures fast, accurate detection of the junction temperature. Overtemperature cutout occurs in the range 150 to 190 °C, a typical value being 170 °C. The device is automatically restarted when the chip temperature falls of about 15°C below shut-down temperature.

- STATUS FEEDBACK:

in the case of an overtemperature fault condition ($T_j > T_{jsh}$), the device tries to sink a diagnostic current I_{gf} through the INPUT pin in order to indicate fault condition. If driven from a low impedance source, this current may be used in order to warn the control circuit of a device shutdown. If the drive impedance is high enough so that the INPUT pin driver is not able to supply the current I_{gf} , the INPUT pin will fall to 0V. **This will not however affect the device operation: no requirement is put on the current capability of the INPUT pin driver except to be able to supply the normal operation drive current I_{SS} .**

Additional features of this device are ESD protection according to the Human Body model and the ability to be driven from a TTL Logic circuit.

Figure 1: Switching Time Test Circuit for Resistive Load

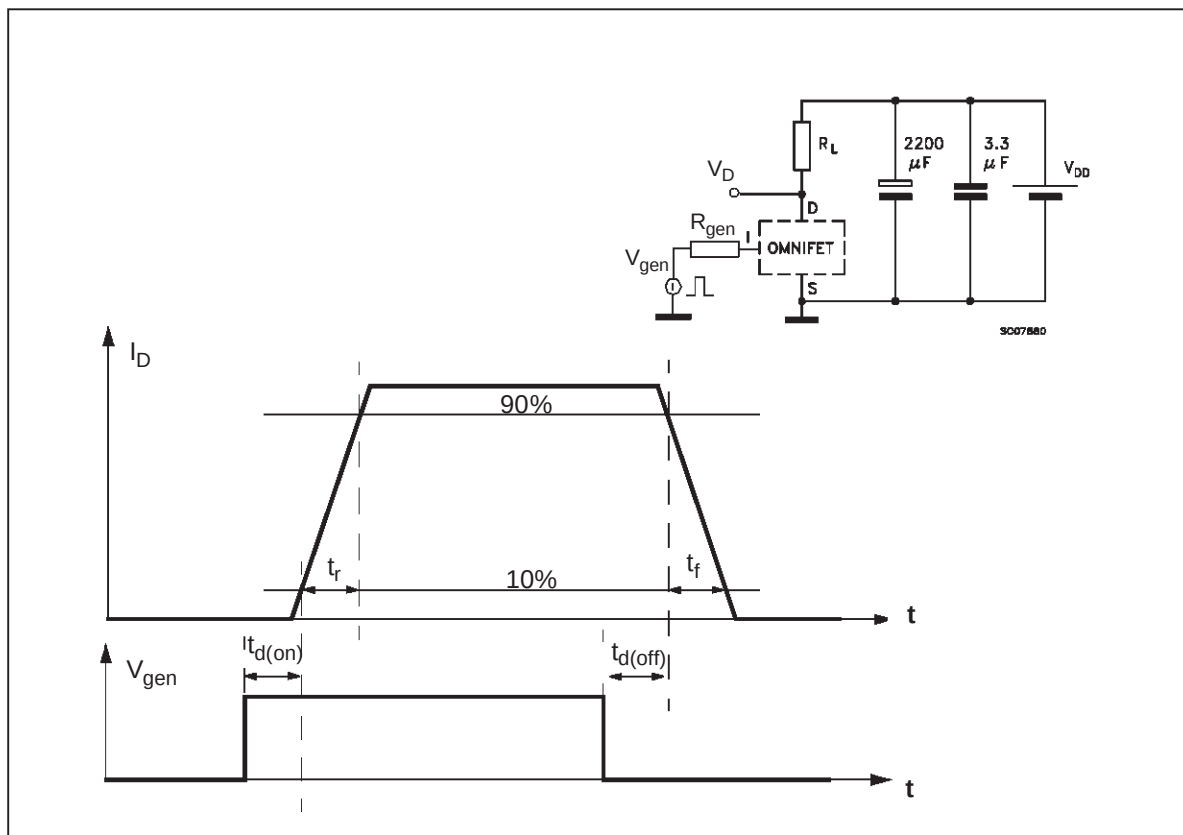


Figure 2: Test Circuit for Diode Recovery Times

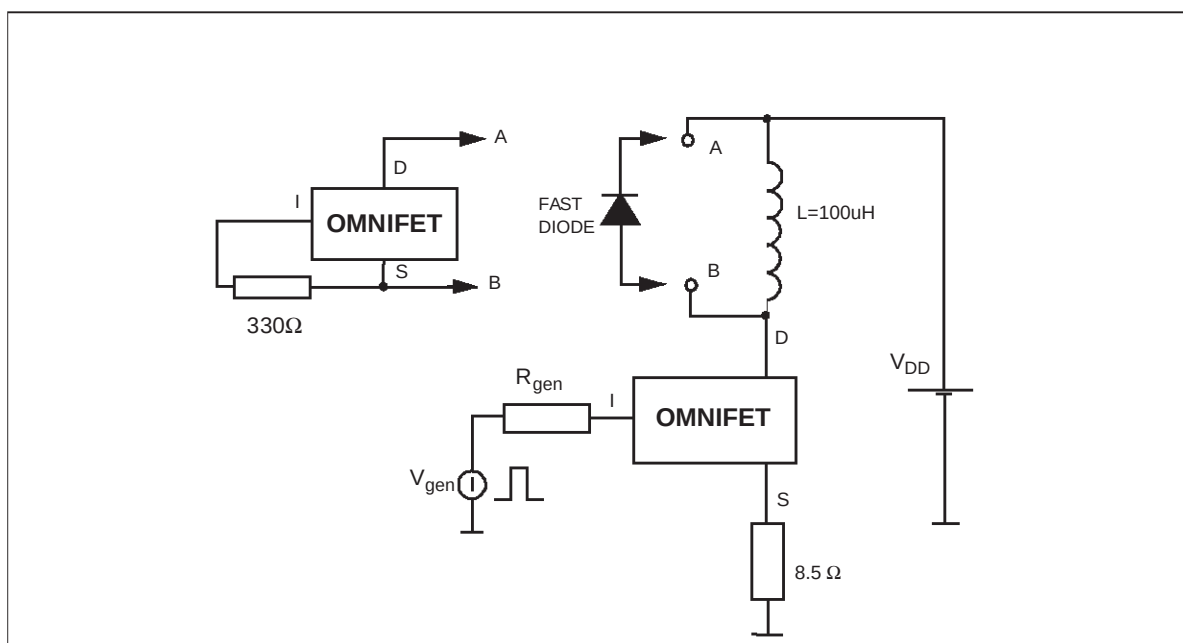
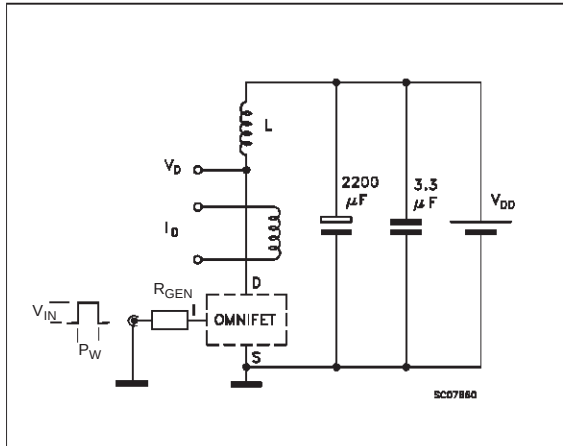
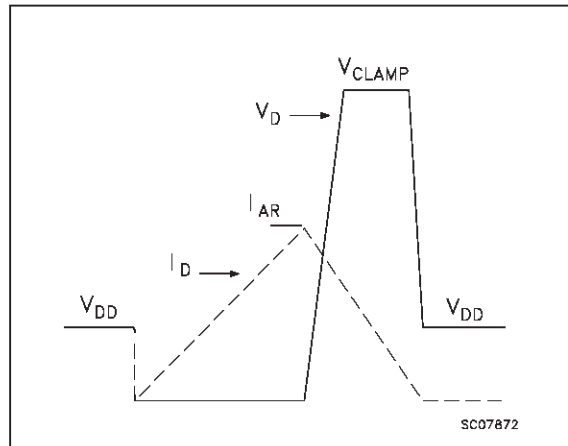
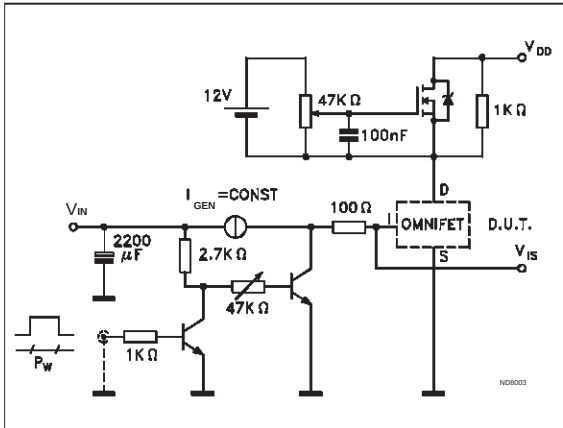
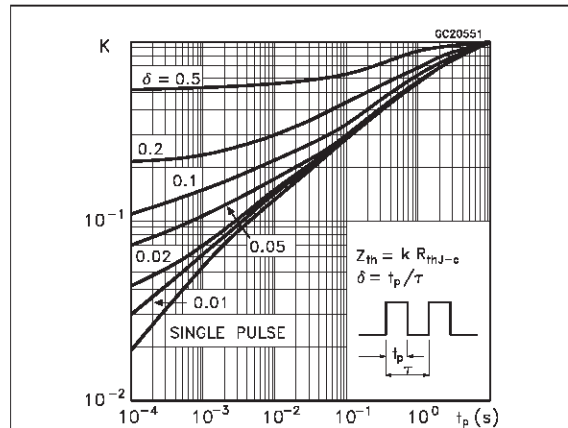
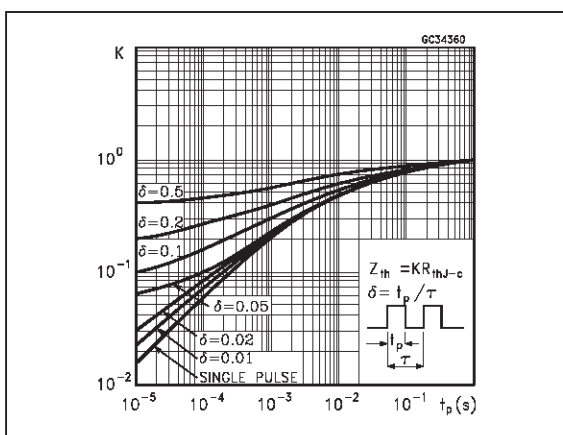
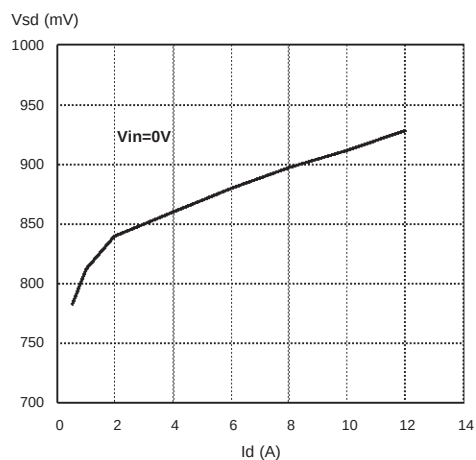
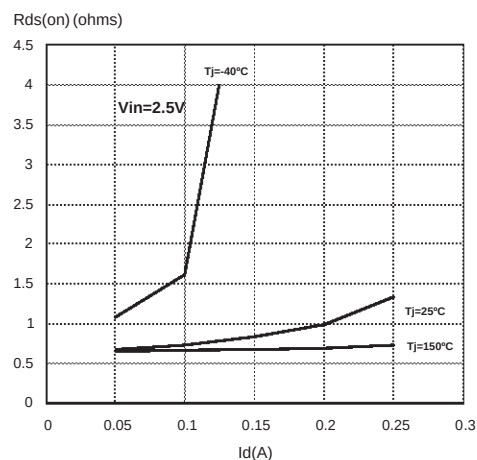


Figure 3: Unclamped Inductive Load Test Circuits

Figure 4: Unclamped Inductive Waveforms

Figure 5: Input Charge Test Circuit

Figure 6: Thermal Impedance for SOT-223

Figure 7: Thermal Impedance for DPAK/IPAK


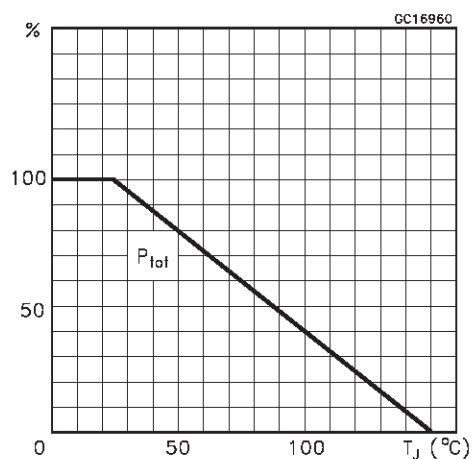
Source-Drain Diode Forward Characteristics



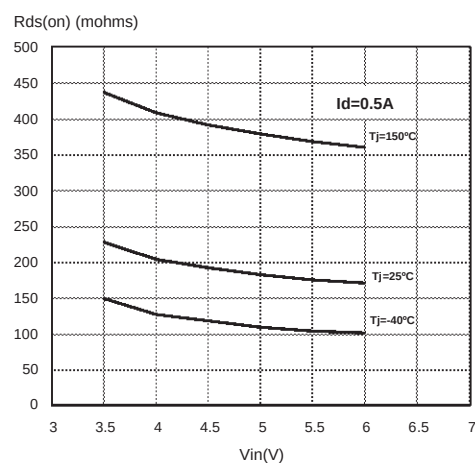
Static Drain Source On Resistance



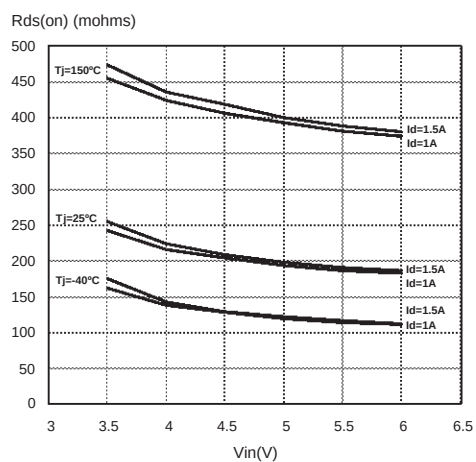
Derating Curve



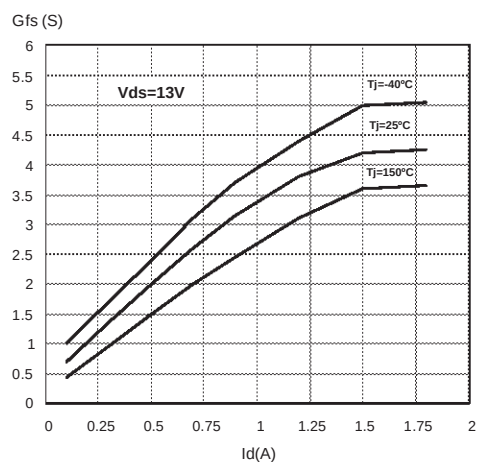
Static Drain-Source On resistance Vs. Input Voltage



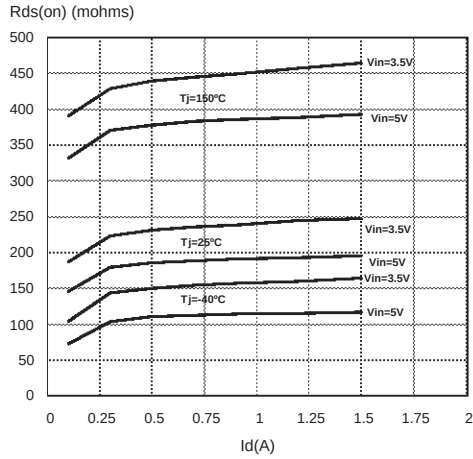
Static Drain-Source On resistance Vs. Input Voltage



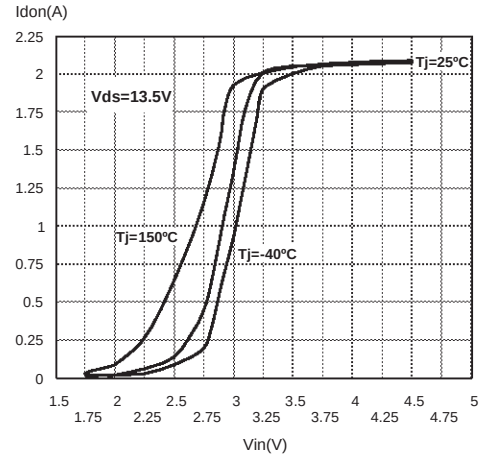
Transconductance



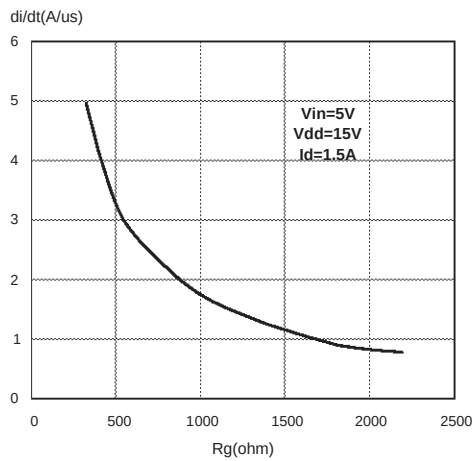
Static Drain-Source On Resistance Vs. Id



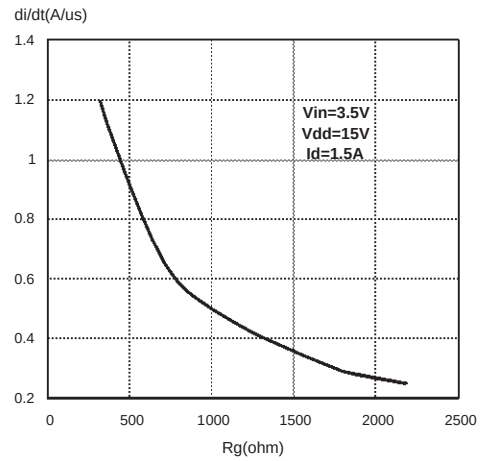
Transfer Characteristics



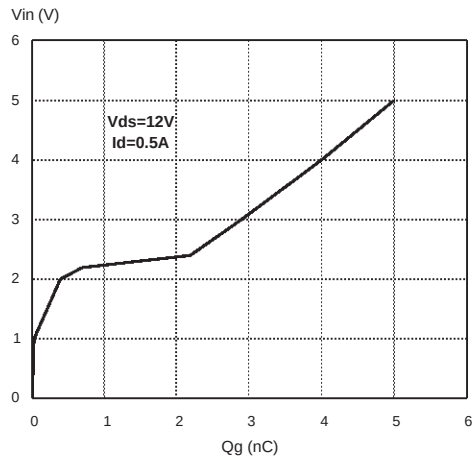
Turn On Current Slope



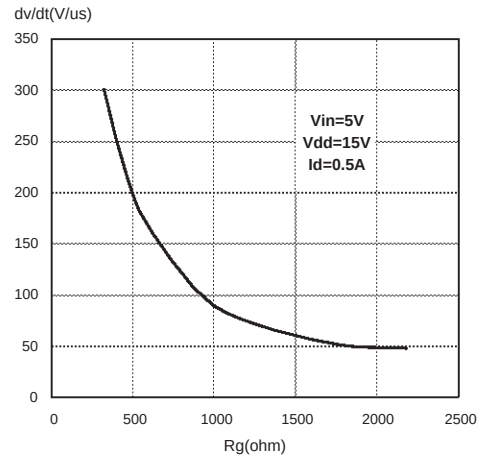
Turn On Current Slope



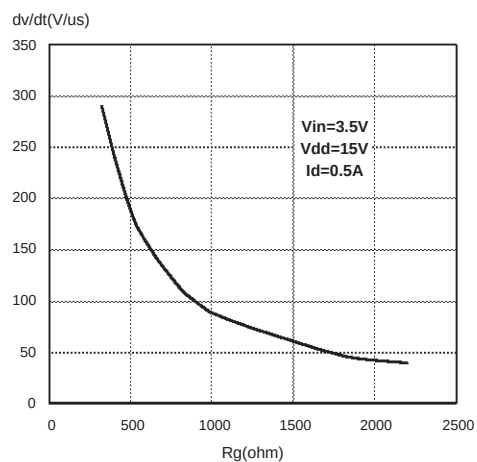
Input Voltage Vs. Input Charge



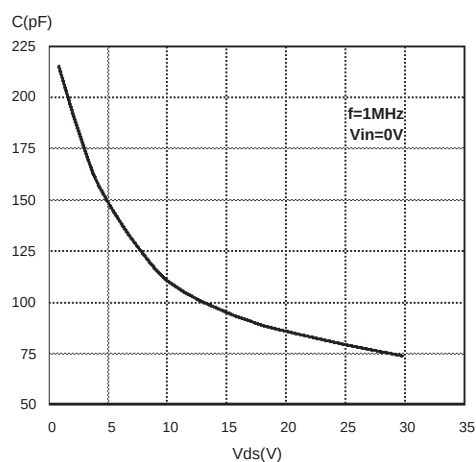
Turn off drain source voltage slope



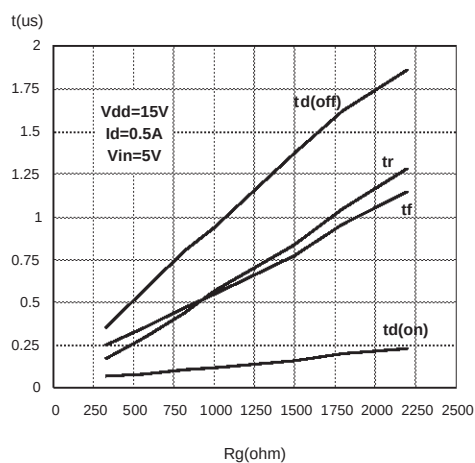
Turn Off Drain-Source Voltage Slope



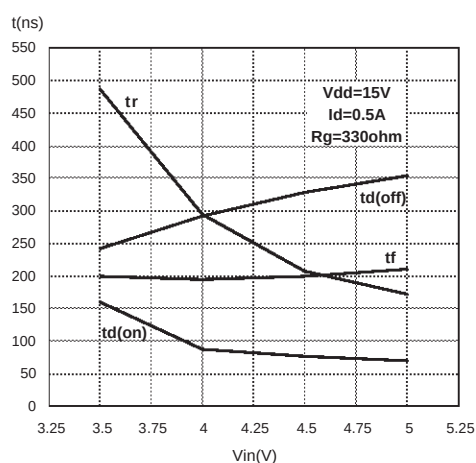
Capacitance Variations



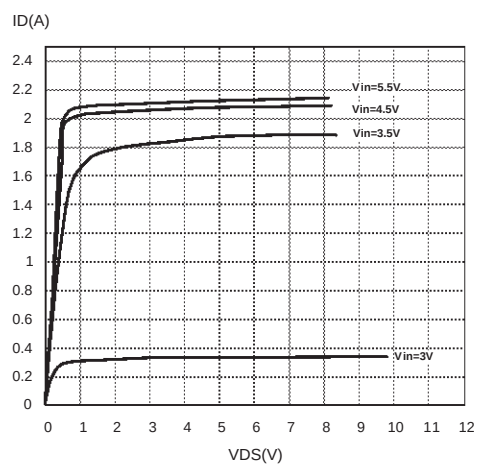
Switching Time Resistive Load



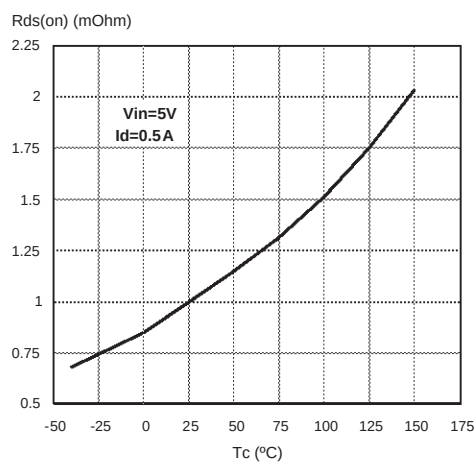
Switching Time Resistive Load



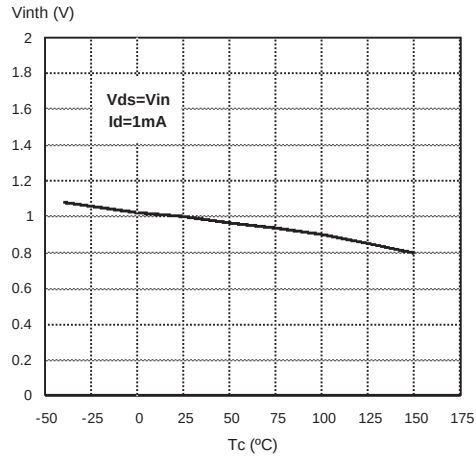
Output Characteristics



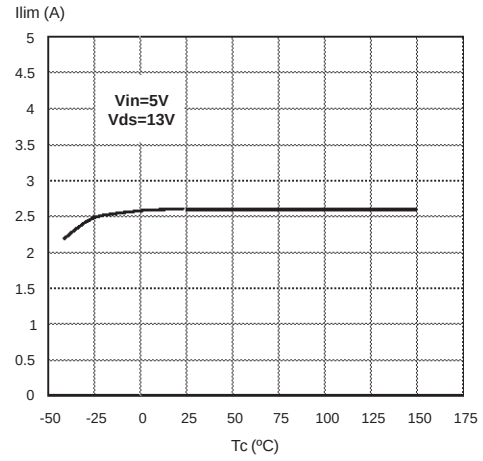
Normalized On Resistance Vs. Temperature



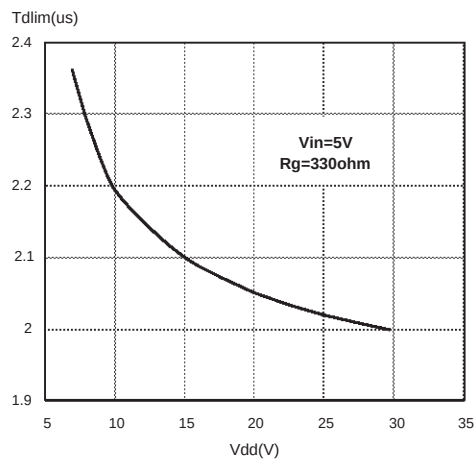
Normalized Input Threshold Voltage Vs. Temperature



Normalized Current Limit Vs. Junction Temperature

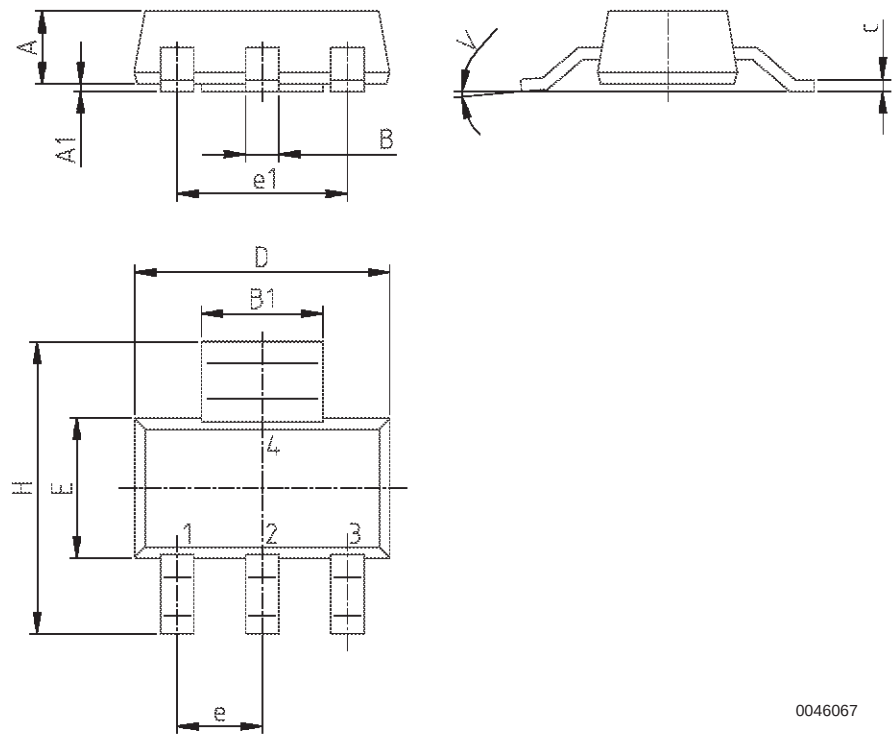


Step Response Current Limit



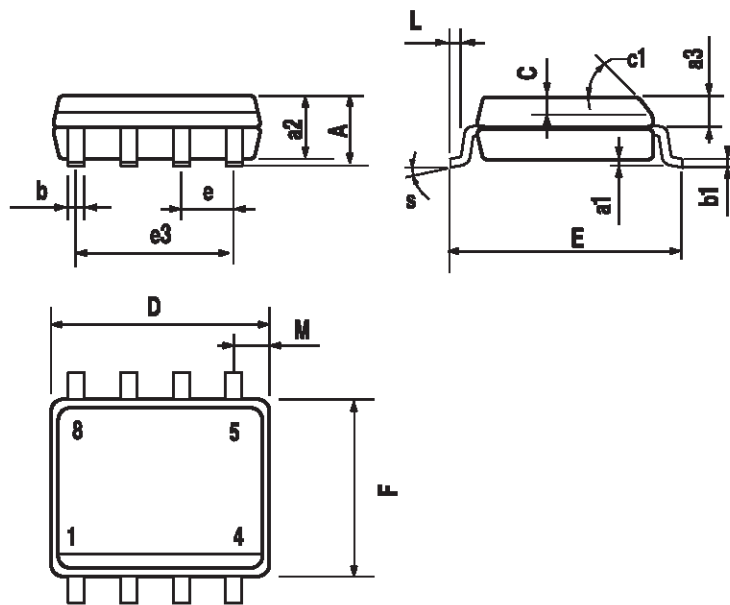
SOT-223 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.8			0.071
B	0.6	0.7	0.85	0.024	0.027	0.033
B1	2.9	3	3.15	0.114	0.118	0.124
c	0.24	0.26	0.35	0.009	0.01	0.014
D	6.3	6.5	6.7	0.248	0.256	0.264
e		2.3			0.09	
e1		4.6			0.181	
E	3.3	3.5	3.7	0.13	0.138	0.146
H	6.7	7	7.3	0.264	0.276	0.287
V	10 (max)					
A1	0.02		0.1	0.0008		0.004



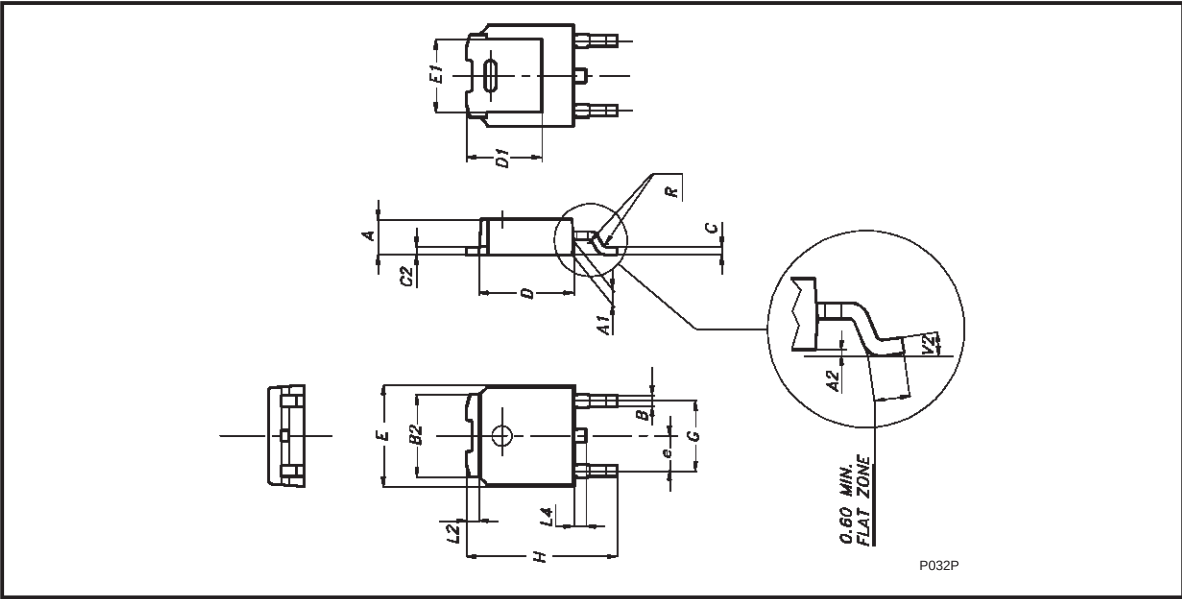
SO-8 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.25	0.003		0.009
a2			1.65			0.064
a3	0.65		0.85	0.025		0.033
b	0.35		0.48	0.013		0.018
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.019
c1	45 (typ.)					
D	4.8		5.0	0.188		0.196
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.14		0.157
L	0.4		1.27	0.015		0.050
M			0.6			0.023
F	8 (max.)					

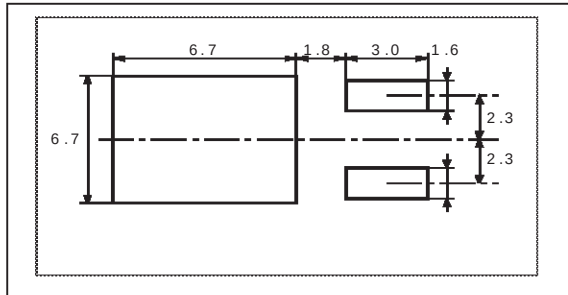


TO-252 (DPAK) MECHANICAL DATA

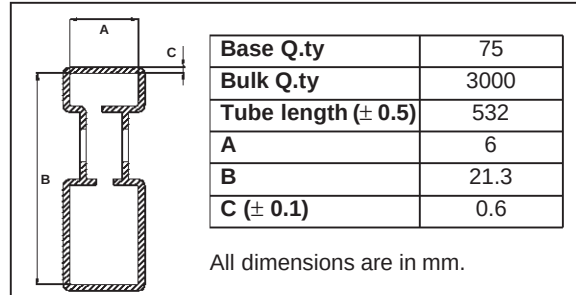
DIM.	mm.		
	MIN.	TYP	MAX.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
B	0.64		0.90
B2	5.20		5.40
C	0.45		0.60
C2	0.48		0.60
D	6.00		6.20
D1		5.1	
E	6.40		6.60
E1		4.7	
e		2.28	
G	4.40		4.60
H	9.35		10.10
L2		0.8	
L4	0.60		1.00
R		0.2	
V2	0°	8°	
Package Weight	Gr. 0.29		



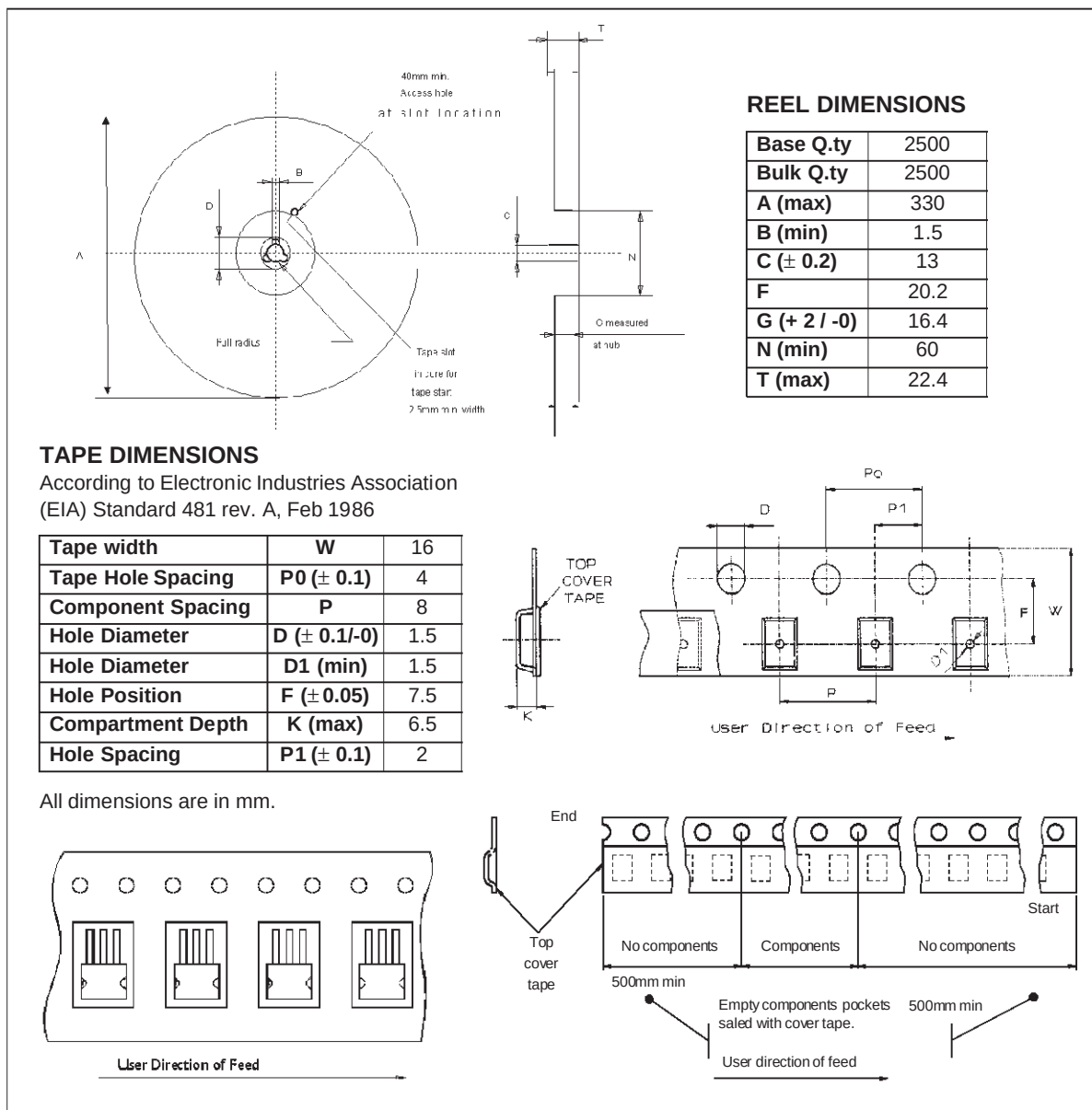
DPAK FOOTPRINT



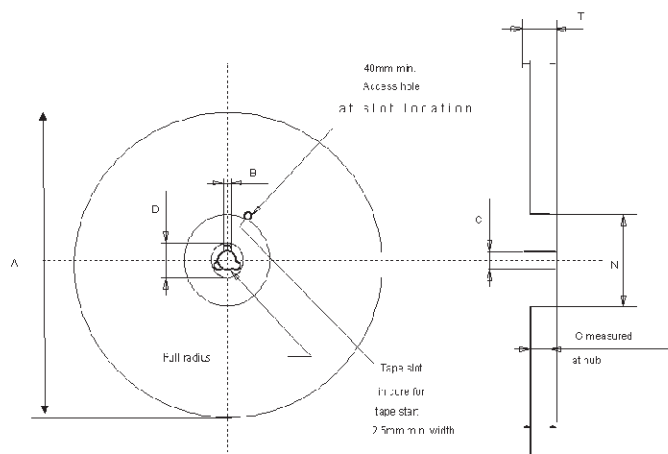
TUBE SHIPMENT (no suffix)



TAPE AND REEL SHIPMENT (suffix "13TR")



SOT-223 TAPE AND REEL SHIPMENT (suffix "13TR")



REEL DIMENSIONS

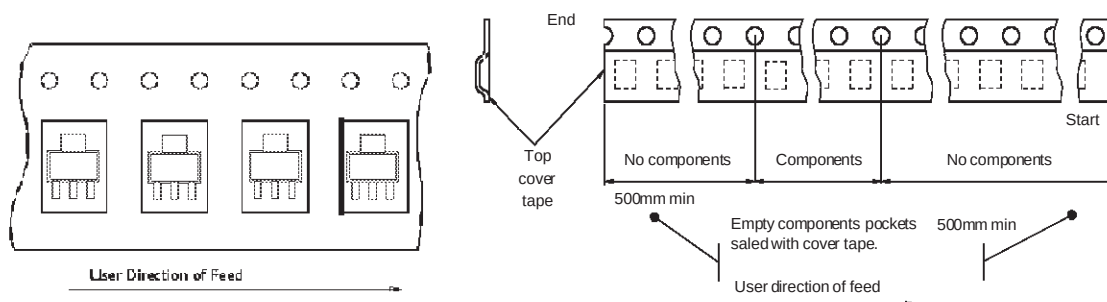
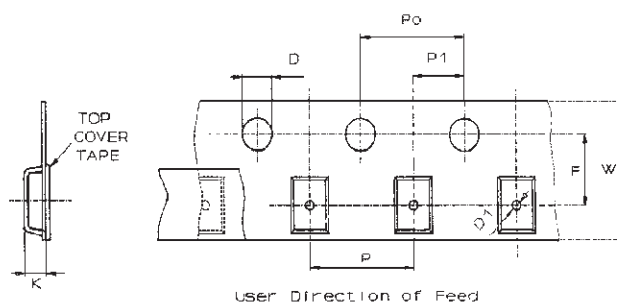
Base Q.ty	1000
Bulk Q.ty	1000
A (max)	330
B (min)	1.5
C (± 0.2)	13
F	20.2
G (+ 2 / -0)	12.4
N (min)	60
T (max)	18.4

TAPE DIMENSIONS

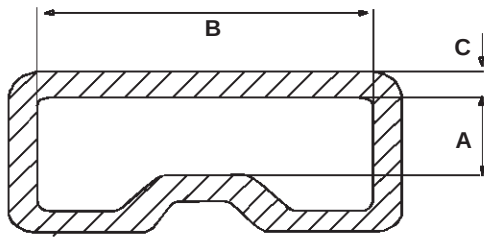
According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb. 1986

Tape width	W	12
Tape Hole Spacing	P0 (± 0.1)	4
Component Spacing	P	8
Hole Diameter	D ($\pm 0.1/-0$)	1.5
Hole Diameter	D1 (min)	1.5
Hole Position	F (± 0.05)	5.5
Compartment Depth	K (max)	4.5
Hole Spacing	P1 (± 0.1)	2

All dimensions are in mm.



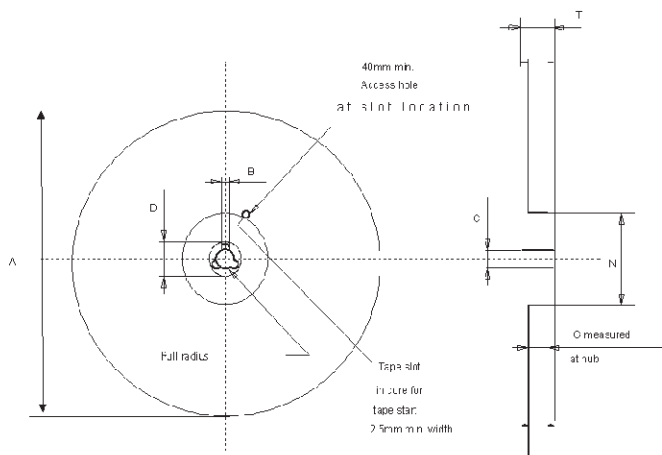
SO-8 TUBE SHIPMENT (no suffix)



Base Q.ty	100
Bulk Q.ty	2000
Tube length (± 0.5)	532
A	3.2
B	6
C (± 0.1)	0.6

All dimensions are in mm.

TAPE AND REEL SHIPMENT (suffix "13TR")



REEL DIMENSIONS

Base Q.ty	2500
Bulk Q.ty	2500
A (max)	330
B (min)	1.5
C (± 0.2)	13
F	20.2
G (+ 2 / - 0)	12.4
N (min)	60
T (max)	18.4

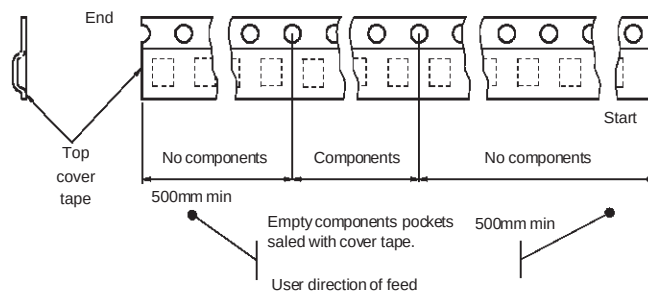
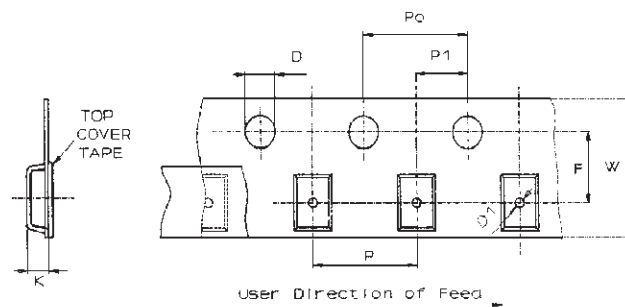
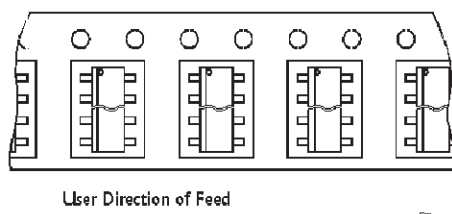
All dimensions are in mm.

TAPE DIMENSIONS

According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb 1986

Tape width	W	12
Tape Hole Spacing	P0 (± 0.1)	4
Component Spacing	P	8
Hole Diameter	D ($\pm 0.1/-0$)	1.5
Hole Diameter	D1 (min)	1.5
Hole Position	F (± 0.05)	5.5
Compartment Depth	K (max)	4.5
Hole Spacing	P1 (± 0.1)	2

All dimensions are in mm.



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