

Features

- Output frequency range: 16.67 MHz to 200 MHz
- Input frequency range: 16.67 MHz to 200 MHz
- 2.5 V or 3.3 V operation
- Split 2.5 V and 3.3 V outputs
- $\pm 2\%$ maximum output duty cycle variation
- 11 clock outputs: drive up to 22 clock lines
- LVCMOS reference clock input
- 125 ps maximum output-output skew
- PLL bypass mode
- Spread Aware™
- Output enable and disable
- Pin compatible with MPC9352 and MPC952
- Industrial temperature range: -40°C to $+85^{\circ}\text{C}$
- 32-pin 1.4 mm TQFP package

Description

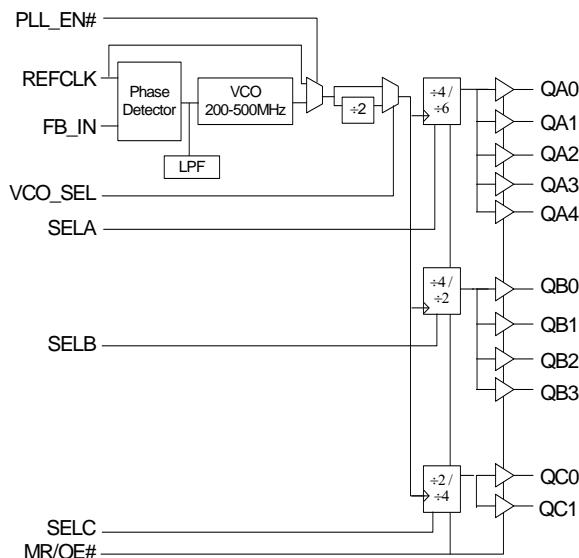
The CY29352 is a low voltage high performance 200 MHz PLL based zero delay buffer designed for high speed clock distribution applications.

The CY29352 features an LVCMOS reference clock input and provides 11 outputs partitioned in three banks of five, four, and two outputs. Bank A divides the VCO output by four and six while bank B divides by four and two, and bank C divides by two and four per SEL(A:C) settings, see [Function Table on page 4](#). These dividers allow output to input ratios of 3:1, 2:1, 3:2, 1:1, 2:3, 1:2, and 1:3. Each LVCMOS compatible output drives 50 Ω series or parallel terminated transmission lines. For series terminated transmission lines, each output drives one or two traces, giving the device an effective fanout of 1:22.

The PLL is stable if the VCO is configured to run between 200 MHz to 500 MHz. This allows a wide range of output frequencies from 16.67 MHz to 200 MHz. For normal operation, the external feedback input, FB_IN, is connected to one of the outputs. The internal VCO runs at multiples of the input reference clock set by the feedback divider, see [Frequency Table on page 4](#). When PLL_EN# is HIGH, PLL is bypassed and the reference clock directly feeds the output dividers. This mode is fully static and the minimum input clock frequency specification does not apply.

For a complete list of related documentation, click [here](#).

Block Diagram

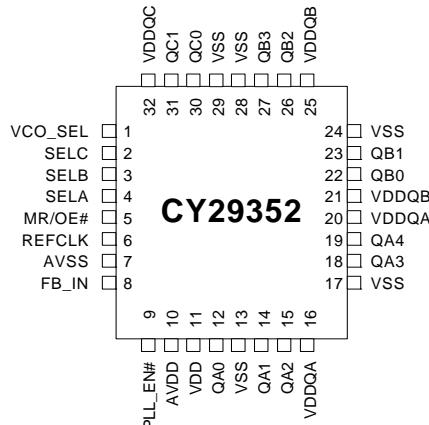


Contents

Pinouts	3
Pin Definitions	3
Frequency Table	4
Function Table	4
Absolute Maximum Conditions	5
DC Parameters	5
DC Parameters	6
AC Parameters	7
AC Parameters	8
Ordering Information	10
Ordering Code Definitions	10
Package Drawing and Dimension	11
Acronyms	12
Document Conventions	12
Units of Measure	12
Document History Page	13
Sales, Solutions, and Legal Information	14
Worldwide Sales and Design Support	14
Products	14
PSoC® Solutions	14
Cypress Developer Community	14
Technical Support	14

Pinouts

Figure 1. 32-pin TQFP pinout



Pin Definitions

Pin	Name	I/O ^[1]	Type	Description
6	REFCLK	I, PD	LVC MOS	Reference clock input
12, 14, 15, 18, 19	QA(0:4)	O	LVC MOS	Clock output bank A
22, 23, 26, 27	QB(0:3)	O	LVC MOS	Clock output bank B
30, 31	QC(0,1)	O	LVC MOS	Clock output bank C
8	FB_IN	I, PD	LVC MOS	Feedback clock input. Connect to an output for normal operation. This input must be at the same voltage rail as input reference clock, see Frequency Table on page 4 .
1	VCO_SEL	I, PD	LVC MOS	VCO divider select input, see Function Table on page 4 .
5	MR/OE#	I, PD	LVC MOS	Master reset or output enable and disable input, see Function Table on page 4 .
9	PLL_EN#	I, PD	LVC MOS	PLL enable and disable input, see Function Table on page 4 .
2, 3, 4	SEL(A:C)	I, PD	LVC MOS	Frequency select input, bank (A:C), see Function Table on page 4 .
16, 20	V _{DDQA}	Supply	V _{DD}	2.5 V or 3.3 V power supply for bank A output clocks ^[2, 3]
21, 25	V _{DDQB}	Supply	V _{DD}	2.5 V or 3.3 V power supply for bank B output clocks ^[2, 3]
32	V _{DDQC}	Supply	V _{DD}	2.5 V or 3.3 V power supply for bank C output clocks ^[2, 3]
10	A _{VDD}	Supply	V _{DD}	2.5 V or 3.3 V power supply for PLL ^[2, 3]
11	V _{DD}	Supply	V _{DD}	2.5 V or 3.3 V power supply for core and inputs ^[2, 3]
7	A _{VSS}	Supply	Ground	Analog ground
13, 17, 24, 28, 29	V _{SS}	Supply	Ground	Common ground

Notes

- PD = Internal pull down.
- A 0.1- μ F bypass capacitor must be placed as close as possible to each positive power pin (< 0.2"). If these bypass capacitors are not close to the pins, the high frequency filtering characteristics are cancelled by the lead inductance of the traces.
- A_{VDD} and V_{DD} pins must be connected to a power supply level that is at least equal or higher than that of V_{DDQA}, V_{DDQB}, and V_{DDQC} power supply pins.

Frequency Table

VCO_SEL	Feedback Output Divider	VCO	Input Frequency Range (AVDD = 3.3 V)	Input Frequency Range (AVDD = 2.5 V)
0	÷2	Input clock * 2	100 MHz to 200 MHz	100 MHz to 200 MHz
0	÷4	Input clock * 4	50 MHz to 125 MHz	50 MHz to 100 MHz
0	÷6	Input clock * 6	33.33 MHz to 83.33 MHz	33.33 MHz to 66.67 MHz
1	÷2	Input clock * 4	50 MHz to 125 MHz	50 MHz to 100 MHz
1	÷4	Input clock * 8	25 MHz to 62.5 MHz	25 MHz to 50 MHz
1	÷6	Input clock * 12	16.67 MHz to 41.67 MHz	16.67 MHz to 33.33 MHz

Function Table

Control	Default	0	1
VCO_SEL	0	VCO	VCO ÷ 2
PLL_EN#	0	PLL enabled, the VCO output connects to the output dividers	Bypass mode, PLL disabled, the input clock connects to the output dividers
MR/OE#	0	Outputs enabled	Outputs disabled (three-state), VCO runs at its minimum frequency
SEL_A	0	QA = VCO ÷ 4	QA = VCO ÷ 6
SEL_B	0	QB = VCO ÷ 4	QB = VCO ÷ 2
SEL_C	0	QC = VCO ÷ 2	QC = VCO ÷ 4

Absolute Maximum Conditions

Parameter	Description	Condition	Min	Max	Unit
V_{DD}	DC supply voltage		-0.3	5.5	V
V_{DD}	DC operating voltage	Functional	2.375	3.465	V
V_{IN}	DC input voltage	Relative to V_{SS}	-0.3	$V_{DD} + 0.3$	V
V_{OUT}	DC output voltage	Relative to V_{SS}	-0.3	$V_{DD} + 0.3$	V
V_{TT}	Output termination voltage		-	$V_{DD} \div 2$	V
LU	Latch up immunity	Functional	200	-	mA
R_{PS}	Power supply ripple	Ripple frequency < 100 kHz	-	150	mVp-p
T_S	Temperature, storage	Non functional	-65	+150	°C
T_A	Temperature, operating ambient	Functional	-40	+85	°C
T_J	Temperature, junction	Functional	-	155	°C
\emptyset_{JC}	Dissipation, junction to case	Functional	-	42	°C/W
\emptyset_{JA}	Dissipation, junction to ambient	Functional	-	105	°C/W
ESD_H	ESD protection (human body model)		2000	-	V
FIT	Failure in time	Manufacturing test	10		ppm

DC Parameters

($V_{DD} = 2.5 \text{ V} \pm 5\%$, $T_A = -40 \text{ }^{\circ}\text{C}$ to $+85 \text{ }^{\circ}\text{C}$)

Parameter	Description	Condition	Min	Typ	Max	Unit
V_{IL}	Input voltage, low	LVC MOS	-	-	0.7	V
V_{IH}	Input voltage, high	LVC MOS	1.7	-	$V_{DD} + 0.3$	V
V_{OL}	Output voltage, low ^[4]	$I_{OL} = 15 \text{ mA}$		-	0.6	V
V_{OH}	Output voltage, high ^[4]	$I_{OH} = -15 \text{ mA}$	1.8	-		V
I_{IL}	Input current, low	$V_{IL} = V_{SS}$	-	-	-10	μA
I_{IH}	Input current, high ^[5]	$V_{IL} = V_{DD}$	-	-	100	μA
I_{DDA}	PLL supply current	AV_{DD} only	-	5	10	mA
I_{DDQ}	Quiescent supply current	All V_{DD} pins except AV_{DD}	-	3	5	mA
I_{DD}	Dynamic supply current		-	170		mA
C_{IN}	Input pin capacitance		-	4		pF
Z_{OUT}	Output impedance		-	17–20		Ω

Notes

- Driving one 50Ω parallel terminated transmission line to a termination voltage of V_{TT} . Alternatively, each output drives up to two 50Ω series terminated transmission lines.
- Inputs have pull down resistors that affect the input current.

DC Parameters

($V_{DD} = 3.3 \text{ V} \pm 5\%$, $T_A = -40 \text{ }^\circ\text{C}$ to $+85 \text{ }^\circ\text{C}$)

Parameter	Description	Condition	Min	Typ	Max	Unit
V_{IL}	Input voltage, low	LVC MOS	—	—	0.8	V
V_{IH}	Input voltage, high	LVC MOS	2.0	—	$V_{DD} + 0.3$	V
V_{OL}	Output voltage, low ^[6]	$I_{OL} = 24 \text{ mA}$	—	—	0.55	V
		$I_{OL} = 12 \text{ mA}$	—	—	0.30	
V_{OH}	Output voltage, high ^[6]	$I_{OH} = -24 \text{ mA}$	2.4	—	—	V
I_{IL}	Input current, low	$V_{IL} = V_{SS}$	—	—	-10	μA
I_{IH}	Input current, high ^[7]	$V_{IL} = V_{DD}$	—	—	100	μA
I_{DDA}	PLL supply current	AV_{DD} only	—	5	10	mA
V_{IL}	Input voltage, low	LVC MOS	—	—	0.8	V
V_{IH}	Input voltage, high	LVC MOS	2.0	—	$V_{DD} + 0.3$	V
V_{OL}	Output voltage, low ^[6]	$I_{OL} = 24 \text{ mA}$	—	—	0.55	V
		$I_{OL} = 12 \text{ mA}$	—	—	0.30	
V_{OH}	Output voltage, high ^[6]	$I_{OH} = -24 \text{ mA}$	2.4	—	—	V
I_{IL}	Input current, low	$V_{IL} = V_{SS}$	—	—	-10	μA
I_{IH}	Input current, high ^[7]	$V_{IL} = V_{DD}$	—	—	100	μA
I_{DDA}	PLL supply current	AV_{DD} only	—	5	10	mA
I_{DDQ}	Quiescent supply current	All V_{DD} pins except AV_{DD}	—	3	5	mA
I_{DD}	Dynamic supply current		—	240	—	mA
C_{IN}	Input pin capacitance		—	4	—	pF
Z_{OUT}	Output impedance		—	14–17	—	Ω

Notes

6. Driving one 50Ω parallel terminated transmission line to a termination voltage of V_{TT} . Alternatively, each output drives up to two 50Ω series terminated transmission lines.
7. Inputs have pull down resistors that affect the input current.

AC Parameters

($V_{DD} = 2.5 \text{ V} \pm 5\%$, $T_A = -40 \text{ }^\circ\text{C}$ to $+85 \text{ }^\circ\text{C}$)

Parameter ^[8]	Description	Condition	Min	Typ	Max	Unit
f_{VCO}	VCO frequency		200	—	400	MHz
f_{in}	Input frequency	÷2 feedback	100	—	200	MHz
		÷4 feedback	50	—	100	
		÷6 feedback	33.33	—	66.67	
		÷8 feedback	25	—	50	
		÷12 feedback	16.67	—	33.33	
		Bypass mode (PLL_EN# = 1)	0	—	200	
f_{refDC}	Input duty cycle		25	—	75	%
t_r, t_f	REFCLK input rise and fall time	0.7 V to 1.7 V	—	—	1.0	ns
f_{MAX}	Maximum output frequency	÷2 output	100	—	200	MHz
		÷4 output	50	—	100	
		÷6 output	33.33	—	66.67	
		÷8 output	25	—	50	
		÷12 output	16.67	—	33.33	
DC	Output duty cycle	$f_{MAX} < 100 \text{ MHz}$	47	—	53	%
		$f_{MAX} > 100 \text{ MHz}$	44	—	56	
t_r, t_f	Output rise and fall times	0.6 V to 1.8 V	0.1	—	1.0	ns
$t_{(\phi)}$	Propagation delay (static phase offset)	REFCLK to FB_IN, same V_{DD} , does not include jitter	—100	—	100	ps
$t_{sk(O)}$	Output to output skew	Skew within bank	—	—	125	ps
$t_{sk(B)}$	Bank to bank skew	Banks at same voltage, same frequency	—	—	175	ps
		Banks at same voltage, different frequency	—	—	225	
$t_{PLZ, HZ}$	Output disable time		—	—	8	ns
$t_{PZL, ZH}$	Output enable time		—	—	10	ns
BW	PLL closed loop bandwidth (-3 dB)	÷2 feedback	—	2	—	MHz
		÷4 feedback	—	1–1.5	—	
		÷6 feedback	—	0.6	—	
		÷8 feedback	—	0.75	—	
		÷12 feedback	—	0.5	—	
$t_{JIT(CC)}$	Cycle to cycle jitter	Same frequency	—	—	100	ps
		Multiple frequencies	—	—	300	
$t_{JIT(PER)}$	Period jitter	Same frequency	—	—	100	ps
		Multiple frequencies	—	—	150	
$t_{JIT(\phi)}$	IO phase jitter	$VCO < 300 \text{ MHz}$	—	150	—	ps
		$VCO > 300 \text{ MHz}$	—	100	—	
t_{LOCK}	Maximum PLL lock time		—	—	1	ms

Note

8. AC characteristics apply for parallel output termination of 50Ω to V_{TT} . Outputs are at the same supply voltage unless otherwise stated. Parameters are guaranteed by characterization and are not 100% tested.

AC Parameters

($V_{DD} = 3.3 \text{ V} \pm 5\%$, $T_A = -40 \text{ }^\circ\text{C}$ to $+85 \text{ }^\circ\text{C}$)

Parameter ^[9]	Description	Condition	Min	Typ	Max	Unit
f_{VCO}	VCO frequency		200	—	500	MHz
f_{in}	Input frequency	÷2 feedback	100	—	200	MHz
		÷4 feedback	50	—	125	
		÷6 feedback	33.33	—	83.33	
		÷8 feedback	25	—	62.5	
		÷12 feedback	16.67	—	41.67	
		Bypass mode (PLL_EN# = 1)	0	—	200	
f_{refDC}	Input duty cycle		25	—	75	%
t_r, t_f	REFCLK input rise and fall time	0.8 V to 2.0 V	—	—	1.0	ns
f_{MAX}	Maximum output frequency	÷2 output	100	—	200	MHz
		÷4 output	50	—	125	
		÷6 output	33.33	—	83.33	
		÷8 output	25	—	62.5	
		÷12 output	16.67	—	41.67	
DC	Output duty cycle	$f_{MAX} < 100 \text{ MHz}$	48	—	52	%
			—	—	—	
$t_{(\phi)}$	Propagation delay (static phase offset)	REFCLK to FB_IN, same V_{DD} , does not include jitter	-100	—	200	ps
$t_{sk(O)}$	Output to output skew	Skew within each Bank	—	—	125	ps
$t_{sk(B)}$	Bank to bank skew	Banks at same voltage, same frequency	—	—	175	ps
		Banks at same voltage, different frequency	—	—	235	
		Banks at different voltage	—	—	425	
$t_{PLZ, HZ}$	Output disable time		—	—	8	ns
$t_{PZL, ZH}$	Output enable time		—	—	10	ns
BW	PLL closed loop bandwidth (-3 dB)	÷2 feedback	—	2	—	MHz
		÷4 feedback	—	1-1.5	—	
		÷6 feedback	—	0.6	—	
		÷8 feedback	—	0.75	—	
		÷12 feedback	—	0.5	—	
$t_{JIT(CC)}$	Cycle to cycle jitter	Same frequency	—	—	100	ps
		Multiple frequencies	—	—	275	
$t_{JIT(PER)}$	Period jitter	Same frequency	—	—	100	ps
		Multiple frequencies	—	—	150	
$t_{JIT(\phi)}$	IO phase jitter	$VCO < 300 \text{ MHz}$	—	150	—	ps
		$VCO > 300 \text{ MHz}$	—	100	—	
t_{LOCK}	Maximum PLL lock time		—	—	1	ms

Note

9. AC characteristics apply for parallel output termination of 50Ω to V_{TT} . Outputs are at the same supply voltage unless otherwise stated. Parameters are guaranteed by characterization and are not 100% tested.

Figure 2. AC Test Reference for $V_{DD} = 3.3\text{ V} / 2.5\text{ V}$

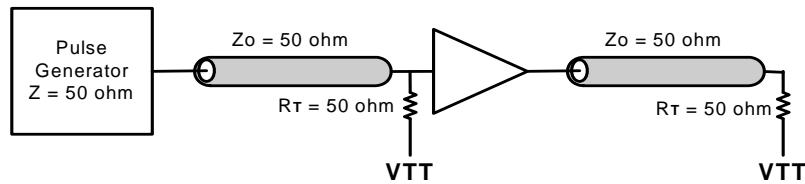


Figure 3. Propagation Delay $t(\phi)$, Static Phase Offset

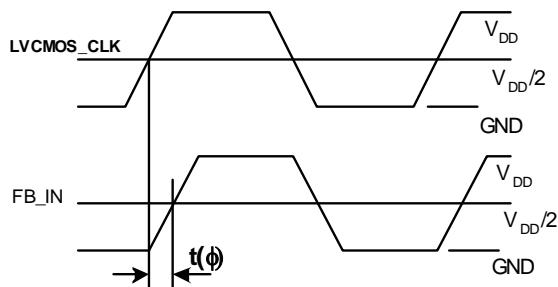


Figure 4. Output Duty Cycle (DC)

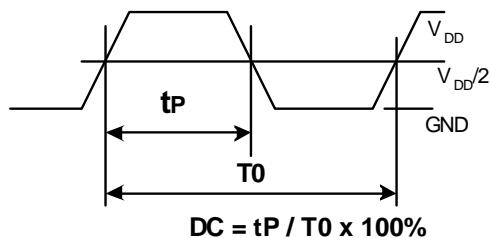
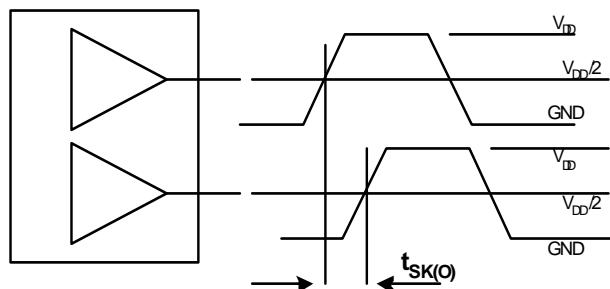


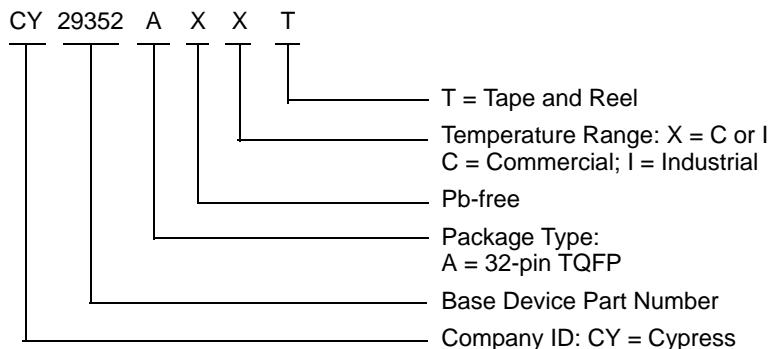
Figure 5. Output to Output Skew, $t_{sk(O)}$



Ordering Information

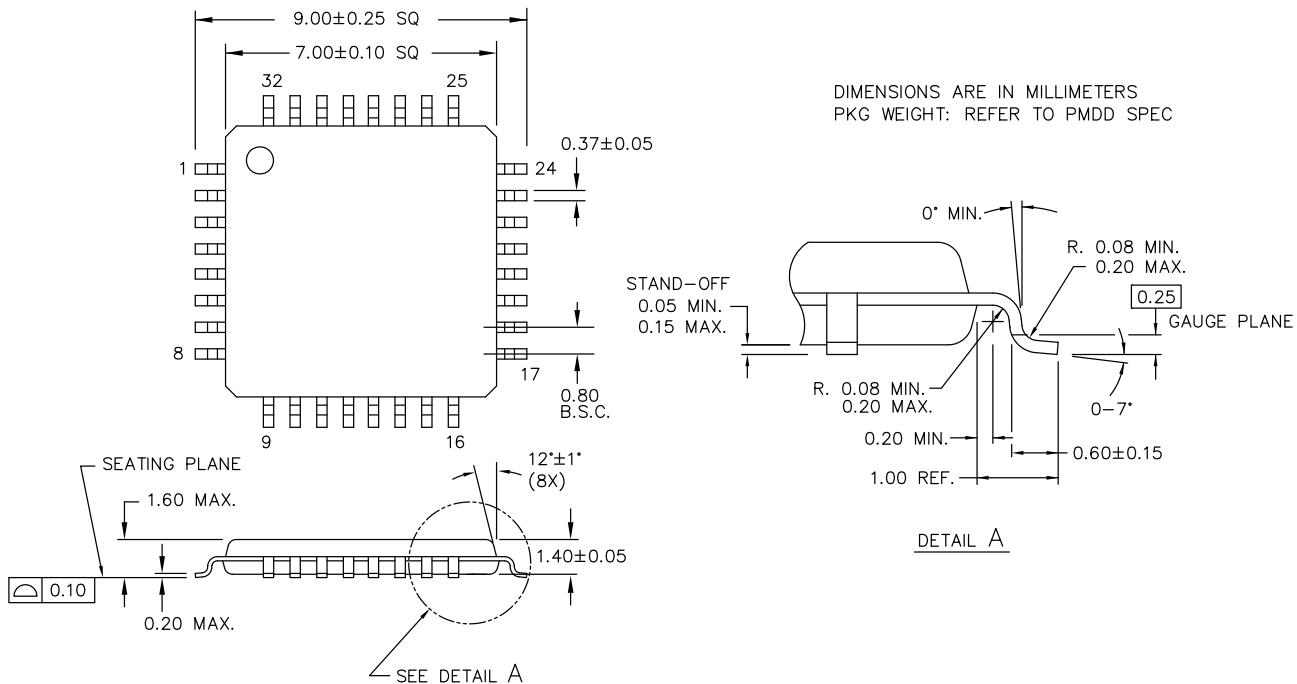
Part Number	Package Type	Product Flow
Pb-free		
CY29352AXI	32-pin TQFP	Industrial, -40 °C to +85 °C
CY29352AXIT	32-pin TQFP – Tape and Reel	Industrial, -40 °C to 85 °C

Ordering Code Definitions



Package Drawing and Dimension

Figure 6. 32-pin TQFP (7 x 7 x 1.4 mm) Package Outline, 51-85088



51-85088 *E

Acronyms

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
ESD	electrostatic discharge
I/O	Input/Output
LVCMOS	Low Voltage Complementary Metal Oxide Semiconductor
LVTTL	Low Voltage Transistor-Transistor Logic
PLL	Phase Locked Loop
TQFP	Thin Quad Flat Pack
VCO	Voltage-Controlled Oscillator

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
Hz	hertz
kHz	kilohertz
kV	kilovolt
MHz	megahertz
µA	microampere
mA	milliampere
ms	millisecond
mV	millivolt
ns	nanosecond
Ω	ohm
ppm	parts per million
%	percent
pF	picofarad
ps	picosecond
V	volt
W	watt

Document History Page

Document Title: CY29352, 2.5 V or 3.3 V, 200 MHz, 11 Output Zero Delay Buffer Document Number: 38-07476				
Rev.	ECN No.	Issue Date	Orig. of Change	Description of Change
**	124654	03/21/03	RGL	New Data Sheet
*A	739798	See ECN	RGL	Removed the leaded parts and replaced by lead-free parts
*B	1923227	See ECN	PYG / KVM / AESA	Corrected package thickness from 1.0 mm to 1.4 mm in Features section on page 1 and in Figure 5.
*C	3163592	02/05/2011	CXQ	Added Ordering Code Definitions . Updated Package Drawing and Dimension . Added Acronyms and Units of Measure . Updated in new template.
*D	4311272	03/17/2014	CINM	Updated Package Drawing and Dimension : spec 51-85088 – Changed revision from *C to *E. Updated in new template. Completing Sunset Review.
*E	4587350	12/05/2014	AJU	Added related documentation hyperlink in page 1.
*F	5740179	05/17/2017	PSR	Changed TCLK references to REFCLK. Updated the template.

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at [Cypress Locations](#).

Products

ARM® Cortex® Microcontrollers	cypress.com/arm
Automotive	cypress.com/automotive
Clocks & Buffers	cypress.com/clocks
Interface	cypress.com/interface
Internet of Things	cypress.com/iot
Memory	cypress.com/memory
Microcontrollers	cypress.com/mcu
PSoC	cypress.com/psoc
Power Management ICs	cypress.com/pmic
Touch Sensing	cypress.com/touch
USB Controllers	cypress.com/usb
Wireless Connectivity	cypress.com/wireless

PSoC® Solutions

[PSoC 1](#) | [PSoC 3](#) | [PSoC 4](#) | [PSoC 5LP](#) | [PSoC 6](#)

Cypress Developer Community

[Forums](#) | [WICED IOT Forums](#) | [Projects](#) | [Video](#) | [Blogs](#) | [Training](#) | [Components](#)

Technical Support

cypress.com/support

© Cypress Semiconductor Corporation, 2003-2017. This document is the property of Cypress Semiconductor Corporation and its subsidiaries, including Spansion LLC ("Cypress"). This document, including any software or firmware included or referenced in this document ("Software"), is owned by Cypress under the intellectual property laws and treaties of the United States and other countries worldwide. Cypress reserves all rights under such laws and treaties and does not, except as specifically stated in this paragraph, grant any license under its patents, copyrights, trademarks, or other intellectual property rights. If the Software is not accompanied by a license agreement and you do not otherwise have a written agreement with Cypress governing the use of the Software, then Cypress hereby grants you a personal, non-exclusive, nontransferable license (without the right to sublicense) (1) under its copyright rights in the Software (a) for Software provided in source code form, to modify and reproduce the Software solely for use with Cypress hardware products, only internally within your organization, and (b) to distribute the Software in binary code form externally to end users (either directly or indirectly through resellers and distributors), solely for use on Cypress hardware product units, and (2) under those claims of Cypress's patents that are infringed by the Software (as provided by Cypress, unmodified) to make, use, distribute, and import the Software solely for use with Cypress hardware products. Any other use, reproduction, modification, translation, or compilation of the Software is prohibited.

TO THE EXTENT PERMITTED BY APPLICABLE LAW, CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS DOCUMENT OR ANY SOFTWARE OR ACCOMPANYING HARDWARE, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. To the extent permitted by applicable law, Cypress reserves the right to make changes to this document without further notice. Cypress does not assume any liability arising out of the application or use of any product or circuit described in this document. Any information provided in this document, including any sample design information or programming code, is provided only for reference purposes. It is the responsibility of the user of this document to properly design, program, and test the functionality and safety of any application made of this information and any resulting product. Cypress products are not designed, intended, or authorized for use as critical components in systems designed or intended for the operation of weapons, weapons systems, nuclear installations, life-support devices or systems, other medical devices or systems (including resuscitation equipment and surgical implants), pollution control or hazardous substances management, or other uses where the failure of the device or system could cause personal injury, death, or property damage ("Unintended Uses"). A critical component is any component of a device or system whose failure to perform can be reasonably expected to cause the failure of the device or system, or to affect its safety or effectiveness. Cypress is not liable, in whole or in part, and you shall and hereby do release Cypress from any claim, damage, or other liability arising from or related to all Unintended Uses of Cypress products. You shall indemnify and hold Cypress harmless from and against all claims, costs, damages, and other liabilities, including claims for personal injury or death, arising from or related to any Unintended Uses of Cypress products.

Cypress, the Cypress logo, Spansion, the Spansion logo, and combinations thereof, WICED, PSoC, CapSense, EZ-USB, F-RAM, and Traveo are trademarks or registered trademarks of Cypress in the United States and other countries. For a more complete list of Cypress trademarks, visit cypress.com. Other names and brands may be claimed as property of their respective owners.