

RQJ0602EGDQS

Silicon P Channel MOS FET
Power Switching

REJ03G1268-0300

Rev.3.00

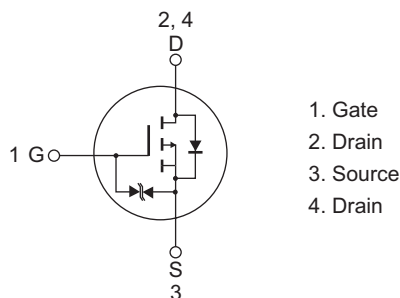
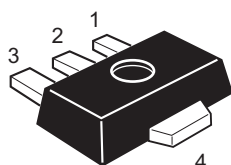
Jun 05, 2006

Features

- Low on-resistance
 $R_{DS(on)} = 485 \text{ m}\Omega$ typ ($V_{GS} = -10 \text{ V}$, $I_D = -0.75 \text{ A}$)
- Low drive current
- High speed switching
- 4.5 V gate drive

Outline

RENESAS package code: PLZZ0004CA-A
(Package name: UPAK®)



Note: Marking is "EG".

*UPAK is a trademark of Renesas Technology Corp.

Absolute Maximum Ratings

($T_a = 25^\circ\text{C}$)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	-60	V
Gate to source voltage	V_{GSS}	+10 / -20	V
Drain current	I_D	-1.5	A
Drain peak current	$I_{D(pulse)}$ ^{Note1}	-2.2	A
Body - drain diode reverse drain current	I_{DR}	-1.5	A
Channel dissipation	P_{ch} ^{Note2}	1.5	W
Channel dissipation	$P_{ch(pulse)}$ ^{Note1}	5	W
Channel temperature	T_{ch}	150	$^\circ\text{C}$
Storage temperature	T_{stg}	-55 to +150	$^\circ\text{C}$

Notes: 1. $PW \leq 1 \text{ s}$, duty cycle $\leq 1\%$

2. When using the glass epoxy board (FR-4: 40 x 40 x 1 mm)

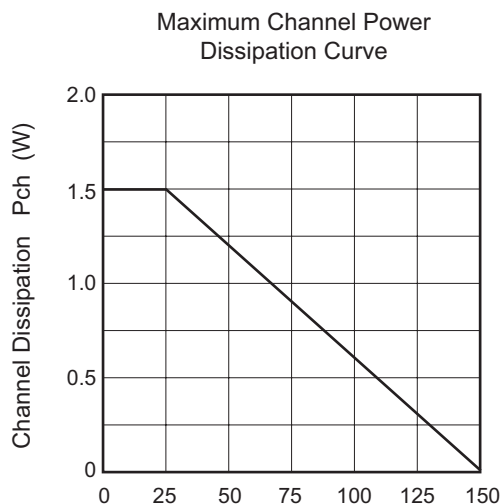
Electrical Characteristics

(Ta = 25°C)

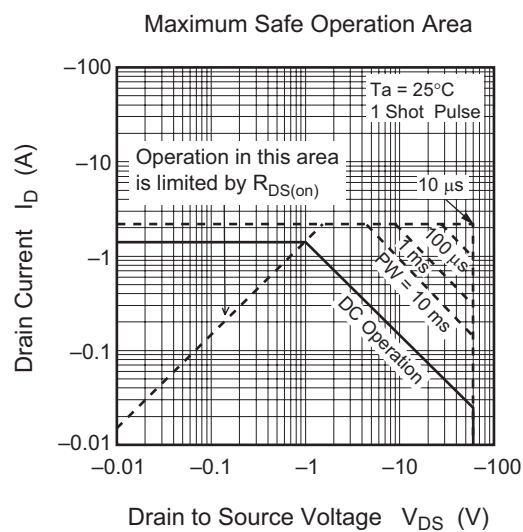
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	-60	—	—	V	$I_D = -10 \text{ mA}$, $V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	+10	—	—	V	$I_G = +100 \mu\text{A}$, $V_{DS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	-20	—	—	V	$I_G = -100 \mu\text{A}$, $V_{DS} = 0$
Gate to source leak current	I_{GSS}	—	—	+10	μA	$V_{GS} = +8 \text{ V}$, $V_{DS} = 0$
Gate to source leak current	I_{GSS}	—	—	-10	μA	$V_{GS} = -16 \text{ V}$, $V_{DS} = 0$
Drain to source leak current	I_{DSS}	—	—	-1	μA	$V_{DS} = -60 \text{ V}$, $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	-1.0	—	-2.0	V	$V_{DS} = -10 \text{ V}$, $I_D = -1 \text{ mA}$
Drain to source on state resistance	$R_{DS(on)}$	—	485	607	$\text{m}\Omega$	$I_D = -0.75 \text{ A}$, $V_{GS} = -10 \text{ V}^{\text{Note3}}$
	$R_{DS(on)}$	—	620	868	$\text{m}\Omega$	$I_D = -0.75 \text{ A}$, $V_{GS} = -4.5 \text{ V}^{\text{Note3}}$
Forward transfer admittance	$ y_{fs} $	0.8	1.4	—	S	$I_D = -0.75 \text{ A}$, $V_{DS} = -10 \text{ V}^{\text{Note3}}$
Input capacitance	C_{iss}	—	135	—	pF	$V_{DS} = -10 \text{ V}$ $V_{GS} = 0$ $f = 1 \text{ MHz}$
Output capacitance	C_{oss}	—	24	—	pF	
Reverse transfer capacitance	C_{rss}	—	12	—	pF	
Turn - on delay time	$t_{d(on)}$	—	11	—	ns	$I_D = -1 \text{ A}$ $V_{GS} = -10 \text{ V}$ $R_L = 6.6 \Omega$ $R_g = 4.7 \Omega$
Rise time	t_r	—	28	—	ns	
Turn - off delay time	$t_{d(off)}$	—	29	—	ns	
Fall time	t_f	—	3.6	—	ns	
Total gate charge	Q_g	—	2.9	—	nC	$V_{DD} = -10 \text{ V}$
Gate to source charge	Q_{gs}	—	0.6	—	nC	$V_{GS} = -10 \text{ V}$
Gate to drain charge	Q_{gd}	—	0.3	—	nC	$I_D = -1.5 \text{ A}$
Body - drain diode forward voltage	V_{DF}	—	-0.9	—	V	$I_F = -1.5 \text{ A}$, $V_{GS} = 0^{\text{Note3}}$

Notes: 3. Pulse test

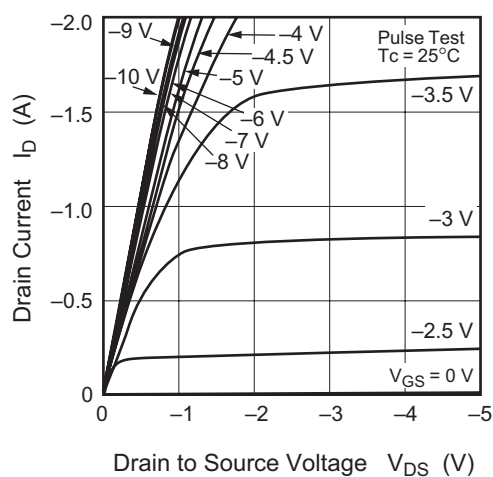
Main Characteristics

Ambient Temperature T_a (°C)

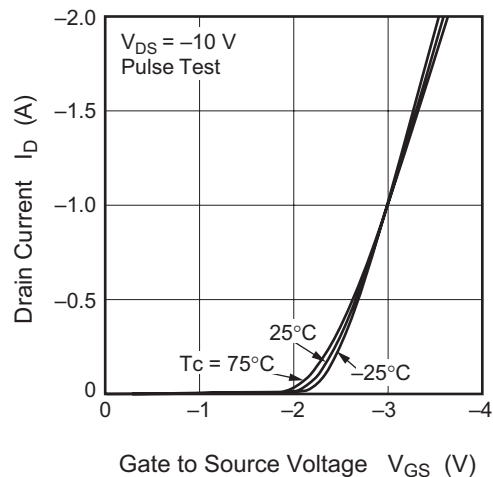
*When using the glass epoxy board (FR-4: 40 × 40 × 1 mm)



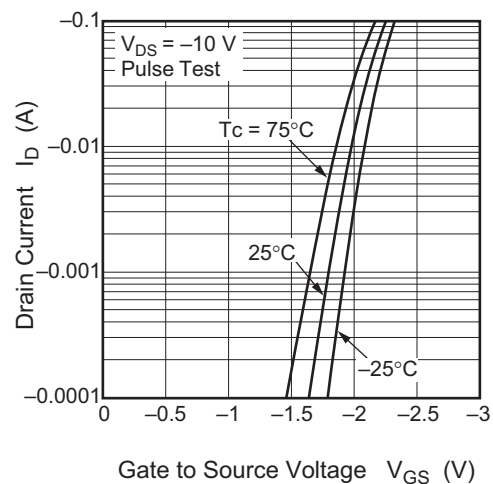
Typical Output Characteristics



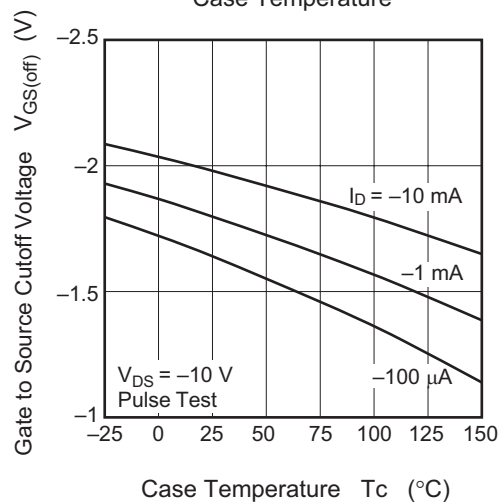
Typical Transfer Characteristics (1)

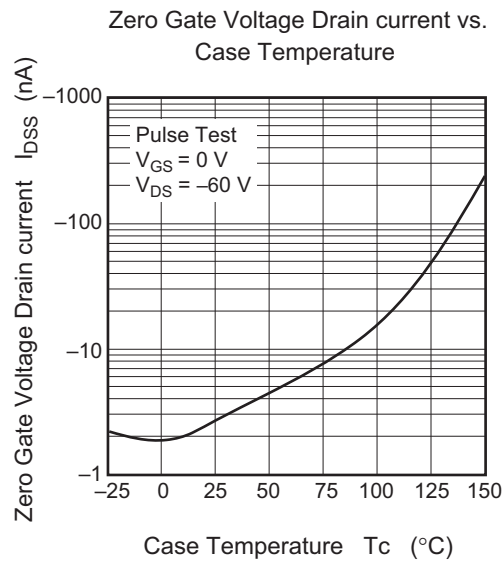
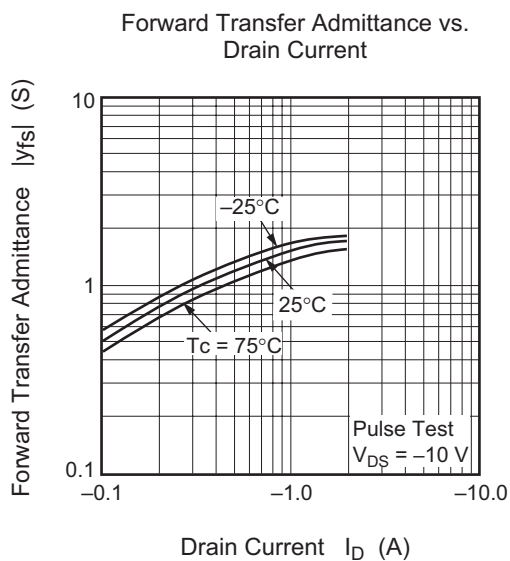
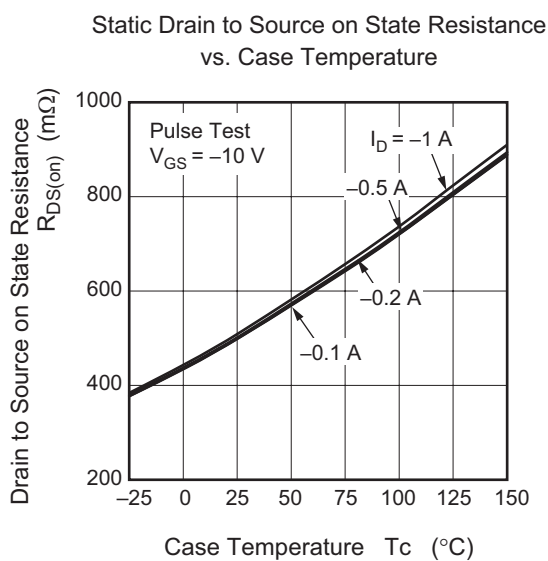
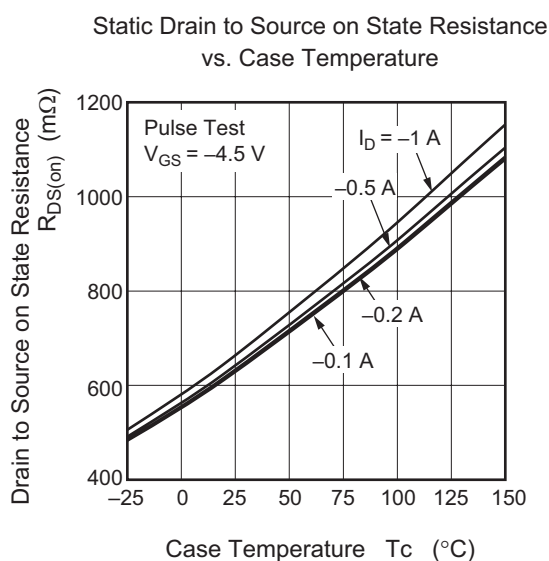
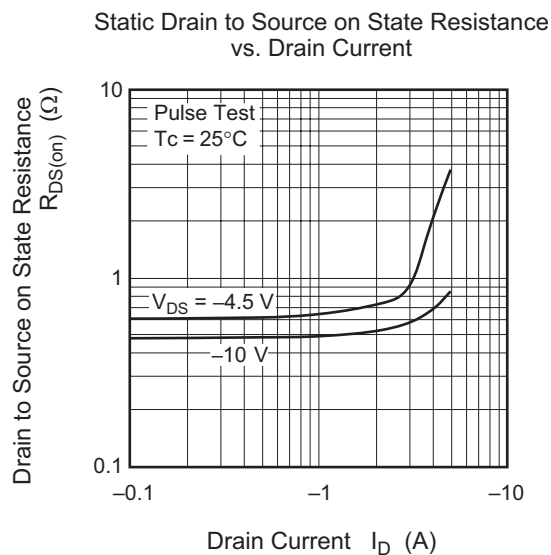
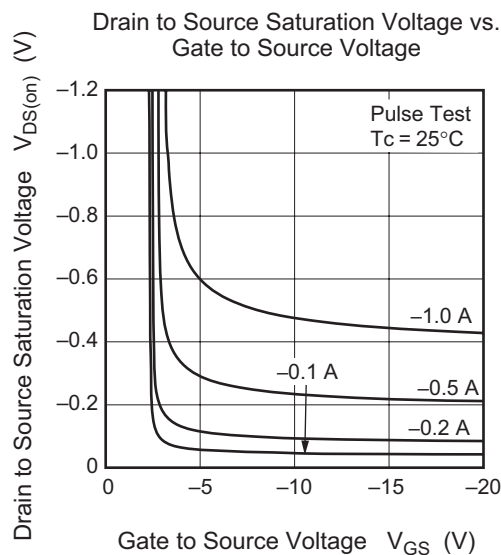


Typical Transfer Characteristics (2)

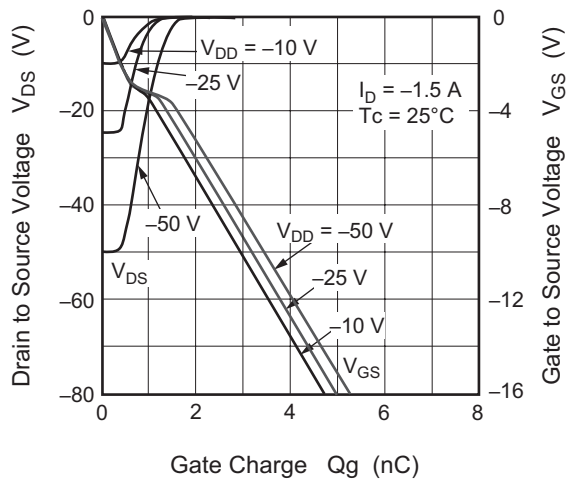


Gate to Source Cutoff Voltage vs. Case Temperature

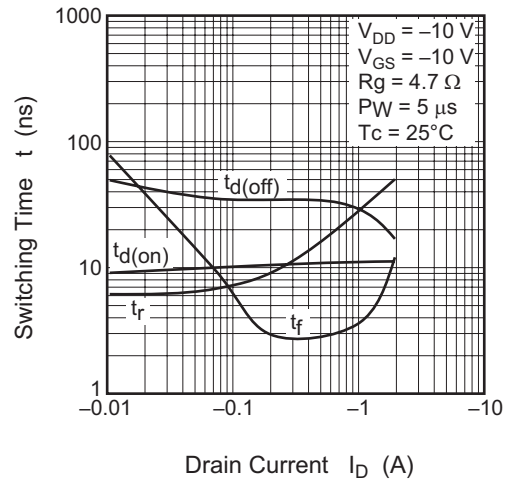




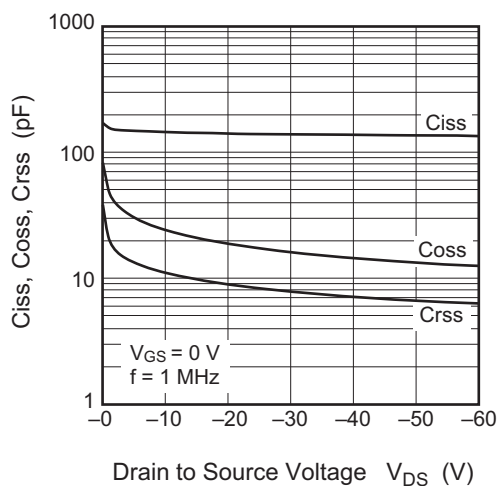
Dynamic Input Characteristics



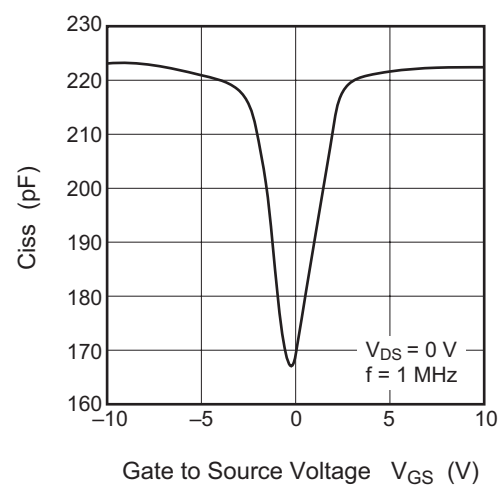
Switching Characteristics



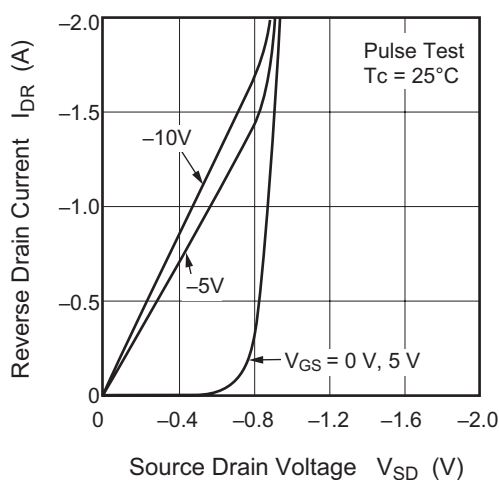
Typical Capacitance vs. Drain to Source Voltage



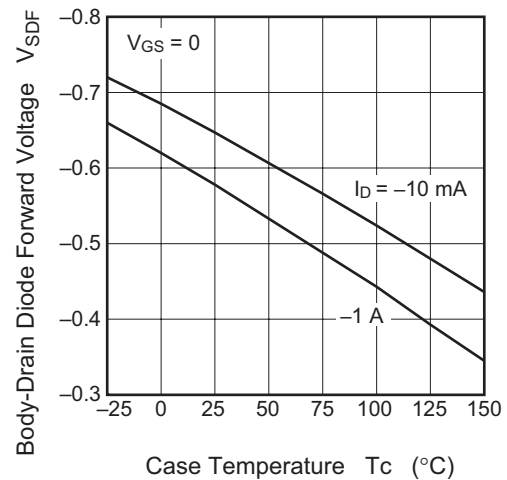
Input Capacitance vs. Gate to Source Voltage



Reverse Drain Current vs. Source to Drain Voltage



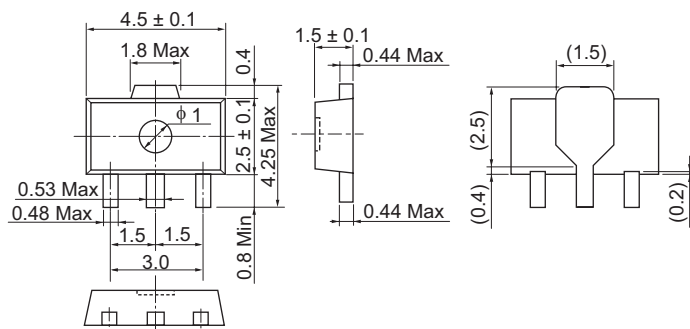
Body-Drain Diode Forward Voltage vs. Case Temperature



Package Dimensions

Package Name	JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
UPAK	SC-62	PLZZ0004CA-A	UPAK / UPAKV	0.050g

Unit: mm



Ordering Information

Part Name	Quantity	Shipping Container
RQJ0602EGDQSTL-E	1000 pcs.	ϕ 178 reel, 12 mm Emboss taping

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