PSMN059-150Y

N-channel TrenchMOS SiliconMAX standard level FET

Rev. 03 — 17 March 2011 Product data sheet

1. Product profile

1.1 General description

SiliconMAX standard level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product is designed and qualified for use in computing, communications, consumer and industrial applications only.

1.2 Features and benefits

- Higher operating power due to low thermal resistance
- Suitable for high frequency applications due to fast switching characteristics

1.3 Applications

- Class D amplifier
- DC-to-DC converters
- Motion control
- Switched-mode power supplies

1.4 Quick reference data

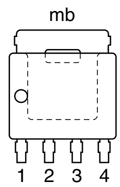
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25$ °C; $T_j \leq 150$ °C	-	-	150	V
I_D	drain current	$T_{mb} = 25$ °C; $V_{GS} = 10$ V; see Figure 1; see Figure 3	-	-	43	A
P_{tot}	total power dissipation	$T_{mb} = 25$ °C; see Figure 2	-	-	113	W
Static characteristics						
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10$ V; $I_D = 12$ A; $T_j = 25$ °C; see Figure 9; see Figure 10	-	46	59	mΩ
Dynamic characteristics						
Q_{GD}	gate-drain charge	$V_{GS} = 10$ V; $I_D = 12$ A; $V_{DS} = 75$ V; see Figure 11; see Figure 12	-	9.1	-	nC

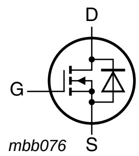
2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source		
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		



SOT669 (LFPAK)



3. Ordering information

Table 3. Ordering information

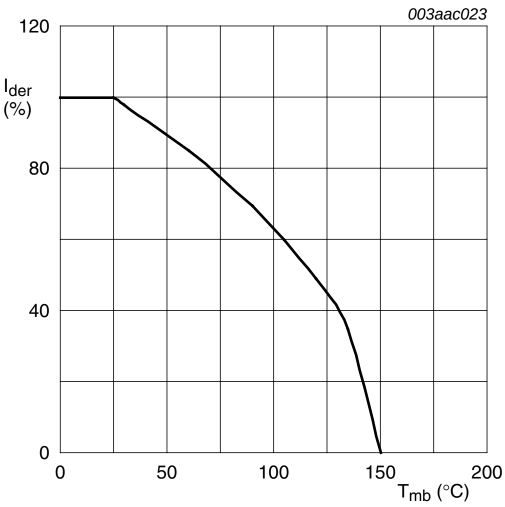
Type number	Package		
	Name	Description	Version
PSMN059-150Y	LFPAK	plastic single-ended surface-mounted package (LFPAK); 4 leads	SOT669

4. Limiting values

Table 4. Limiting values

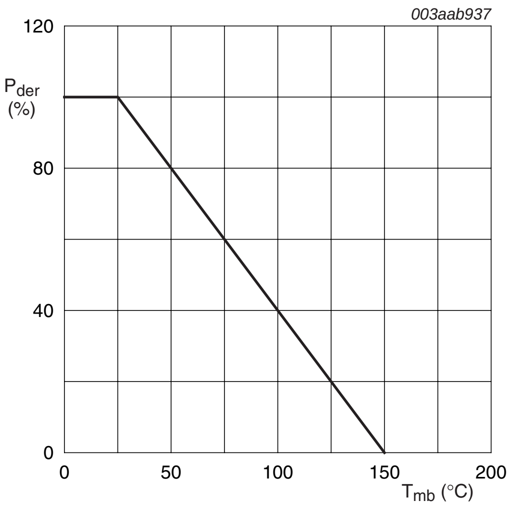
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25$ °C; $T_j \leq 150$ °C	-	150	V
V_{DGR}	drain-gate voltage	$T_j \geq 25$ °C; $T_j \leq 150$ °C; $R_{GS} = 20\ \Omega$	-	150	V
V_{GS}	gate-source voltage		-20	20	V
I_D	drain current	$V_{GS} = 10$ V; $T_{mb} = 25$ °C; see Figure 1; see Figure 3	-	43	A
		$V_{GS} = 10$ V; $T_{mb} = 100$ °C; see Figure 1	-	27.7	A
I_{DM}	peak drain current	pulsed; $t_p \leq 10$ µs; $T_{mb} = 25$ °C; see Figure 3	-	129	A
P_{tot}	total power dissipation	$T_{mb} = 25$ °C; see Figure 2	-	113	W
T_{stg}	storage temperature		-55	150	°C
T_j	junction temperature		-55	150	°C
Source-drain diode					
I_S	source current	$T_{mb} = 25$ °C	-	52	A
I_{SM}	peak source current	pulsed; $t_p \leq 10$ µs; $T_{mb} = 25$ °C	-	208	A
Avalanche ruggedness					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10$ V; $T_{j(init)} = 25$ °C; $I_D = 12.1$ A; $V_{sup} \leq 150$ V; unclamped; $t_p = 0.21$ ms; $R_{GS} = 50\ \Omega$	-	255	mJ



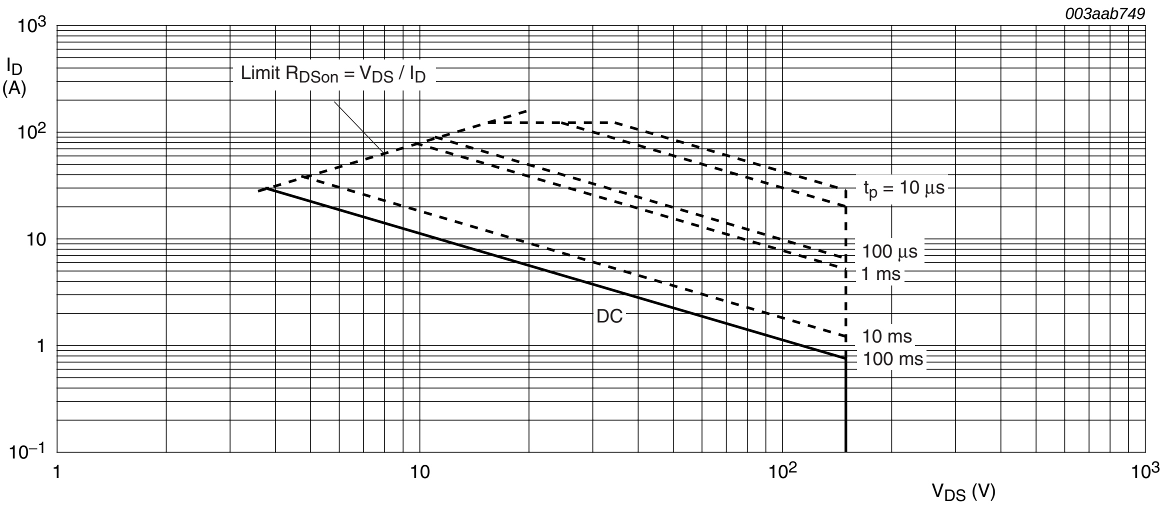
$$I_{der} = \frac{I_D}{I_{D(25°C)}} \times 100\,\%$$

Fig 1. Normalized continuous drain current as a function of mounting base temperature



$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\,\%$$

Fig 2. Normalized total power dissipation as a function of solder point temperature



$$T_{mb} = 25\,°C; I_{DM} \text{ is single pulse}$$

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	mounted on a printed-circuit board; vertical in still air; see Figure 4	-	-	1.1	K/W

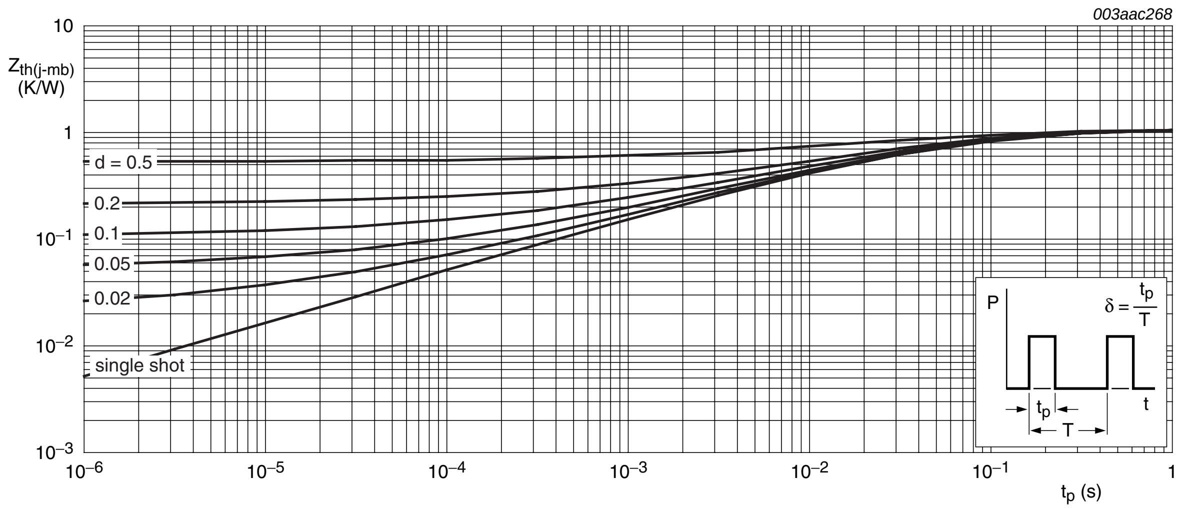
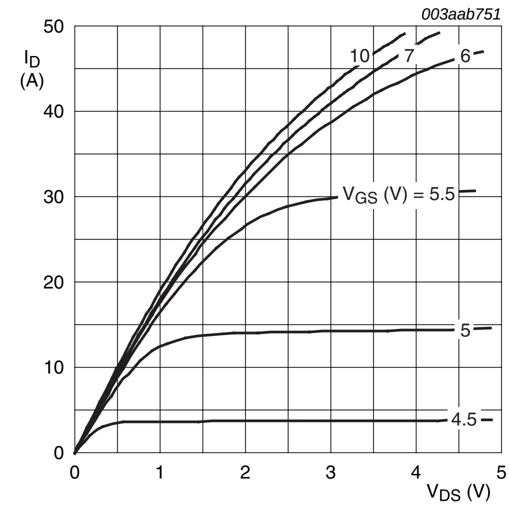


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

6. Characteristics

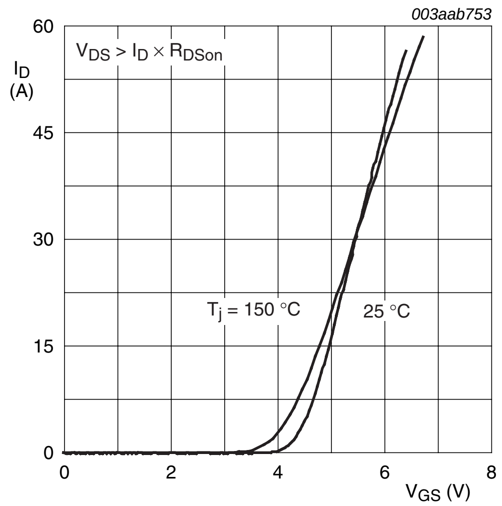
Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 µA; V_{GS} = 0 V; T_j = 25 °C	150	-	-	V
		I_D = 250 µA; V_{GS} = 0 V; T_j = -55 °C	133	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}; T_j = 25 °C; see Figure 7; see Figure 8	2	3	4	V
		I_D = 1 mA; V_{DS} = V_{GS}; T_j = 150 °C; see Figure 7; see Figure 8	1	-	-	V
		I_D = 1 mA; V_{DS} = V_{GS}; T_j = -55 °C; see Figure 7; see Figure 8	-	-	4.4	V
I_{DSS}	drain leakage current	V_{DS} = 120 V; V_{GS} = 0 V; T_j = 25 °C	-	-	1	µA
		V_{DS} = 120 V; V_{GS} = 0 V; T_j = 150 °C	-	-	100	µA
I_{GSS}	gate leakage current	V_{GS} = 20 V; V_{DS} = 0 V; T_j = 25 °C	-	-	100	nA
		V_{GS} = -20 V; V_{DS} = 0 V; T_j = 25 °C	-	-	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 12 A; T_j = 25 °C; see Figure 9; see Figure 10	-	46	59	mΩ
		V_{GS} = 10 V; I_D = 12 A; T_j = 150 °C; see Figure 9; see Figure 10	-	101	135	mΩ
R_G	gate resistance	f = 1 MHz	-	1.1	-	Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	I_D = 12 A; V_{DS} = 75 V; V_{GS} = 10 V; see Figure 11; see Figure 12	-	27.9	-	nC
Q_{GS}	gate-source charge		-	6.3	-	nC
Q_{GD}	gate-drain charge		-	9.1	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	I_D = 12 A; V_{DS} = 75 V; see Figure 11; see Figure 12	-	4.8	-	V
C_{iss}	input capacitance	V_{DS} = 30 V; V_{GS} = 0 V; f = 1 MHz; T_j = 25 °C; see Figure 13	-	1529	-	pF
C_{oss}	output capacitance		-	208	-	pF
C_{rss}	reverse transfer capacitance		-	66	-	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 75 V; R_L = 3 Ω; V_{GS} = 10 V; $R_{G(ext)}$ = 5.6 Ω	-	14.2	-	ns
t_r	rise time		-	42	-	ns
$t_{d(off)}$	turn-off delay time		-	54.2	-	ns
t_f	fall time		-	11.1	-	ns
Source-drain diode						
V_{SD}	source-drain voltage	I_S = 12 A; V_{GS} = 0 V; T_j = 25 °C; see Figure 14	-	0.9	1.2	V
t_{rr}	reverse recovery time	I_S = 12 A; dI_S/dt = -100 A/µs; V_{GS} = 0 V; V_{DS} = 30 V	-	114	-	ns
Q_r	recovered charge	I_S = 12 A; dI_S/dt = -100 A/µs; V_{GS} = 0 V	-	175	-	nC



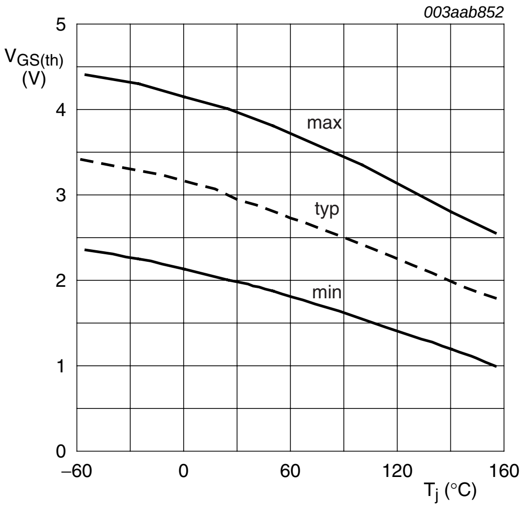
T_j = 25 °C

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values



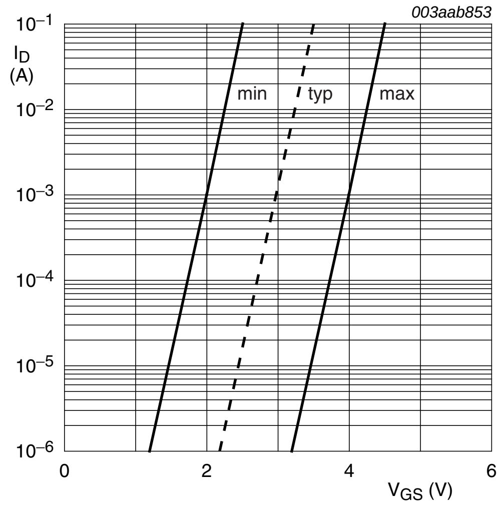
T_j = 25 °C and 150 °C; $V_{DS} > I_D \times R_{DSon}$

Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values



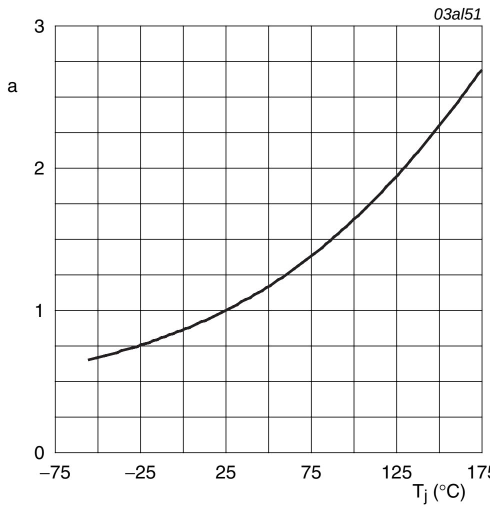
$I_D = 1mA; V_{DS} = V_{GS}$

Fig 7. Gate-source threshold voltage as a function of junction temperature



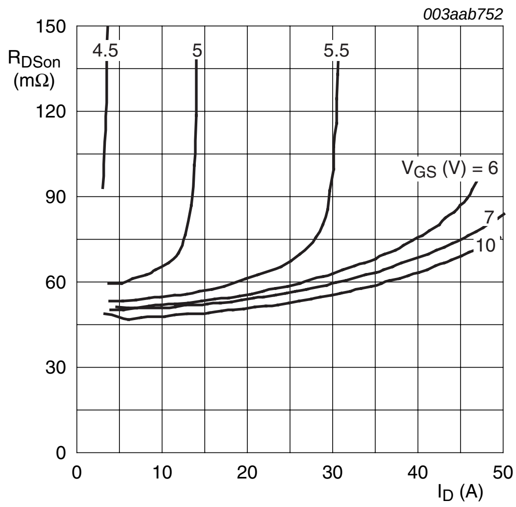
$T_j = 25°C; V_{DS} = 5V$

Fig 8. Sub-threshold drain current as a function of gate-source voltage



$$a = \frac{R_{DSon}}{R_{DSon(25°C)}}$$

Fig 9. Normalized drain-source on-state resistance factor as a function of junction temperature



$$T_j = 25°C$$

Fig 10. Drain-source on-state resistance as a function of drain current; typical values

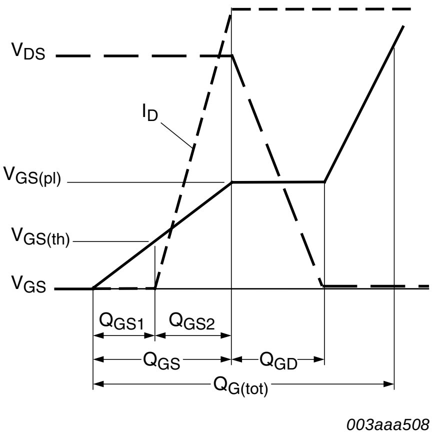
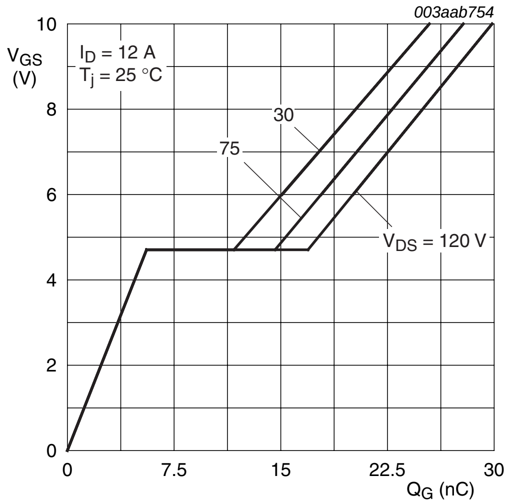
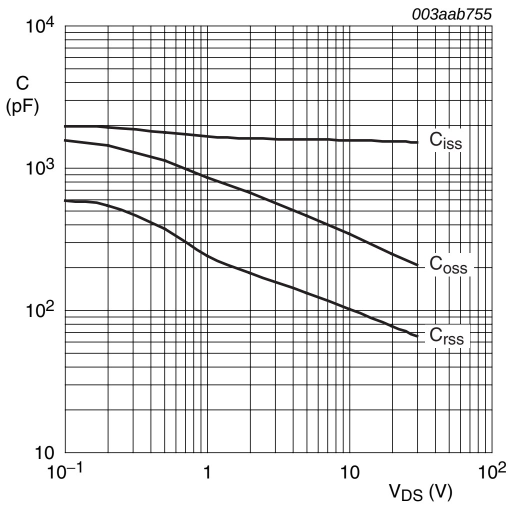


Fig 11. Gate charge waveform definitions



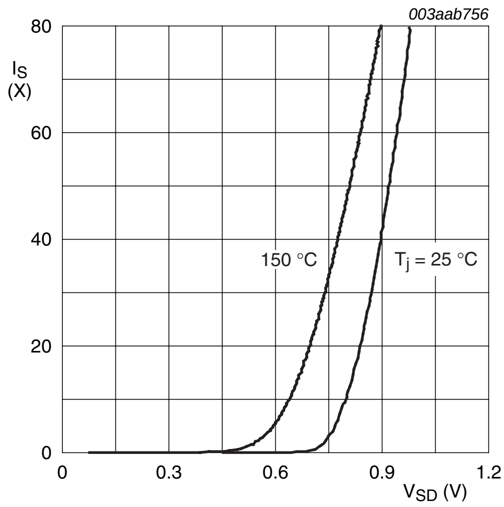
$$I_D = 12 A; V_{DS} = 30, 75 \, and \, 120 V$$

Fig 12. Gate-source voltage as a function of gate charge; typical values



$V_{GS} = 0V; f = 1MHz$

Fig 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

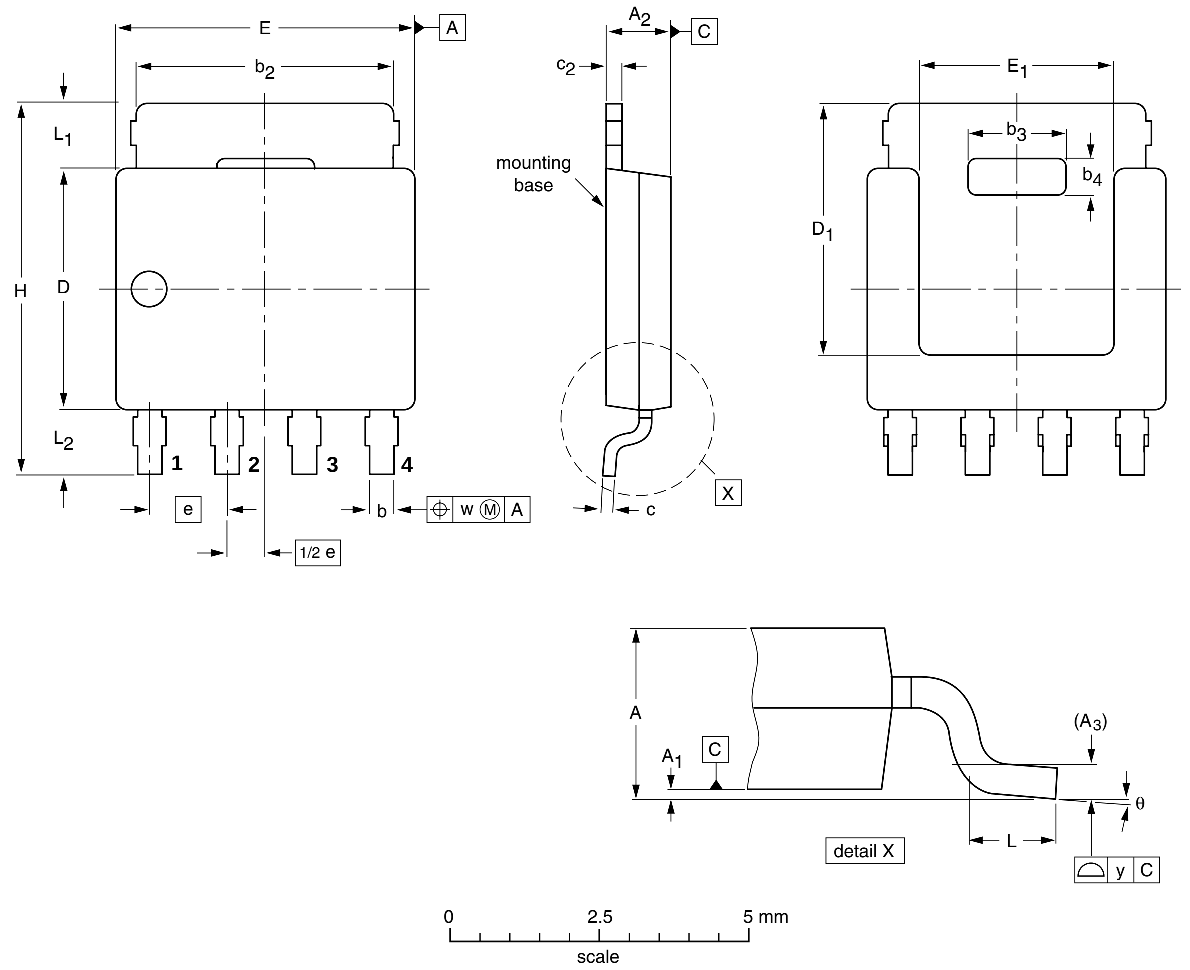


$T_j = 25°C$ and $150°C$; $V_{GS} = 0V$

Fig 14. Source current as a function of source-drain voltage; typical values

7. Package outline

Plastic single-ended surface-mounted package (LFPAK); 4 leads **SOT669**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	A_2	A_3	b	b_2	b_3	b_4	c	c_2	D(1)	D_1(1) max	E(1)	E_1(1)	e	H	L	L_1	L_2	w	y	θ
mm	1.20	0.15	1.10	0.25	0.50	4.41	2.2	0.9	0.25	0.30	4.10	4.20	5.0	3.3	1.27	6.2	0.85	1.3	1.3	0.25	0.1	8°
	1.01	0.00	0.95		0.35	3.62	2.0	0.7	0.19	0.24	3.80		4.8	3.1		5.8	0.40	0.8	0.8			0°

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT669		MO-235				~~04-10-13~~ 06-03-16

Fig 15. Package outline SOT669 (LFPAK)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PSMN059-150Y v.3	20110317	Product data sheet	-	PSMN059-150Y v.2
Modifications:	• Various changes to content.			
PSMN059-150Y v.2	20101220	Product data sheet	-	PSMN059-150Y v.1

9. Legal information

9.1 Data sheet status

Document status [1] [2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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