

74LVC2G04-Q100

Dual inverter

Rev. 6 — 15 August 2023

Product data sheet

1. General description

The 74LVC2G04-Q100 is a dual inverter. Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in mixed 3.3 V and 5 V environments.

Schmitt-trigger action at all inputs makes the circuit tolerant of slower input rise and fall times.

This device is fully specified for partial power-down applications using I_{OFF} . The I_{OFF} circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
 - Specified from -40 °C to +85 °C and -40 °C to +125 °C
- Wide supply voltage range from 1.65 V to 5.5 V
- Overvoltage tolerant inputs to 5.5 V
- High noise immunity
- ± 24 mA output drive ($V_{CC} = 3.0$ V)
- CMOS low power dissipation
- Direct interface with TTL levels
- I_{OFF} circuitry provides partial Power-down mode operation
- Latch-up performance exceeds 250 mA
- Complies with JEDEC standard:
 - JESD8-7 (1.65 V to 1.95 V)
 - JESD8-5 (2.3 V to 2.7 V)
 - JESD8C (2.7 V to 3.6 V)
 - JESD36 (4.6 V to 5.5 V)
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Multiple package options

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LVC2G04GW-Q100	-40 °C to +125 °C	TSSOP6	plastic thin shrink small outline package; 6 leads; body width 1.25 mm	SOT363-2
74LVC2G04GV-Q100	-40 °C to +125 °C	SC-74; TSOP6	plastic surface-mounted package; 6 leads	SOT457
74LVC2G04GS-Q100	-40 °C to +125 °C	XSON6	extremely thin small outline package; no leads; 6 terminals; body 1.0 × 1.0 × 0.35 mm	SOT1202

4. Marking

Table 2. Marking

Type number	Marking code [1]
74LVC2G04GW-Q100	V4
74LVC2G04GV-Q100	V04
74LVC2G04GS-Q100	V4

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

5. Functional diagram

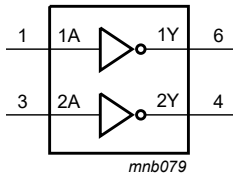


Fig. 1. Logic symbol

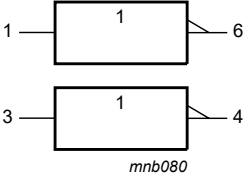


Fig. 2. IEC logic symbol

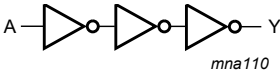
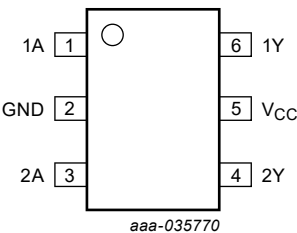


Fig. 3. Logic diagram (one gate)

6. Pinning information

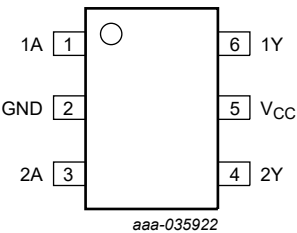
6.1. Pinning

GW package
SOT363-2 (TSSOP6)



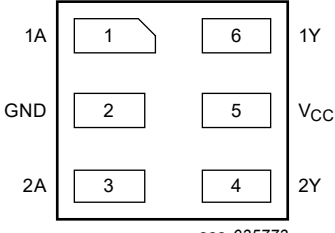
aaa-035770

GV package
SOT457 (SC-74; TSOP6)



aaa-035922

GS package
SOT1202 (XSON6)



aaa-035773

Transparent top view

6.2. Pin description

Table 3. Pin description

Symbol	Pin	Description
1A	1	data input
GND	2	ground (0 V)
2A	3	data input
2Y	4	data output
V _{CC}	5	supply voltage
1Y	6	data output

7. Functional description

Table 4. Function table

H = HIGH voltage level; L = LOW voltage level.

Input	Output
nA	nY
L	H
H	L

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+6.5	V
I _{IK}	input clamping current	V _I < 0 V	-50	-	mA
V _I	input voltage	[1]	-0.5	+6.5	V
I _{OK}	output clamping current	V _O > V _{CC} or V _O < 0 V	-	±50	mA
V _O	output voltage	Active mode [1]	-0.5	V _{CC} + 0.5	V
		Power-down mode; V _{CC} = 0 V [1]	-0.5	+6.5	V
I _O	output current	V _O = 0 V to V _{CC}	-	±50	mA
I _{CC}	supply current		-	100	mA
I _{GND}	ground current		-100	-	mA
P _{tot}	total power dissipation	T _{amb} = -40 °C to +125 °C [2]	-	250	mW
T _{stg}	storage temperature		-65	+150	°C

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
[2] For SOT363-2 (TSSOP6) package: P_{tot} derates linearly with 3.7 mW/K above 83 °C.
For SOT457 (SC-74; TSOP6) package: P_{tot} derates linearly with 4.1 mW/K above 89 °C.
For SOT1202 (XSON6) package: P_{tot} derates linearly with 3.3 mW/K above 74 °C.

9. Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		1.65	-	5.5	V
V_I	input voltage		0	-	5.5	V
V_O	output voltage	Active mode	0	-	V_{CC}	V
		Power-down mode; $V_{CC} = 0$ V	0	-	5.5	V
T_{amb}	ambient temperature		-40	-	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 1.65$ V to 2.7 V	-	-	20	ns/V
		$V_{CC} = 2.7$ V to 5.5 V	-	-	10	ns/V

10. Static characteristics

Table 7. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
V_{IH}	HIGH-level input voltage	$V_{CC} = 1.65$ V to 1.95 V	$0.65V_{CC}$	-	-	$0.65V_{CC}$	-	V
		$V_{CC} = 2.3$ V to 2.7 V	1.7	-	-	1.7	-	V
		$V_{CC} = 2.7$ V to 3.6 V	2.0	-	-	2.0	-	V
		$V_{CC} = 4.5$ V to 5.5 V	$0.7V_{CC}$	-	-	$0.7V_{CC}$	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 1.65$ V to 1.95 V	-	-	$0.35V_{CC}$	-	$0.35V_{CC}$	V
		$V_{CC} = 2.3$ V to 2.7 V	-	-	0.7	-	0.7	V
		$V_{CC} = 2.7$ V to 3.6 V	-	-	0.8	-	0.8	V
		$V_{CC} = 4.5$ V to 5.5 V	-	-	$0.3V_{CC}$	-	$0.3V_{CC}$	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}						
		$I_O = -100$ μ A; $V_{CC} = 1.65$ V to 5.5 V	$V_{CC} - 0.1$	-	-	$V_{CC} - 0.1$	-	V
		$I_O = -4$ mA; $V_{CC} = 1.65$ V	1.2	-	-	0.95	-	V
		$I_O = -8$ mA; $V_{CC} = 2.3$ V	1.9	-	-	1.7	-	V
		$I_O = -12$ mA; $V_{CC} = 2.7$ V	2.2	-	-	1.9	-	V
		$I_O = -24$ mA; $V_{CC} = 3.0$ V	2.3	-	-	2.0	-	V
		$I_O = -32$ mA; $V_{CC} = 4.5$ V	3.8	-	-	3.4	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}						
		$I_O = 100$ μ A; $V_{CC} = 1.65$ V to 5.5 V	-	-	0.10	-	0.10	V
		$I_O = 4$ mA; $V_{CC} = 1.65$ V	-	-	0.45	-	0.70	V
		$I_O = 8$ mA; $V_{CC} = 2.3$ V	-	-	0.30	-	0.45	V
		$I_O = 12$ mA; $V_{CC} = 2.7$ V	-	-	0.40	-	0.60	V
		$I_O = 24$ mA; $V_{CC} = 3.0$ V	-	-	0.55	-	0.80	V
		$I_O = 32$ mA; $V_{CC} = 4.5$ V	-	-	0.55	-	0.80	V
I_I	input leakage current	$V_I = 5.5$ V or GND; $V_{CC} = 0$ V to 5.5 V	-	± 0.1	± 1	-	± 1	μ A
I_{OFF}	power-off leakage current	$V_{CC} = 0$ V; V_I or $V_O = 5.5$ V	-	± 0.1	± 2	-	± 2	μ A

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
I_{CC}	supply current	$V_I = 5.5 \text{ V}$ or GND; $I_O = 0 \text{ A}$; $V_{CC} = 1.65 \text{ V}$ to 5.5 V	-	0.1	4	-	4	μA
ΔI_{CC}	additional supply current	per pin; $V_{CC} = 2.3 \text{ V}$ to 5.5 V ; $V_I = V_{CC} - 0.6 \text{ V}$; $I_O = 0 \text{ A}$	-	5	500	-	500	μA
C_I	input capacitance	$V_{CC} = 3.3 \text{ V}$; $V_I = \text{GND}$ to V_{CC}	-	2.5	-	-	-	pF

[1] All typical values are measured at $V_{CC} = 3.3 \text{ V}$ and $T_{amb} = 25 \text{ }^\circ\text{C}$.

11. Dynamic characteristics

Table 8. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 5.

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
t_{pd}	propagation delay	nA to nY; see Fig. 4 [2]						
		$V_{CC} = 1.65 \text{ V}$ to 1.95 V	1.0	3.5	8.0	1.0	9.5	ns
		$V_{CC} = 2.3 \text{ V}$ to 2.7 V	1.0	2.2	4.4	1.0	5.4	ns
		$V_{CC} = 2.7 \text{ V}$	1.0	2.7	5.2	1.0	7.0	ns
		$V_{CC} = 3.0 \text{ V}$ to 3.6 V	0.5	2.7	4.1	0.5	5.5	ns
		$V_{CC} = 4.5 \text{ V}$ to 5.5 V	1.0	1.9	3.2	1.0	3.8	ns
C_{PD}	power dissipation capacitance	$V_I = \text{GND}$ to V_{CC} ; $V_{CC} = 3.3 \text{ V}$ [3]	-	13.5	-	-	-	pF

[1] Typical values are measured at $T_{amb} = 25 \text{ }^\circ\text{C}$ and $V_{CC} = 1.8 \text{ V}$, 2.5 V , 2.7 V , 3.3 V and 5.0 V respectively.

[2] t_{pd} is the same as t_{PLH} and t_{PHL} .

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum (C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

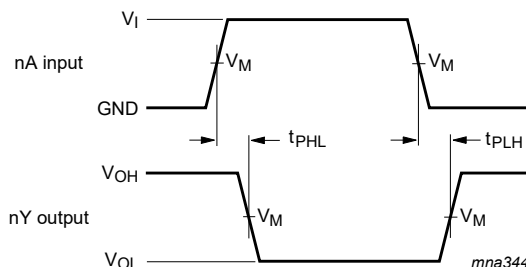
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

$\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

11.1. Waveforms and test circuit



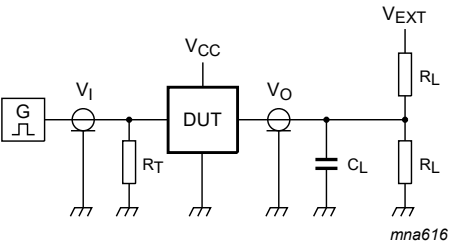
Measurement points are given in Table 9.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 4. The input nA to output nY propagation delays

Table 9. Measurement points

Supply voltage	Input	Output
V _{CC}	V _M	V _M
1.65 V to 1.95 V	0.5V _{CC}	0.5V _{CC}
2.3 V to 2.7 V	0.5V _{CC}	0.5V _{CC}
2.7 V	1.5 V	1.5 V
3.0 V to 3.6 V	1.5 V	1.5 V
4.5 V to 5.5 V	0.5V _{CC}	0.5V _{CC}



Test data is given in [Table 10](#).
Definitions for test circuit:
 R_L = Load resistance;
 C_L = Load capacitance including jig and probe capacitance;
 R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator;
 V_{EXT} = External voltage for measuring switching times.

Fig. 5. Test circuit for measuring switching times

Table 10. Test data

Supply voltage	Input		Load		V _{EXT}
V _{CC}	V _I	t _r = t _f	C _L	R _L	t _{PLH} , t _{PHL}
1.65 V to 1.95 V	V _{CC}	≤ 2.0 ns	30 pF	1 kΩ	open
2.3 V to 2.7 V	V _{CC}	≤ 2.0 ns	30 pF	500 Ω	open
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open
4.5 V to 5.5 V	V _{CC}	≤ 2.5 ns	50 pF	500 Ω	open

12. Package outline

TSSOP6: plastic thin shrink small outline package; 6 leads; body width 1.25 mm

SOT363-2

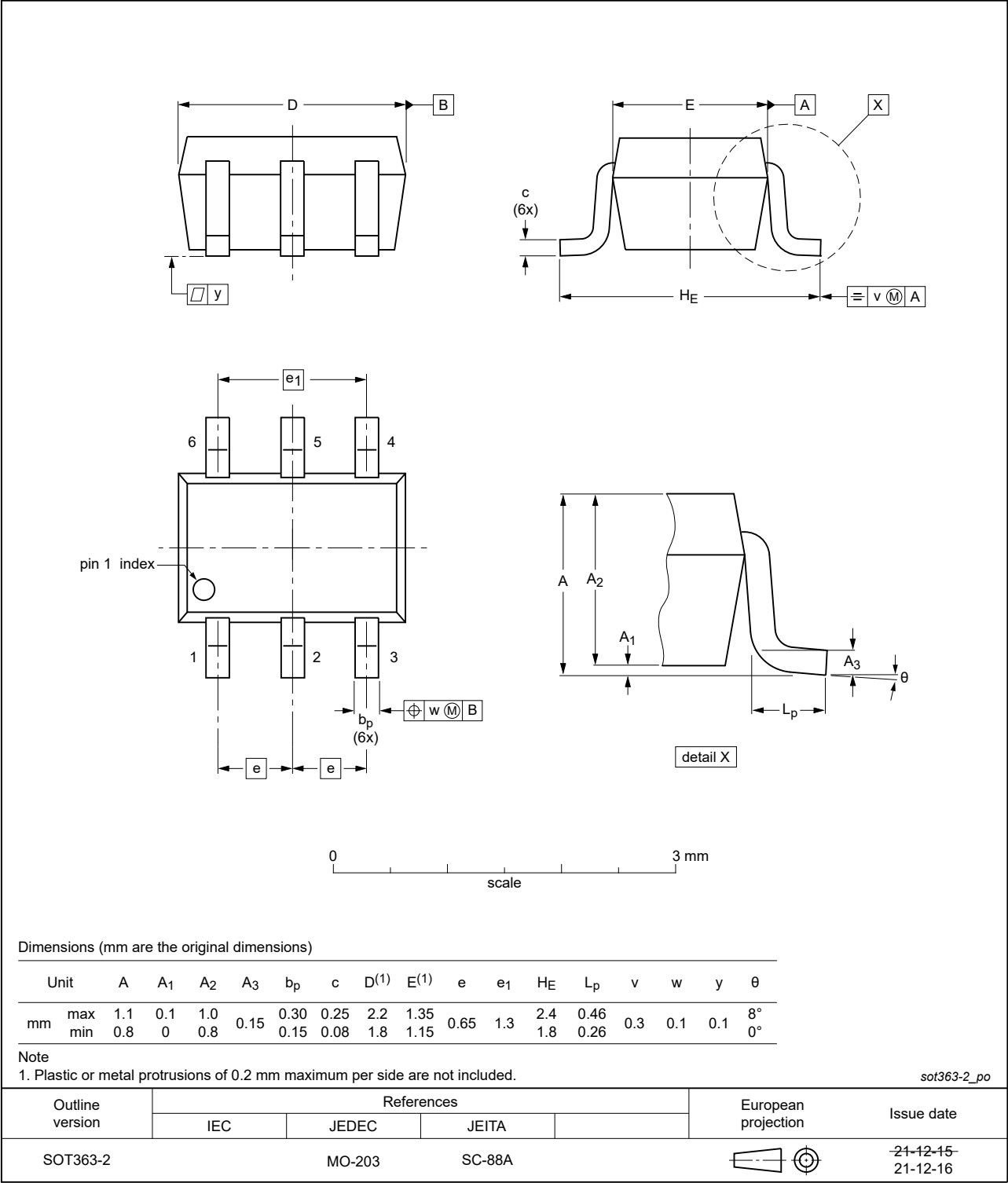


Fig. 6. Package outline SOT363-2 (TSSOP6)

Plastic, surface-mounted package (SC-74; TSOP6); 6 leads

SOT457

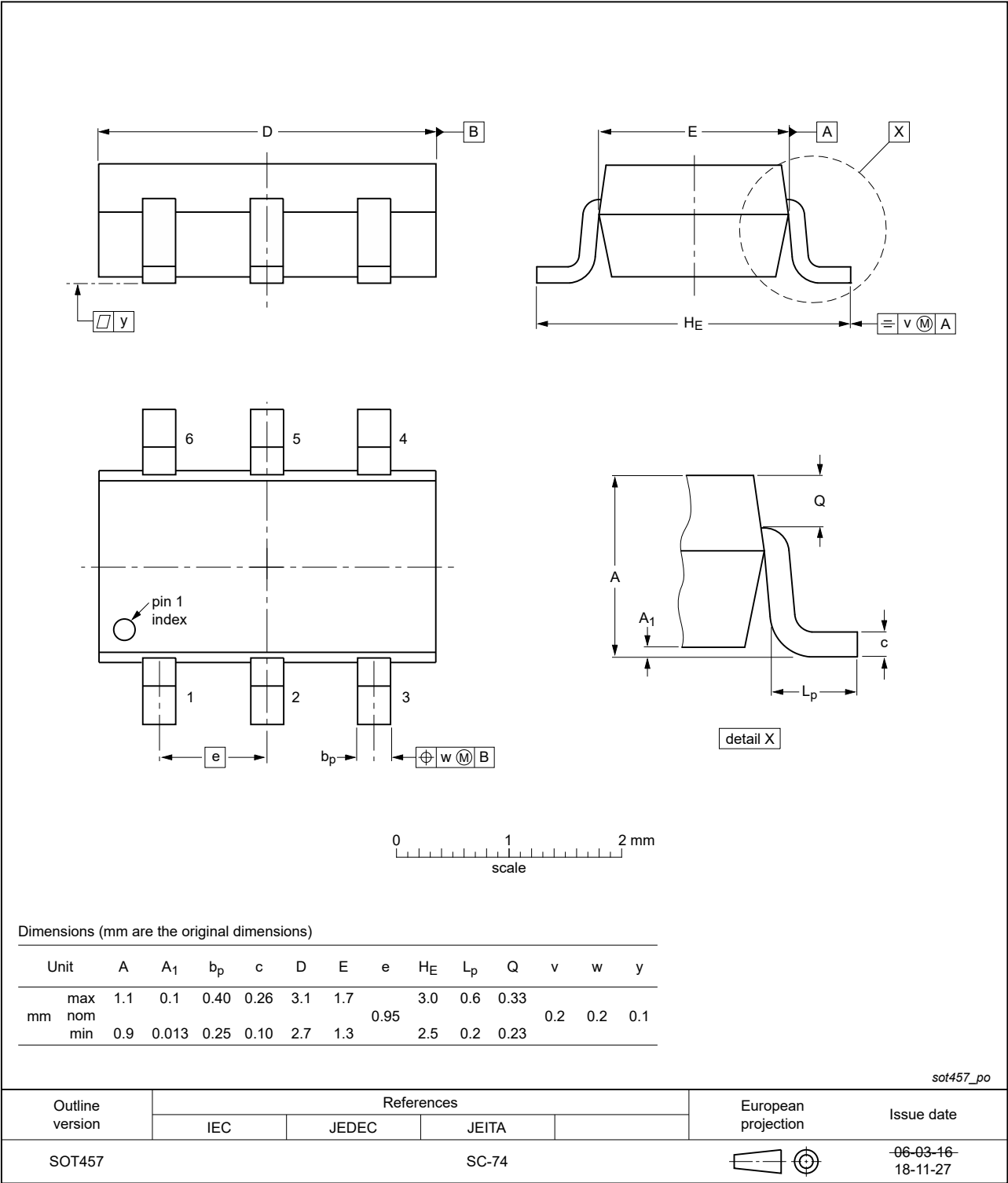


Fig. 7. Package outline SOT457 (SC-74; TSOP6)

XSON6: extremely thin small outline package; no leads;
6 terminals; body 1.0 x 1.0 x 0.35 mm

SOT1202

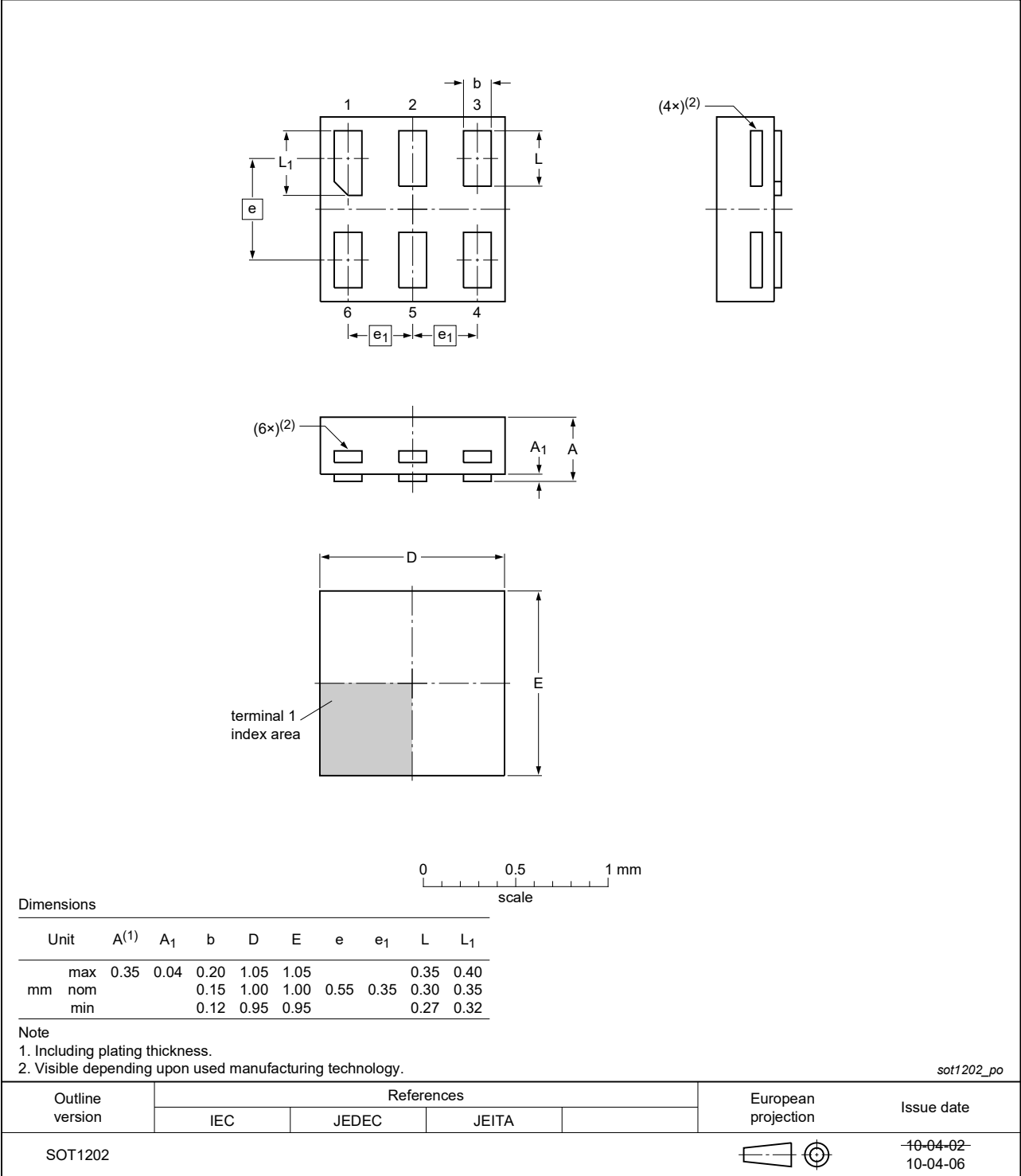


Fig. 8. Package outline SOT1202 (XSON6)

13. Abbreviations

Table 11. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC2G04_Q100 v.6	20230815	Product data sheet	-	74LVC2G04_Q100 v.5
Modifications:	Section 2: ESD specification updated according to the latest JEDEC standard.			
74LVC2G04_Q100 v.5	20220126	Product data sheet	-	74LVC2G04_Q100 v.4
Modifications:	Package SOT363 (SC-88) changed to SOT363-2 (TSSOP6).			
74LVC2G04_Q100 v.4	20210929	Product data sheet	-	74LVC2G04_Q100 v.3
Modifications:	- Table 5: Derating values for P_{tot} total power dissipation updated. - Section 1 and Section 2 updated.			
74LVC2G04_Q100 v.3	20190125	Product data sheet	-	74LVC2G04_Q100 v.2
Modifications:	- The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. - Legal texts have been adapted to the new company name where appropriate. - Pin 6 description updated. Section 6.2 - Added type number 74LVC2G04GS-Q100 (SOT1202/XSON6). - Fig. 7: Package outline drawing SOT457 updated.			
74LVC2G04_Q100 v.2	20161213	Product data sheet	-	74LVC2G04_Q100 v.1
Modifications:	Table 7: The maximum limits for leakage current and supply current have changed.			
74LVC2G04_Q100 v.1	20140520	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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