

FEATURES

- **Guaranteed Offset Voltage:** 150 μ V Max
–55°C to 125°C: 500 μ V Max
- **Guaranteed Drift:** 4 μ V/°C Max
- **Guaranteed Bias Current**
70°C: 150pA Max
125°C: 2.5nA Max
- **Guaranteed Slew Rate:** 12V/ μ s Min
- Available in 8-Pin PDIP and SO Packages

APPLICATIONS

- Precision, High Speed Instrumentation
- Logarithmic Amplifiers
- D/A Output Amplifiers
- Photodiode Amplifiers
- Voltage-to-Frequency Converters
- Frequency-to-Voltage Converters
- Fast, Precision Sample-and-Hold

DESCRIPTION

The LT[®]1055/LT1056 JFET input operational amplifiers combine precision specifications with high speed performance.

For the first time, 16V/ μ s slew rate and 6.5MHz gain bandwidth product are simultaneously achieved with offset voltage of typically 50 μ V, 1.2 μ V/°C drift, bias currents of 40pA at 70°C and 500pA at 125°C.

The 150 μ V maximum offset voltage specification is the best available on any JFET input operational amplifier.

The LT1055 and LT1056 are differentiated by their operating currents. The lower power dissipation LT1055 achieves lower bias and offset currents and offset voltage. The additional power dissipation of the LT1056 permits higher slew rate, bandwidth and faster settling time with a slight sacrifice in DC performance.

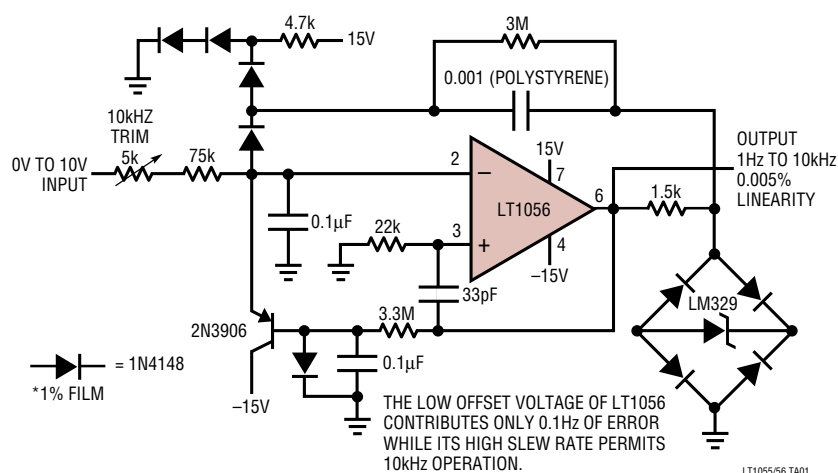
The voltage-to-frequency converter shown below is one of the many applications which utilize both the precision and high speed of the LT1055/LT1056.

For a JFET input op amp with 23V/ μ s guaranteed slew rate, refer to the LT1022 data sheet.

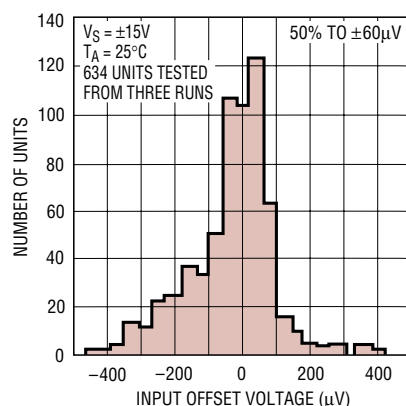
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TYPICAL APPLICATION

1Hz to 10kHz Voltage-to-Frequency Converter



Distribution of Input Offset Voltage (H Package)



LT1055/LT1056

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage	$\pm 20V$
Differential Input Voltage	$\pm 40V$
Input Voltage	$\pm 20V$
Output Short-Circuit Duration	Indefinite
Operating Temperature Range	
LT1055AM/LT1055M/LT1056AM/ LT1056M (OBSOLETE)	$-55^{\circ}C$ to $125^{\circ}C$

LT1055AC/LT1055C/LT1056AC/ LT1056C	$0^{\circ}C$ to $70^{\circ}C$
Storage Temperature Range	
All Devices	$-65^{\circ}C$ to $150^{\circ}C$
Lead Temperature (Soldering, 10 sec)	$300^{\circ}C$

PACKAGE/ORDER INFORMATION

TOP VIEW N8 PACKAGE 8-LEAD PDIP $T_{JMAX} = 150^{\circ}C$, $\theta_{JA} = 130^{\circ}C/W$	ORDER PART NUMBER LT1055CN8 LT1056CN8	TOP VIEW S8 PACKAGE 8-LEAD PLASTIC SO $T_{JMAX} = 150^{\circ}C$, $\theta_{JA} = 150^{\circ}C/W$	ORDER PART NUMBER LT1055S8 LT1056S8 S8 PART MARKING 1055 1056								
TOP VIEW H PACKAGE 8-LEAD TO-5 METAL CAN $T_{JMAX} = 150^{\circ}C$, $\theta_{JA} = 150^{\circ}C/W$, $\theta_{JC} = 45^{\circ}C/W$	ORDER PART NUMBER <table><tr><td>LT1055ACH</td><td>LT1056ACH</td></tr><tr><td>LT1055CH</td><td>LT1056CH</td></tr><tr><td>LT1055AMH</td><td>LT1056AMH</td></tr><tr><td>LT1055MH</td><td>LT1056MH</td></tr></table> OBSOLETE PACKAGE Consider the N8 Package for Alternate Source			LT1055ACH	LT1056ACH	LT1055CH	LT1056CH	LT1055AMH	LT1056AMH	LT1055MH	LT1056MH
LT1055ACH	LT1056ACH										
LT1055CH	LT1056CH										
LT1055AMH	LT1056AMH										
LT1055MH	LT1056MH										
Order Options Tape and Reel: Add #TR Lead Free: Add #PBF Lead Free Tape and Reel: Add #TRPBF Lead Free Part Marking: http://www.linear.com/leadfree/											

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS $T_A = 25^{\circ}C$, $V_S = \pm 15V$, $V_{CM} = 0V$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1055AM/LT1056AM LT1055AC/LT1056AC			LT1055M/LT1056M LT1055CH/LT1056CH LT1055CN8/LT1056CN8			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage (Note 2)	LT1055 H Package	—	50	150	—	70	400	μV
		LT1056 H Package	—	50	180	—	70	450	μV
		LT1055 N8 Package	—	—	—	—	120	700	μV
		LT1056 N8 Package	—	—	—	—	140	800	μV
I_{OS}	Input Offset Current	Fully Warm Up	—	2	10	—	2	20	pA

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ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$. $V_S = \pm 15\text{V}$, $V_{CM} = 0\text{V}$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1055AM/LT1056AM LT1055AC/LT1056AC			LT1055M/LT1056M LT1055CH/LT1056CH LT1055CN8/LT1056CN8			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
I_B	Input Bias Current	Fully Warmed Up $V_{CM} = 10\text{V}$	—	± 10	± 50	—	± 10	± 50	pA
			—	30	130	—	30	150	pA
	Input Resistance: Differential	Common Mode $V_{CM} = -11\text{V}$ to 8V $V_{CM} = 8\text{V}$ to 11V	—	10^{12}	—	—	10^{12}	—	Ω
			—	10^{12}	—	—	10^{12}	—	Ω
			—	10^{11}	—	—	10^{11}	—	Ω
	Input Capacitance		—	4	—	—	4	—	pF
e_n	Input Noise Voltage	0.1Hz to 10Hz LT1055 LT1056	—	1.8	—	—	2.0	—	μV_{P-P}
			—	2.5	—	—	2.8	—	μV_{P-P}
	Input Noise Voltage Density	$f_0 = 10\text{Hz}$ (Note 3)	—	28	50	—	30	60	$\text{nV}/\sqrt{\text{Hz}}$
		$f_0 = 1\text{kHz}$ (Note 4)	—	14	20	—	15	22	$\text{nV}/\sqrt{\text{Hz}}$
I_n	Input Noise Current Density	$f_0 = 10\text{Hz}, 1\text{kHz}$ (Note 5)	—	1.8	4	—	1.8	4	$\text{fA}/\sqrt{\text{Hz}}$
A_{VOL}	Large-Signal Voltage Gain	$V_0 = \pm 10\text{V}$ $R_L = 2\text{k}$	150	400	—	120	400	—	V/mV
		$R_L = 1\text{k}$	130	300	—	100	300	—	V/mV
	Input Voltage Range		± 11	± 12	—	± 11	± 12	—	V
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 11\text{V}$	86	100	—	83	98	—	dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 10\text{V}$ to $\pm 18\text{V}$	90	106	—	88	104	—	dB
V_{OUT}	Output Voltage Swing	$R_L = 2\text{k}$	± 12	± 13.2	—	± 12	± 13.2	—	V
SR	Slew Rate	LT1055	10	13	—	7.5	12	—	V/ μs
		LT1056	12	16	—	9.0	14	—	V/ μs
GBW	Gain Bandwidth Product	$f = 1\text{MHz}$ LT1055	—	5.0	—	—	4.5	—	MHz
		LT1056	—	6.5	—	—	5.5	—	MHz
I_S	Supply Current	LT1055	—	2.8	4.0	—	2.8	4.0	mA
		LT1056	—	5.0	6.5	—	5.0	7.0	mA
	Offset Voltage Adjustment Range	$R_{POT} = 100\text{k}$	—	± 5	—	—	± 5	—	mV

The ● denotes the specifications which apply over the temperature range $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$. $V_S = \pm 15\text{V}$, $V_{CM} = 0\text{V}$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LT1055AC LT1056AC			LT1055CH/LT1056CH LT1055CN8/LT1056CN8			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage (Note 2)	LT1055 H Package	●	—	100	330	—	140	750	μV
		LT1056 H Package	●	—	100	360	—	140	800	μV
		LT1055 N8 Package	●	—	—	—	—	250	1250	μV
		LT1056 N8 Package	●	—	—	—	—	280	1350	μV
	Average Temperature Coefficient of Input Offset Voltage	H Package (Note 6)	●	—	1.2	4.0	—	1.6	8.0	$\mu\text{V}/^\circ\text{C}$
		N8 Package (Note 6)	●	—	—	—	—	3.0	12.0	$\mu\text{V}/^\circ\text{C}$
I_{OS}	Input Offset Current	Warmed Up LT1055	●	—	10	50	—	16	80	pA
		$T_A = 70^\circ\text{C}$ LT1056	●	—	14	70	—	18	100	pA
I_B	Input Bias Current	Warmed Up LT1055	●	—	± 30	± 150	—	± 40	± 200	pA
		$T_A = 70^\circ\text{C}$ LT1056	●	—	± 40	± 80	—	± 50	± 240	pA
A_{VOL}	Large-Signal Voltage Gain	$V_0 = \pm 10\text{V}$, $R_L = 2\text{k}$	●	80	250	—	60	250	—	V/mV
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 10.5\text{V}$	●	85	100	—	82	98	—	dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 10\text{V}$ to $\pm 18\text{V}$	●	89	105	—	87	103	—	dB
V_{OUT}	Output Voltage Swing	$R_L = 2\text{k}$	●	± 12	± 13.1	—	± 12	± 13.1	—	V

LT1055/LT1056

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the temperature range $-55^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$. $V_S = \pm 15\text{V}$, $V_{CM} = 0\text{V}$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LT1055AM LT1056AM			LT1055M LT1056M			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage (Note 2)	LT1055 LT1056	●	—	180	500	—	250	1200	μV
			●	—	180	550	—	250	1250	μV
	Average Temperature Coefficient of Input Offset Voltage	(Note 6)	●	—	1.3	4.0	—	1.8	8.0	$\mu\text{V}/^{\circ}\text{C}$
I_{OS}	Input Offset Current	Warmed Up $T_A = 125^{\circ}\text{C}$	●	—	0.20	1.2	—	0.25	1.8	nA
			●	—	0.25	1.5	—	0.30	2.4	nA
I_B	Input Bias Current	Warmed Up $T_A = 125^{\circ}\text{C}$	●	—	± 0.4	± 2.5	—	± 0.5	± 4.0	nA
			●	—	± 0.5	± 3.0	—	± 0.6	± 5.0	nA
A_{VOL}	Large-Signal Voltage Gain	$V_O = \pm 10\text{V}$, $R_L = 2\text{k}$	●	40	120	—	35	120	—	V/mV
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 10.5\text{V}$	●	85	100	—	82	98	—	dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 10\text{V}$ to $\pm 17\text{V}$	●	88	104	—	86	102	—	dB
V_{OUT}	Output Voltage Swing	$R_L = 2\text{k}$	●	± 12	± 12.9	—	± 12	± 12.9	—	V

$T_A = 25^{\circ}\text{C}$. $V_S = \pm 15\text{V}$, $V_{CM} = 0\text{V}$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LT1055CS8/LT1056CS8			UNITS
				MIN	TYP	MAX	
V_{OS}	Input Offset Voltage (Note 2)				500	1500	μV
I_{OS}	Input Offset Current	Fully Warmed Up			5	30	pA
I_B	Input Bias Current	Fully Warmed Up $V_{CM} = 10\text{V}$			± 30	± 100	pA
					30	150	pA
	Input Resistance Differential Common Mode	$V_{CM} = -11\text{V}$ to 8V $V_{CM} = 8\text{V}$ to 11V			0.4		$\text{T}\Omega$
					0.4		$\text{T}\Omega$
					0.05		$\text{T}\Omega$
	Input Capacitance				4		pF
e_n	Input Noise Voltage	0.1Hz to 10Hz LT1055 LT1056			2.5		μV_{P-P}
					3.5		μV_{P-P}
	Input Noise Voltage Density	$f_0 = 10\text{Hz}$ (Note 4) $f_0 = 1\text{kHz}$ (Note 4)			35	70	nV/ $\sqrt{\text{Hz}}$
					15	22	nV/ $\sqrt{\text{Hz}}$
i_n	Input Noise Current Density	$f_0 = 10\text{Hz}$, 1kHz (Note 5)			2.5	10	fA/ $\sqrt{\text{Hz}}$
A_{VOL}	Large-Signal Voltage Gain	$V_O = \pm 10\text{V}$ $R_L = 2\text{k}$ $R_L = 1\text{k}$			120	400	V/mV
					100	300	V/mV
	Input Voltage Range				± 11	± 12	V
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 11\text{V}$			83	98	dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 10\text{V}$ to $\pm 18\text{V}$			88	104	dB
V_{OUT}	Output Voltage Swing	$R_L = 2\text{k}$			± 12	± 13.2	V
SR	Slew Rate	LT1055 LT1056			7.5	12	V/ μs
					9.0	14	V/ μs
GBW	Gain Bandwidth Product	$f = 1\text{MHz}$ LT1055 LT1056			4.5		MHz
					5.5		MHz
I_S	Supply Current	LT1055 LT1056			2.8	4.0	mA
					5.0	7.0	mA
	Offset Voltage Adjustment Range	$R_{POT} = 100\text{k}$			± 5		mV

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ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the temperature range $0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$. $V_S = \pm 15\text{V}$, $V_{CM} = 0\text{V}$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LT1055CS8/LT1056CS8			UNITS
				MIN	TYP	MAX	
V_{OS}	Input Offset Voltage (Note 2)		●		800	2200	μV
	Average Temperature Coefficient of Input Offset Voltage		●		4	15	$\mu\text{V}/^{\circ}\text{C}$
I_{OS}	Input Offset Current	Warmed Up, $T_A = 70^{\circ}\text{C}$	●		18	150	pA
I_B	Input Bias Current	Warmed Up, $T_A = 70^{\circ}\text{C}$	●		± 60	± 400	pA
A_{VOL}	Large-Signal Voltage Gain	$V_O = \pm 10\text{V}$, $R_L = 2\text{k}$	●	60	250		V/mV
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 10.5\text{V}$	●	82	98		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 10\text{V}$ to $\pm 18\text{V}$	●	87	103		dB
V_{OUT}	Output Voltage Swing	$R_L = 2\text{k}$	●	± 12	± 13.1		V

For MIL-STD components, please refer to LTC883 data sheet for test listing and parameters.

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Offset voltage is measured under two different conditions: (a) approximately 0.5 seconds after application of power; (b) at $T_A = 25^{\circ}\text{C}$ only, with the chip heated to approximately 38°C for the LT1055 and to 45°C for the LT1056, to account for chip temperature rise when the device is fully warmed up.

Note 3: 10Hz noise voltage density is sample tested on every lot of A grades. Devices 100% tested at 10Hz are available on request.

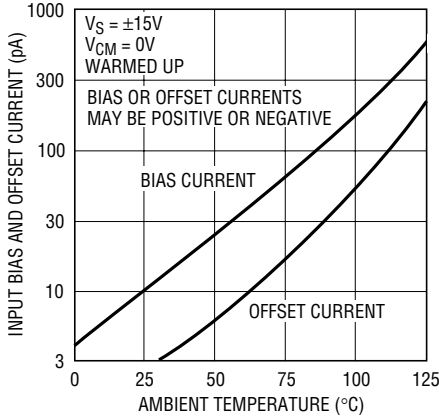
Note 4: This parameter is tested on a sample basis only.

Note 5: Current noise is calculated from the formula: $i_n = (2qI_B)^{1/2}$, where $q = 1.6 \cdot 10^{-19}$ coulomb. The noise of source resistors up to $1\text{G}\Omega$ swamps the contribution of current noise.

Note 6: Offset voltage drift with temperature is practically unchanged when the offset voltage is trimmed to zero with a 100k potentiometer between the balance terminals and the wiper tied to V^+ . Devices tested to tighter drift specifications are available on request.

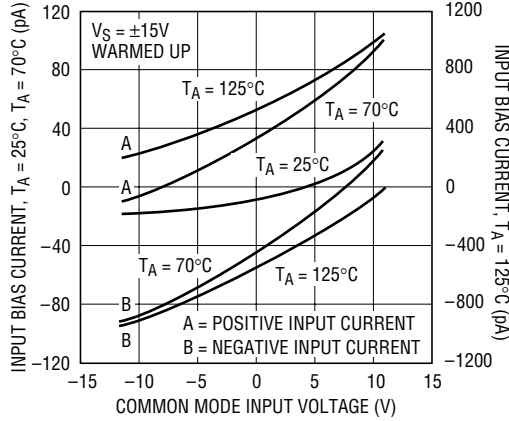
TYPICAL PERFORMANCE CHARACTERISTICS

Input Bias and Offset Currents vs Temperature



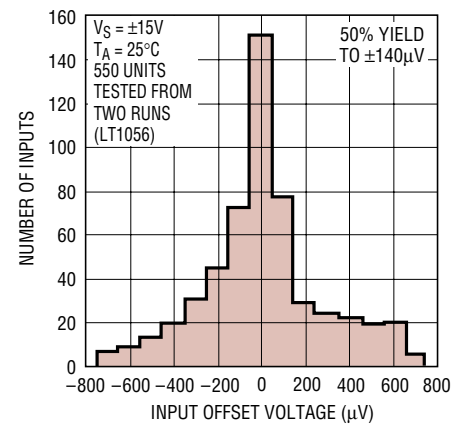
LT1055/56 G01

Input Bias Current Over the Common Mode Range



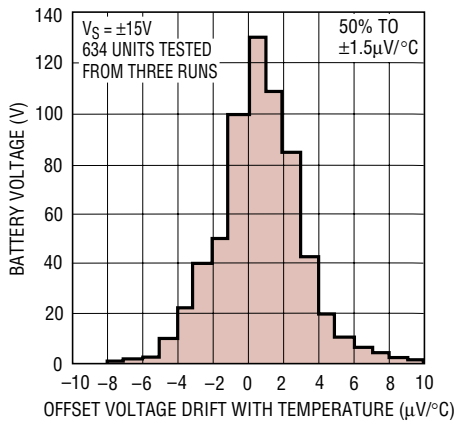
LT1055/56 G02

Distribution of Input Offset Voltage (N8 Package)



LT1055/56 G03

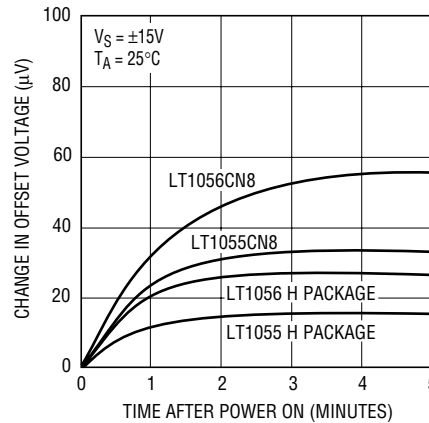
Distribution of Offset Voltage Drift with Temperature (H Package)*



*DISTRIBUTION IN THE PLASTIC (N8) PACKAGE IS SIGNIFICANTLY WIDER.

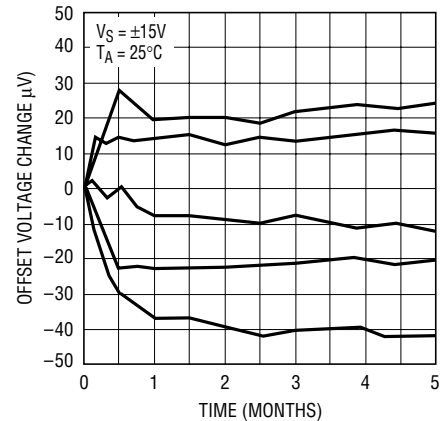
LT1055/56 G04

Warm-Up Drift



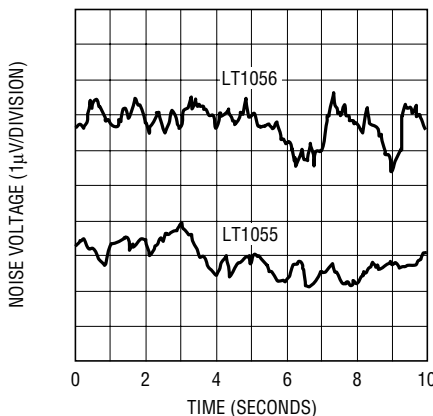
LT1055/56 G05

Long Term Drift of Representative Units



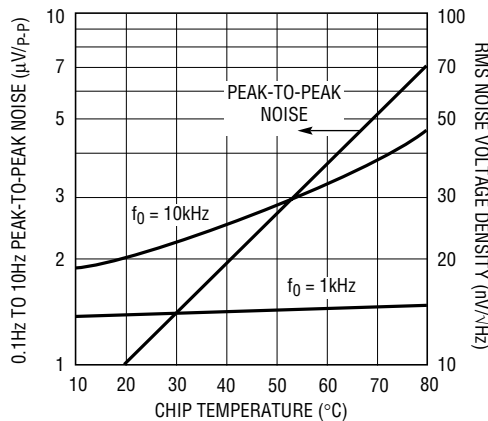
LT1055/56 G06

0.1Hz to 10Hz Noise



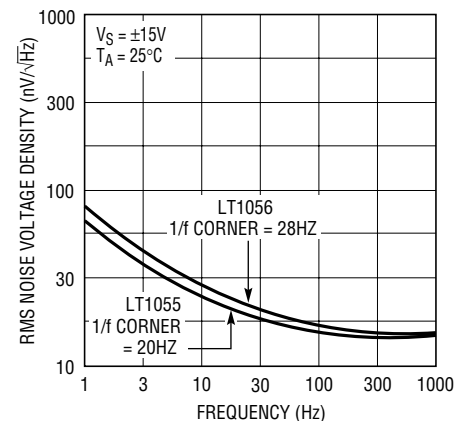
LT1055/56 G07

Noise vs Chip Temperature



LT1055/56 G08

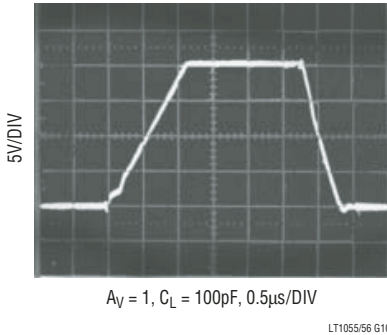
Voltage Noise vs Frequency



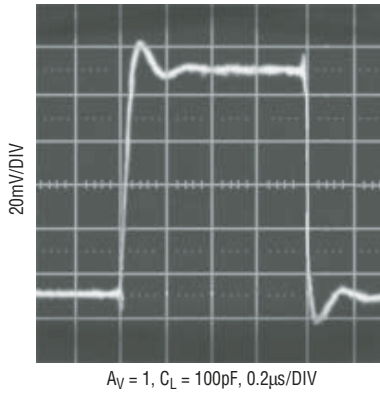
LT1055/56 G09

TYPICAL PERFORMANCE CHARACTERISTICS

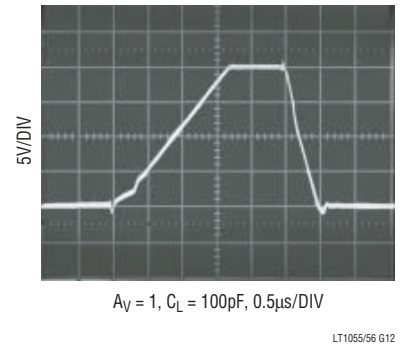
LT1056 Large-Signal Response



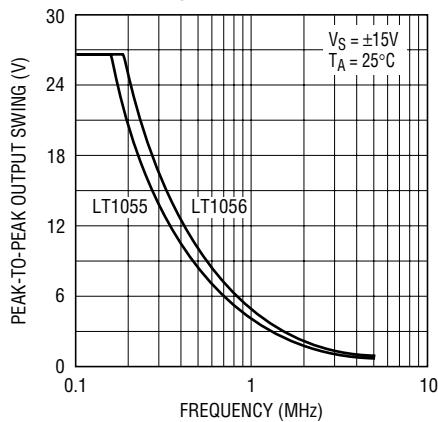
Small-Signal Response



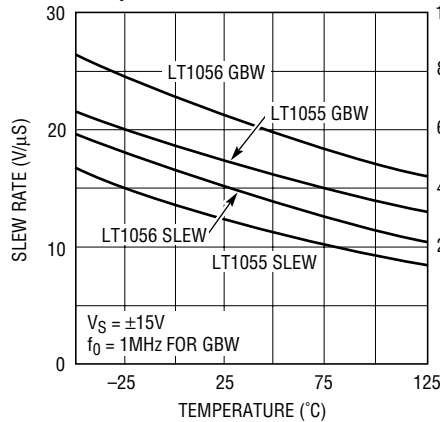
LT1055 Large-Signal Response



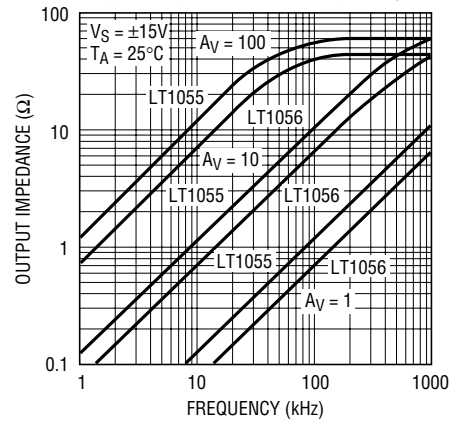
Undistorted Output Swing vs Frequency



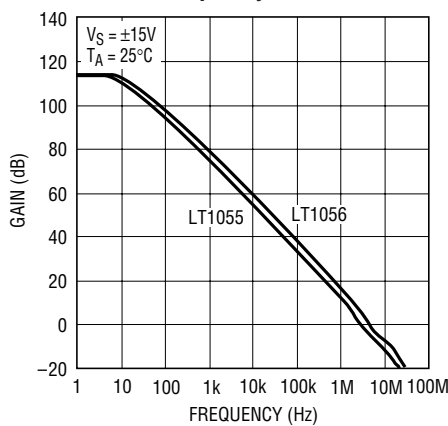
Slew Rate, Gain Bandwidth vs Temperature



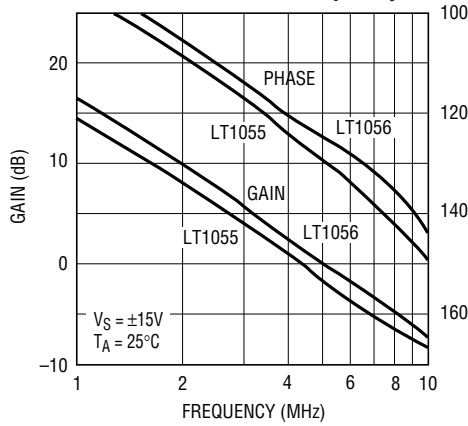
Output Impedance vs Frequency



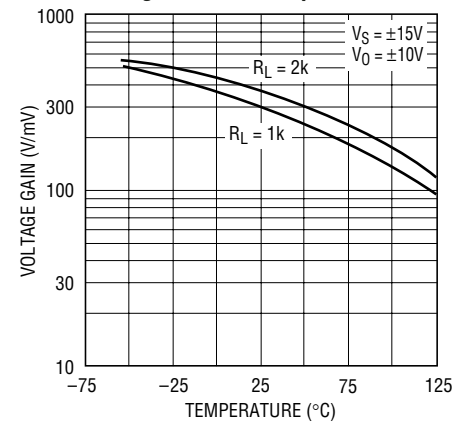
Gain vs Frequency



Gain, Phase Shift vs Frequency

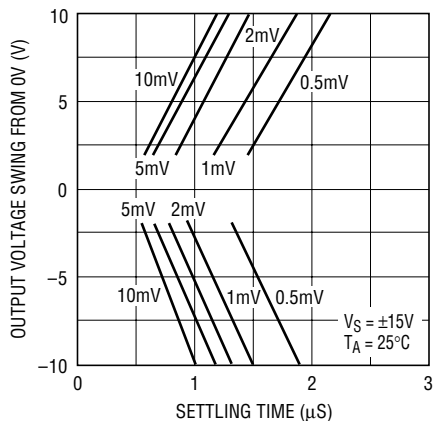


Voltage Gain vs Temperature



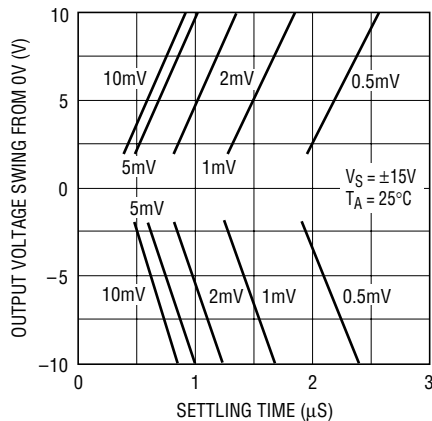
TYPICAL PERFORMANCE CHARACTERISTICS

LT1055 Settling Time



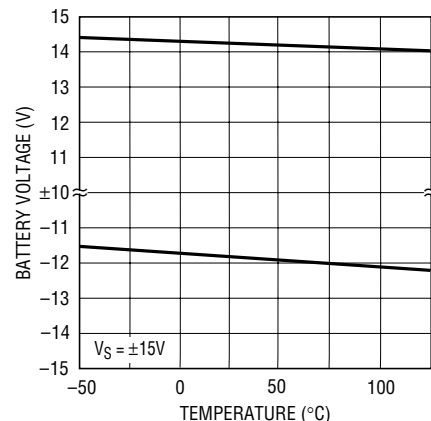
LT1055/56 G19

LT1056 Settling Time



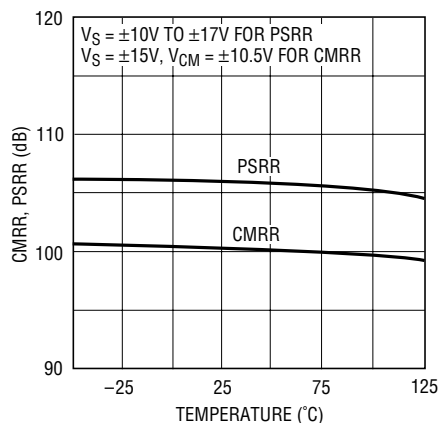
LT1055/56 G20

Common Mode Range vs Temperature



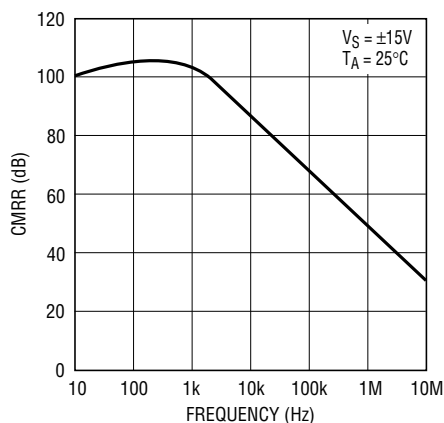
LT1055/56 G21

Common Mode and Power Supply Rejections vs Temperature



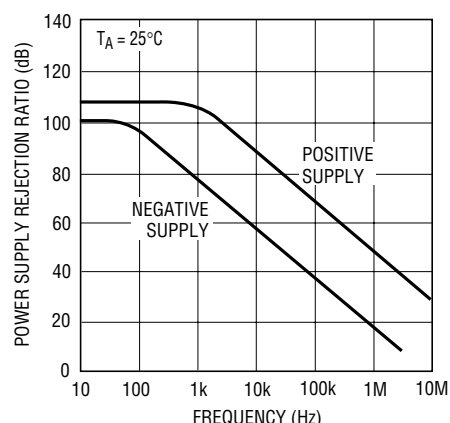
LT1055/56 G22

Common Mode Rejection Ratio vs Frequency



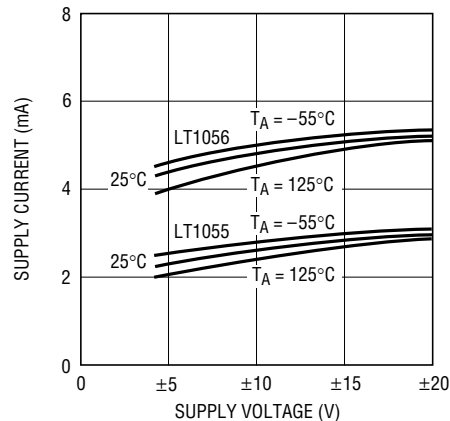
LT1055/56 G23

Power Supply Rejection Ratio vs Frequency



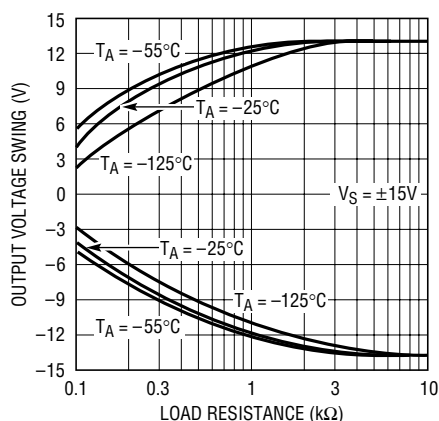
LT1055/56 G24

Supply Current vs Supply Voltage



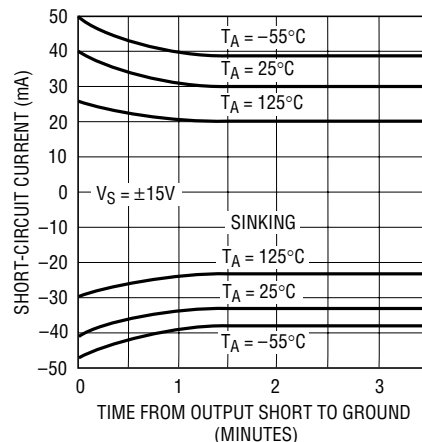
LT1055/56 G25

Output Swing vs Load Resistance



LT1055/56 G26

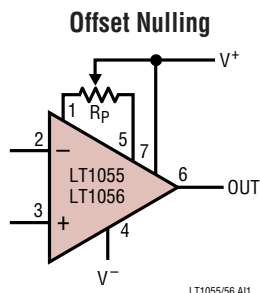
Short-Circuit Current vs Time



LT1055/56 G27

APPLICATIONS INFORMATION

The LT1055/LT1056 may be inserted directly into LF155A/LT355A, LF156A/LT356A, OP-15 and OP-16 sockets. Offset nulling will be compatible with these devices with the wiper of the potentiometer tied to the positive supply.



No appreciable change in offset voltage drift with temperature will occur when the device is nulled with a potentiometer, R_P , ranging from 10k to 200k.

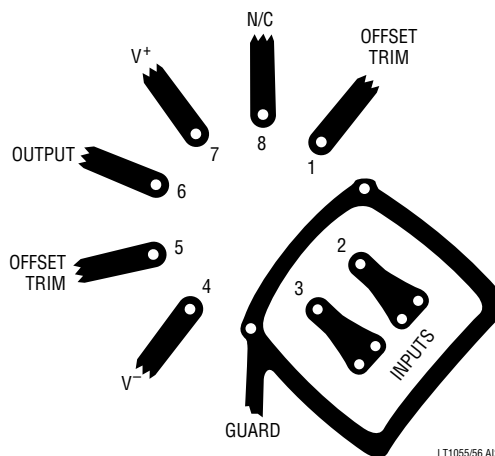
The LT1055/LT1056 can also be used in LF351, LF411, AD547, AD611, OPA-111, and TL081 sockets, provided that the nulling circuitry is removed. Because of the LT1055/LT1056's low offset voltage, nulling will not be necessary in most applications.

Achieving Picoampere/Microvolt Performance

In order to realize the picoampere-microvolt level accuracy of the LT1055/LT1056 proper care must be exercised. For example, leakage currents in circuitry external to the op amp can significantly degrade performance. High quality insulation should be used (e.g. Teflon™, Kel-F); cleaning of all insulating surfaces to remove fluxes and other residues will probably be required. Surface coating may be necessary to provide a moisture barrier in high humidity environments.

Board leakage can be minimized by encircling the input circuitry with a guard ring operated at a potential close to that of the inputs: in inverting configurations the guard ring should be tied to ground, in noninverting connections to the inverting input at pin 2. Guarding both sides of the printed circuit board is required. Bulk leakage reduction depends on the guard ring width.

Teflon is a trademark of Dupont.



The LT1055/LT1056 has the lowest offset voltage of any JFET input op amp available today. However, the offset voltage and its drift with time and temperature are still not as good as on the best bipolar amplifiers because the transconductance of FETs is considerably lower than that of bipolar transistors. Conversely, this lower transconductance is the main cause of the significantly faster speed performance of FET input op amps.

Offset voltage also changes somewhat with temperature cycling. The AM grades show a typical 20 μ V hysteresis (30 μ V on the M grades) when cycled over the -55°C to 125°C temperature range. Temperature cycling from 0°C to 70°C has a negligible (less than 10 μ V) hysteresis effect.

The offset voltage and drift performance are also affected by packaging. In the plastic N8 package the molding compound is in direct contact with the chip, exerting pressure on the surface. While NPN input transistors are largely unaffected by this pressure, JFET device matching and drift are degraded. Consequently, for best DC performance, as shown in the typical performance distribution plots, the TO-5 H package is recommended.

Noise Performance

The current noise of the LT1055/LT1056 is practically immeasurable at $1.8\text{fA}/\sqrt{\text{Hz}}$. At 25°C it is negligible up to 1G of source resistance, R_S (compound to the noise of R_S). Even at 125°C it is negligible to 100M of R_S .

APPLICATIONS INFORMATION

The voltage noise spectrum is characterized by a low 1/f corner in the 20Hz to 30Hz range, significantly lower than on other competitive JFET input op amps. Of particular interest is the fact that with any JFET IC amplifier, the frequency location of the 1/f corner is proportional to the square root of the internal gate leakage currents and, therefore, noise doubles every 20°C. Furthermore, as illustrated in the noise versus chip temperature curves, the 0.1Hz to 10Hz peak-to-peak noise is a strong function of temperature, while wideband noise ($f_0 = 1\text{kHz}$) is practically unaffected by temperature.

Consequently, for optimum low frequency noise, chip temperature should be minimized. For example, operating an LT1056 at $\pm 5\text{V}$ supplies or with a 20°C/W case-to-ambient heat sink reduces 0.1Hz to 10Hz noise from typically 2.5 $\mu\text{V}_{\text{P-P}}$ ($\pm 15\text{V}$, free-air) to 1.5 $\mu\text{V}_{\text{P-P}}$. Similarly, the noise of an LT1055 will be 1.8 $\mu\text{V}_{\text{P-P}}$ typically because of its lower power dissipation and chip temperature.

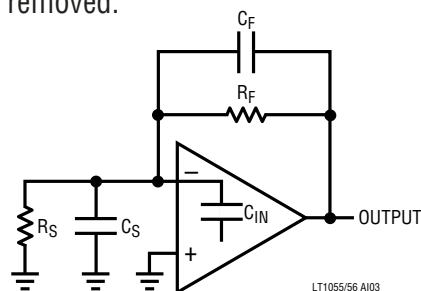
High Speed Operation

Settling time is measured in the test circuit shown. This test configuration has two features which eliminate problems common to settling time measurements: (1) probe

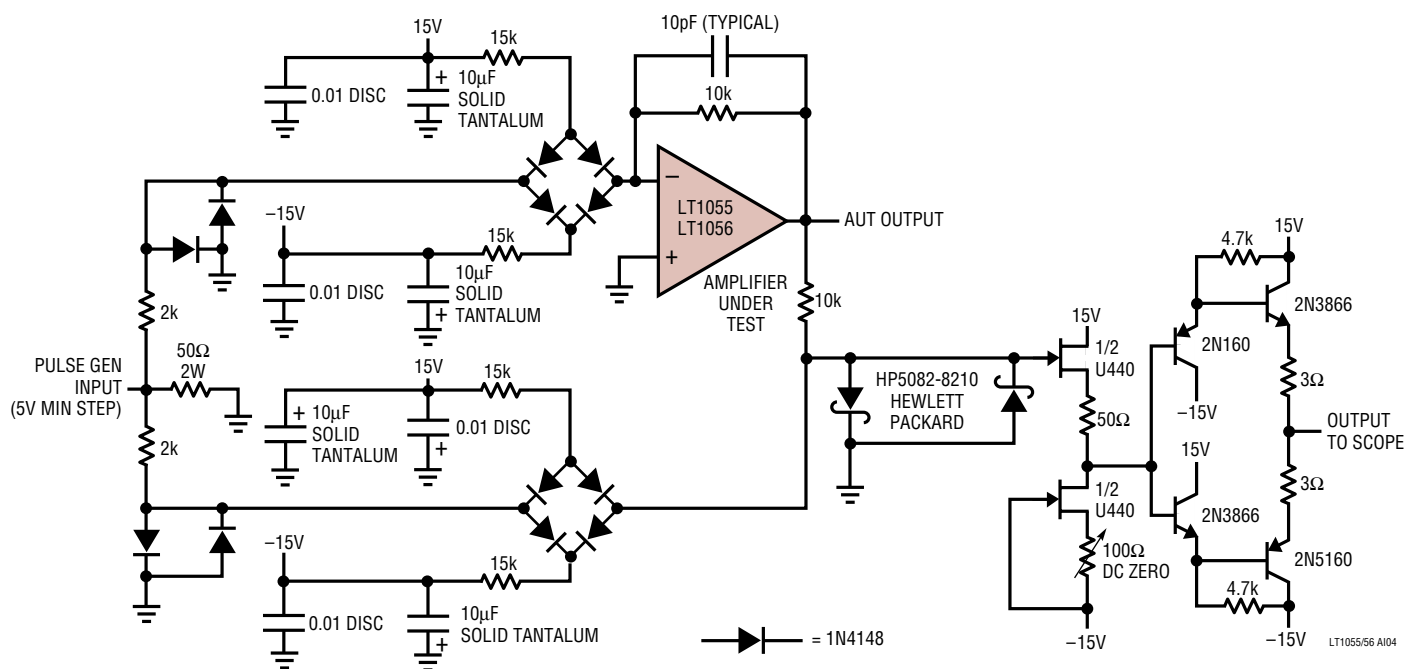
capacitance is isolated from the “false summing” node, and (2) it does not require a “flat top” input pulse since the input pulse is merely used to steer current through the diode bridges. For more details, please see Application Note 10.

As with most high speed amplifiers, care should be taken with supply decoupling, lead dress and component placement.

When the feedback around the op amp is resistive (R_F), a pole will be created with R_F , the source resistance and capacitance (R_S , C_S), and the amplifier input capacitance ($C_{\text{IN}} \approx 4\text{pF}$). In low closed-loop gain configurations and with R_S and R_F in the kilohm range, this pole can create excess phase shift and even oscillation. A small capacitor (C_F) in parallel with R_F eliminates this problem. With R_S ($C_S + C_{\text{IN}}$) = $R_F C_F$, the effect of the feedback pole is completely removed.



Settling Time Test Circuit

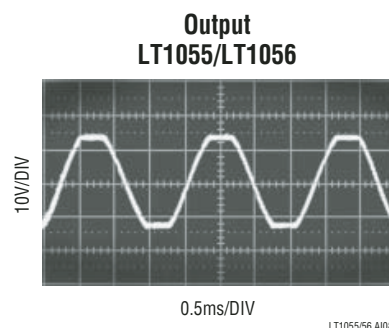
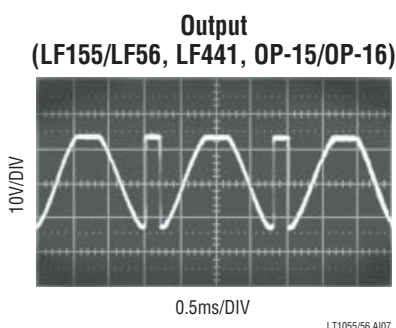
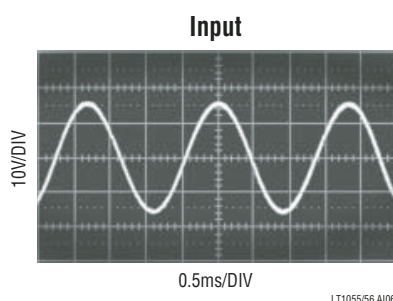
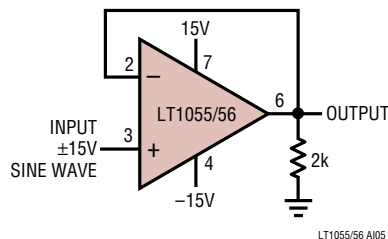


APPLICATIONS INFORMATION

Phase Reversal Protection

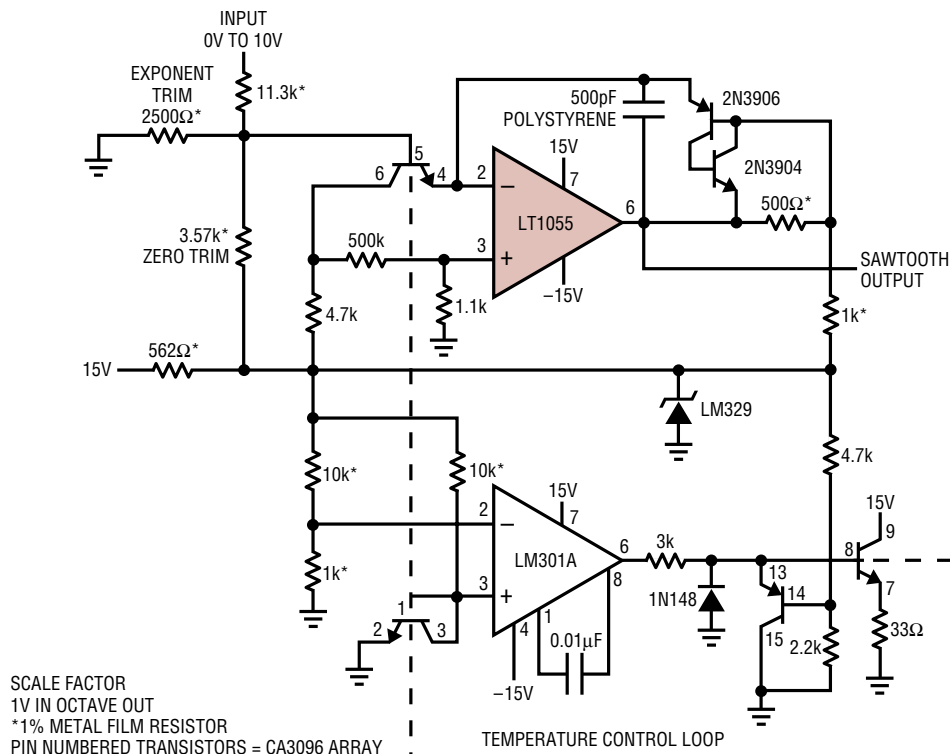
Most industry standard JFET input op amps (e.g., LF155/LF156, LF351, LF411, OP15/16) exhibit phase reversal at the output when the negative common mode limit at the input is exceeded (i.e., from -12V to -15V with $\pm 15\text{V}$ supplies). This can cause lock-up in servo systems. As shown below, the LT1055/LT1056 does not have this problem due to unique phase reversal protection circuitry (Q1 on simplified schematic).

Voltage Follower with Input Exceeding the Negative Common Mode Range



TYPICAL APPLICATIONS [†]

Exponential Voltage-to-Frequency Converter for Music Synthesizers



[†]For ten additional applications utilizing the LT1055 and LT1056, please see the LTC1043 data sheet and Application Note 3.

LT1055/56 TA03

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The circuit diagram shows the internal components of the LT1055/56 TA04 precision current source. It features two operational amplifiers: an LT1055 and an LT1001. The LT1055 is configured as a voltage follower, with its non-inverting input connected to a 0V to 10V input through a 249k resistor. The output of the LT1055 is connected to the non-inverting input of the LT1001. The LT1001 is configured as a precision current source, with its output connected to a 15V supply through a 10k resistor. The circuit also includes a 74C00 NAND gate, a 74C74 monostable multivibrator, and an LM329 timer. The output of the circuit is a current ratio $\frac{f_{OUT}(A)}{f_{CLK}(B)}$.

The diagram shows a two-stage comparator circuit. The first stage uses an LT1056 comparator with its non-inverting input (+) connected to an LT1009 2.5V reference and its inverting input (-) connected to the circuit input through a 4.7k resistor. A feedback path from the output (pin 6) to the inverting input consists of a 50k resistor and an HP5082-2810 delay element in parallel. The output of the first stage (pin 6) is connected to the non-inverting input (+) of an LT1011 comparator. The LT1011's inverting input (-) is grounded, and its output (pin 7) is the final circuit output. Both comparators are powered by a 15V supply and a -15V supply. A 3k resistor is connected between the 15V supply and the output of the second stage.

DELAY = 250ns
 * = 1% FILM RESISTOR

LT1055/56 TA06

[illegible]

*1% FILM RESISTOR

 = 1N4148

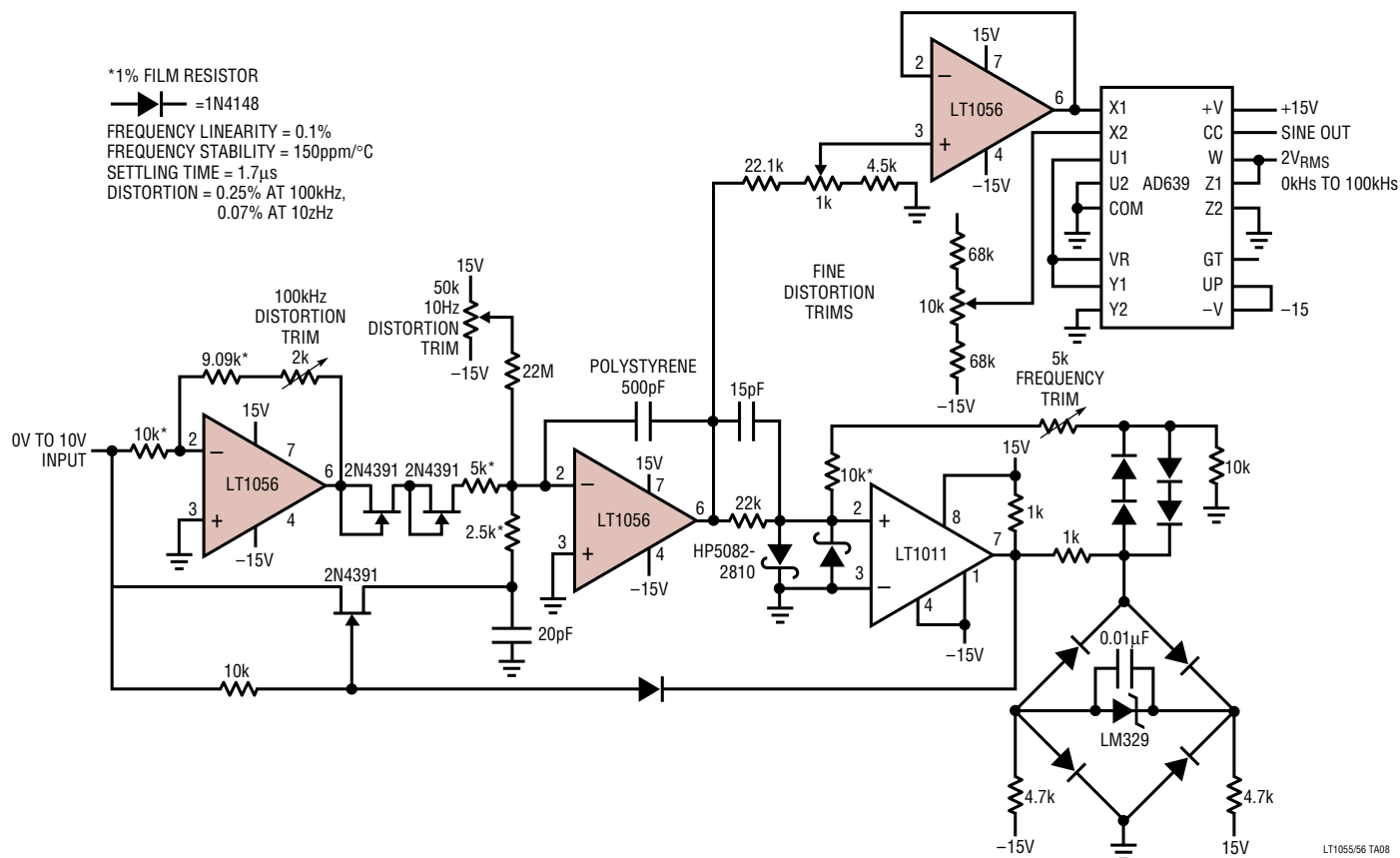
FREQUENCY LINEARITY = 0.1%

FREQUENCY STABILITY = 150ppm/°C

SETTLING TIME = $1.7\mu\text{s}$

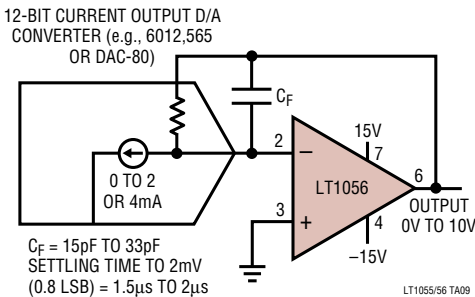
DISTORTION = 0.25% AT 100kHz,

0.07% AT 10zHz

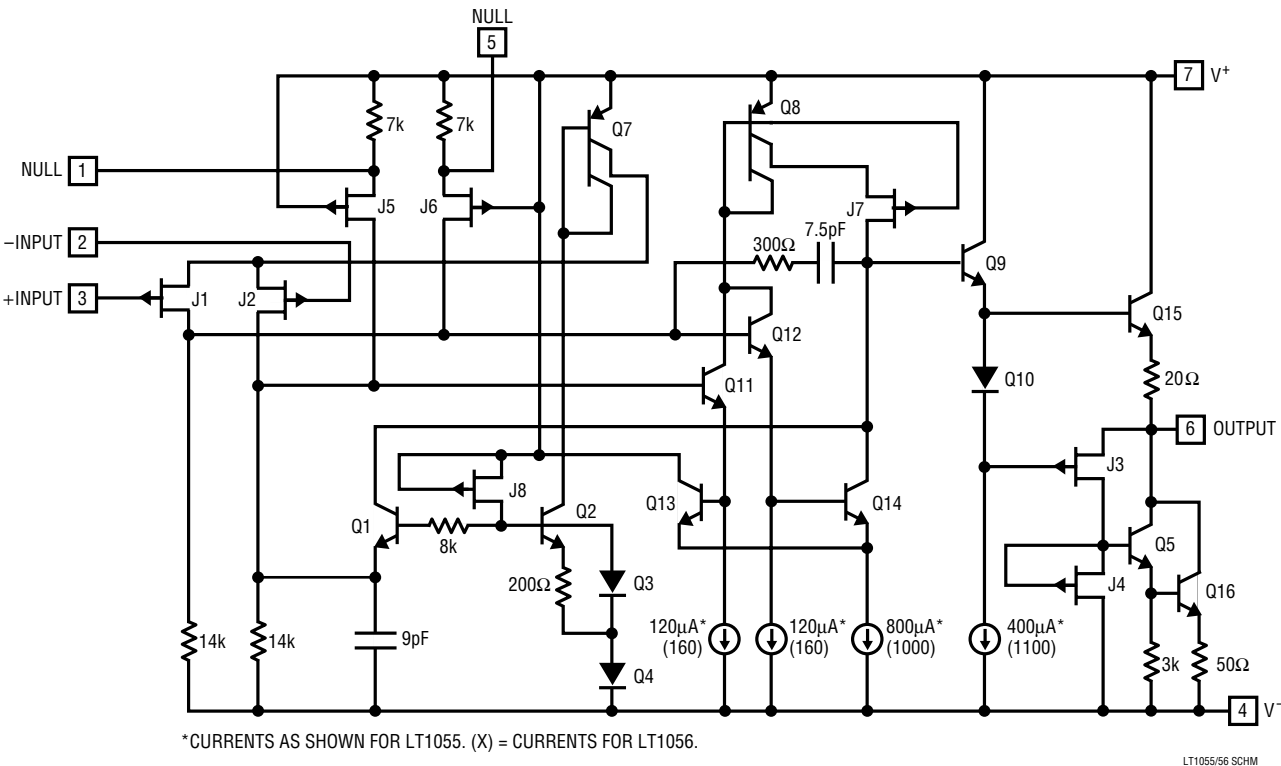


TYPICAL APPLICATIONS

12-Bit Voltage Output D/A Converter

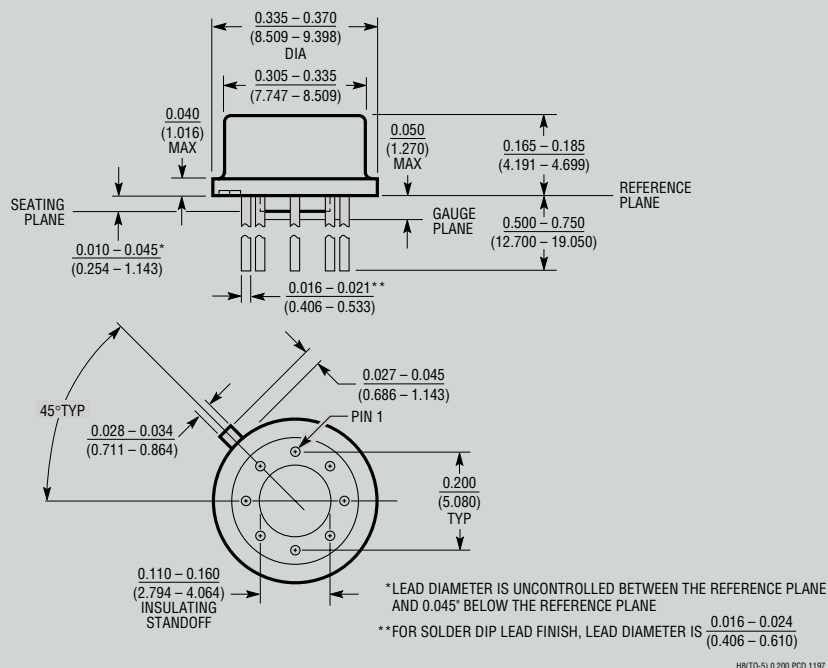


SIMPLIFIED SCHEMATIC



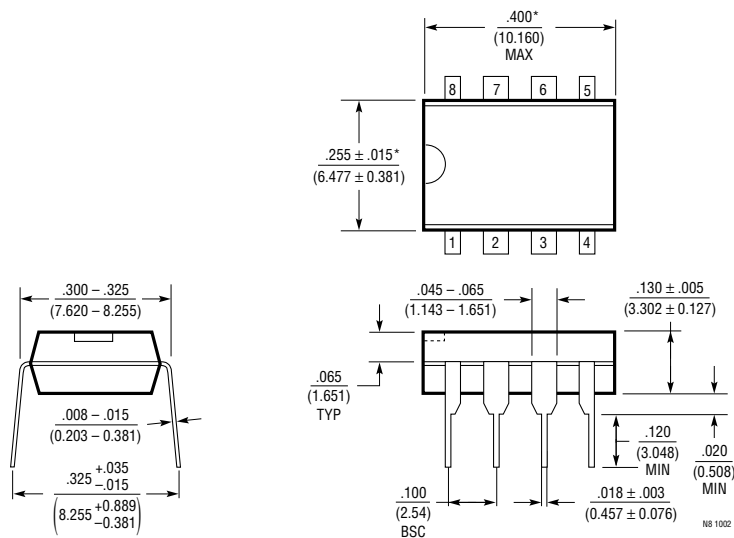
PACKAGE DESCRIPTION

H Package 8-Lead TO-5 Metal Can (.200 Inch PCD) (Reference LTC DWG # 05-08-1320)



OBsolete PACKAGE

N8 Package 8-Lead PDIP (Narrow .300 Inch) (Reference LTC DWG # 05-08-1510)



NOTE:
1. DIMENSIONS ARE INCHES
MILLIMETERS
*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH (0.254mm)

10556fc

[illegible]

PACKAGE DESCRIPTION

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1122	Fast Settling JFET Op Amp	340ns Settling Time, GBW = 14MHz, SR = 60V/μs
LT1792	Low Noise JFET Op Amp	$e_n = 6\text{nV}/\sqrt{\text{Hz}}$ Max at f = 1kHz