CDP1857C

March 1997

4-Bit Bus Buffer/Separator

Features

- **Provides Easy Connection of I/O to CDP1800-Series Microprocessor Data Bus**
- **Non-Inverting Fully Buffered Data Transfer**

Ordering Information

PART NUMBER	TEMP. RANGE	PACKAGE	PKG. NO.
CDP1857CE	-40^{o}C to +85^{o}C	PDIP	E16.3
CDP1857CD	-40^{o}C to +85^{o}C	SBDIP	D16.3

TABLE 1. CDP1857 FUNCTION FOR I/O BUS SEPARATOR OPERATION

CS	$\overline{MRD}$	DATA BUS OUT DB0-DB3	DATA OUT DO0-DO3
0	X	High Impedance	High Impedance
1	0	High Impedance	Data Bus
1	1	Data In	High Impedance

Description

The CDP1857C is a 4-bit CMOS non-inverting bus separator designed for use in CDP1800-series microprocessor systems. It can be controlled directly by a 1800-series microprocessor without the use of additional components.

The CDP1857 is designed for use as a bus buffer or separator between the 1800-series microprocessor data bus and I/O devices. It provides a chip-select (CS) input signal which, when high (1), enables the bus-separator three-state output drivers. The direction of data flow, when enabled, is controlled by the $\overline{MRD}$ input signal.

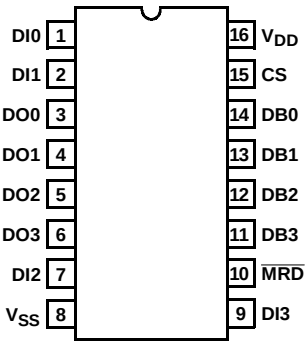
In the CDP1857, when $\overline{MRD}$ = 1, it enables the three-state bus drivers (DB0-DB3) and transfers data from the DATA-IN lines onto the data bus. When $\overline{MRD}$ = 0, it disables the three-state bus drivers (DB0-DB3) and enables the three-state data output drivers (DO0-DO3), thus, transferring data from the data bus to the DATA-OUT terminals.

The CDP1857 can be used as a bidirectional bus buffer by connecting the corresponding DI and DO terminals (Figure 1). The $\overline{MRD}$ output signal from the 1800-series microprocessor has the correct polarity to control the CDP1857 when it is used as I/O bus buffer/separator. Therefore, the 1800-series microprocessor $\overline{MRD}$ signal can be connected directly to the $\overline{MRD}$ input of CDP1857. See Function Table 1 for use of the CDP1857 as an I/O bus buffer/separator.

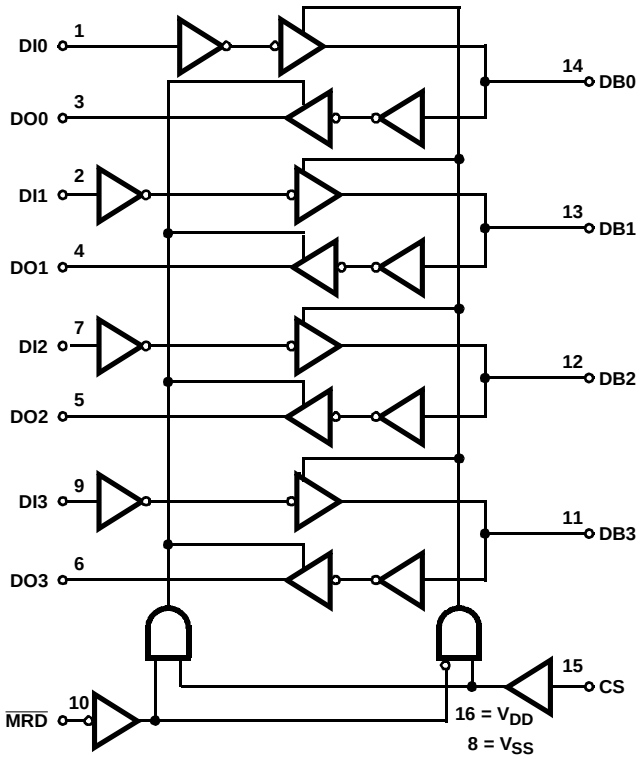
The CDP1857C is supplied in 16-lead hermetic, dual-in-line ceramic packages (D suffix), and in 16-lead plastic packages (E suffix).

Pinout

16 LEAD DIP
TOP VIEW



Functional Diagram For CDP1857



Absolute Maximum Ratings

DC Supply Voltage Range, (V_{DD})
(All Voltages Referenced to V_{SS} Terminal) . . . . . -0.5V to +7V
Input Voltage Range, All Inputs . . . . . -0.5V to V_{DD} +0.5V
DC Input Current, Any One Input . . . . . ±10mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (^{o}C/W)	θ_{JC} (^{o}C/W)
PDIP Package	85	N/A
SBDIP Package	85	22

Device Dissipation Per Output Transistor
T_A = Full Package Temperature Range
(All Package Types) 100mW
Operating Temperature Range (T_A)
Package Type D . . . . . -55^{o}C to +125^{o}C
Package Type E . . . . . -40^{o}C to +85^{o}C
Storage Temperature Range (T_{STG}) . . . . . -65^{o}C to +150^{o}C
Lead Temperature (During Soldering) . . . . . +265^{o}C
At distance 1/16 □± 1/32 In. (1.59 ± 0.79mm)
from case for 10s max

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Static Electrical Specifications

At T_A = -40^{o}C to +85^{o}C, Except as Noted:

PARAMETER	SYMBOL	CONDITIONS V_O (V)	CONDITIONS V_{IN} (V)	CONDITIONS V_{DD} (V)	MIN	(NOTE 1) TYP	MAX	UNITS
Quiescent Device Current	I_{DD}	-	0, 5	5	-	5	50	µA
Output Low Drive (Sink) Current	I_{OL}	0.4	0, 5	5	1.6	3.2	-	mA
Output High Drive (Source) Current	I_{OH}	4.6	0, 5	5	-1.15	-2.3	-	mA
Output Voltage Low-Level (Note 3)	V_{OL}	-	0, 5	5	-	0	0.1	V
Output Voltage High-Level (Note 3)	V_{OH}	-	0, 5	5	4.9	5	-	V
Input Low Voltage	V_{IL}	0.5, 4.5	-	5	-	-	1.5	V
Input High Voltage	V_{IH}	0.5, 4.5	-	5	3.5	-	-	V
Input Leakage Current	I_{IN}	Any Input	0, 5	5	-	-	±1	µA
Operating Current (Note 2)	I_{DD1}	0, 5	0, 5	5	-	50	100	µA
Input Capacitance	C_{IN}	-	-	-	-	5	7.5	pF

NOTES:

1. Typical values are for T_A =+25^{o}C and nominal voltage.
2. Operating current measured in a CDP1802 system at 3.2MHz with outputs floating.
3. I_{OL} = I_{OH} = 1µA.

Dynamic Electrical Specifications

At T_A = -40^{o}C to +85^{o}C, V_{DD} = 5V ±5%, V_{IH} = 0.7 V_{DD}, V_{IL} = 0.3 V_{DD}, t_R, t_F = 20ns, C_L = 100pF

PARAMETER	SYMBOL	V_{DD} (V)	(NOTE 1) TYP	MAX	UNITS
Propagation Delay Time:					
$\overline{MRD}$ or CS to DO	t_{ED}	5	150	225	ns
$\overline{MRD}$ or CS to DB	t_{EB}	5	150	225	ns
DI to DB	t_{IB}	5	100	150	ns
DB to DO	t_{BO}	5	100	150	ns

NOTE:

1. Typical values are for T_A = 25^{o}C and nominal voltages.

Recommended Operating Conditions At T_A = Full Package Temperature Range.For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

PARAMETER	MIN	MAX	UNITS
Supply-Voltage Range	4	6.5	V
Recommended Input Voltage Range	V_{SS}	V_{DD}	V

Timing Diagrams

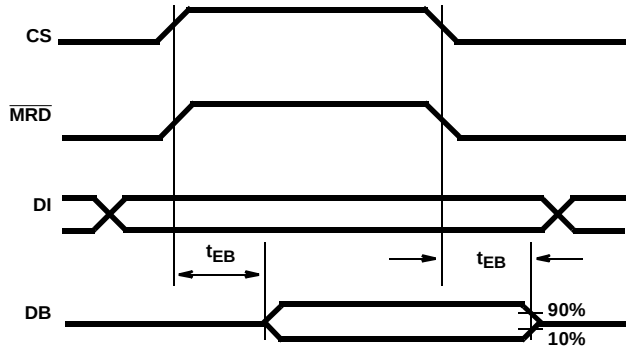


FIGURE 1A. ENABLE TO DB TIME

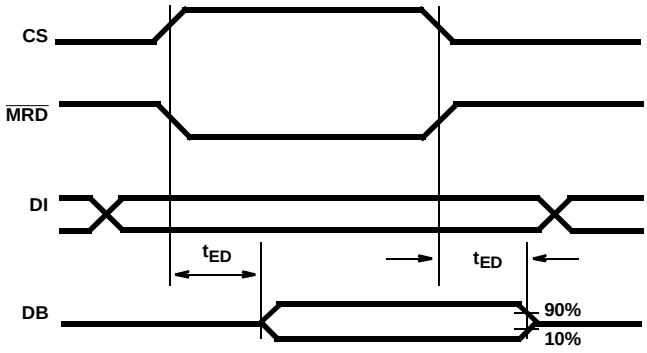


FIGURE 1B. ENABLE TO DO TIME

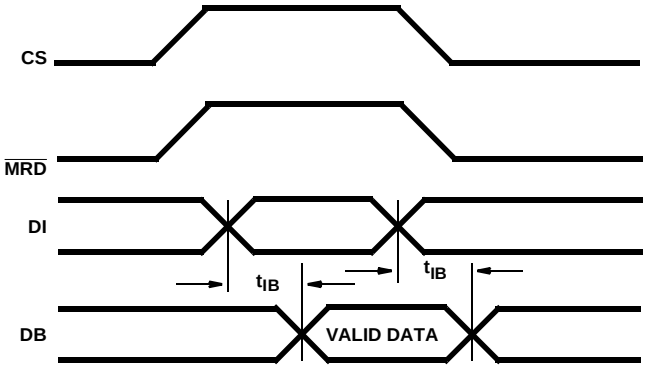


FIGURE 1C. DI TO DB TIME

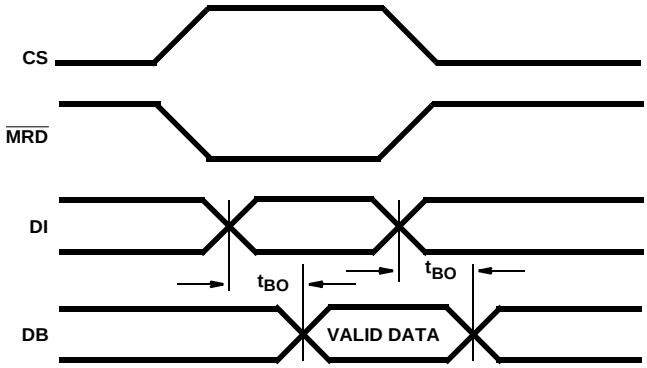


FIGURE 1D. DB TO DO TIME

FIGURE 1. TIMING DIAGRAMS FOR CDP1857C

Typical Applications

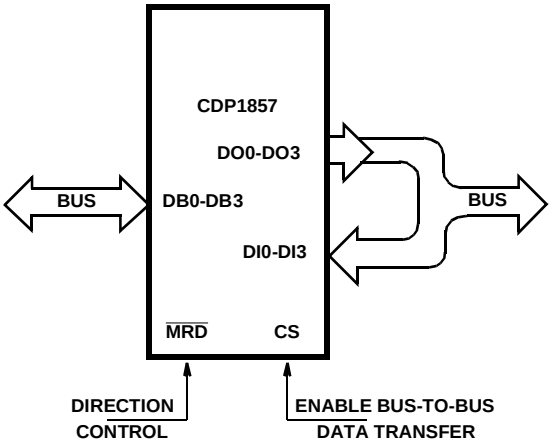


FIGURE 2. CDP1857 BIDIRECTIONAL BUS BUFFER OPERATION

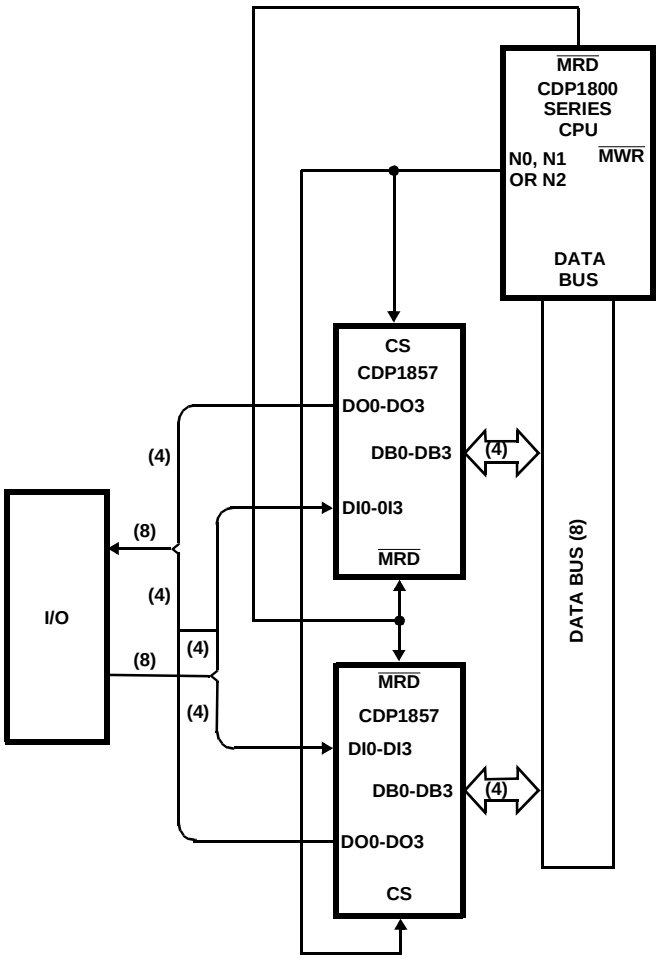


FIGURE 3. CDP1857 BUS SEPARATOR OPERATION

All Intersil U.S. products are manufactured, assembled and tested utilizing ISO9000 quality systems.
Intersil Corporation's quality certifications can be viewed at www.intersil.com/design/quality