



FAST CMOS SYNCHRONOUS PRESETTABLE BINARY COUNTER

IDT74FCT161T/AT/CT

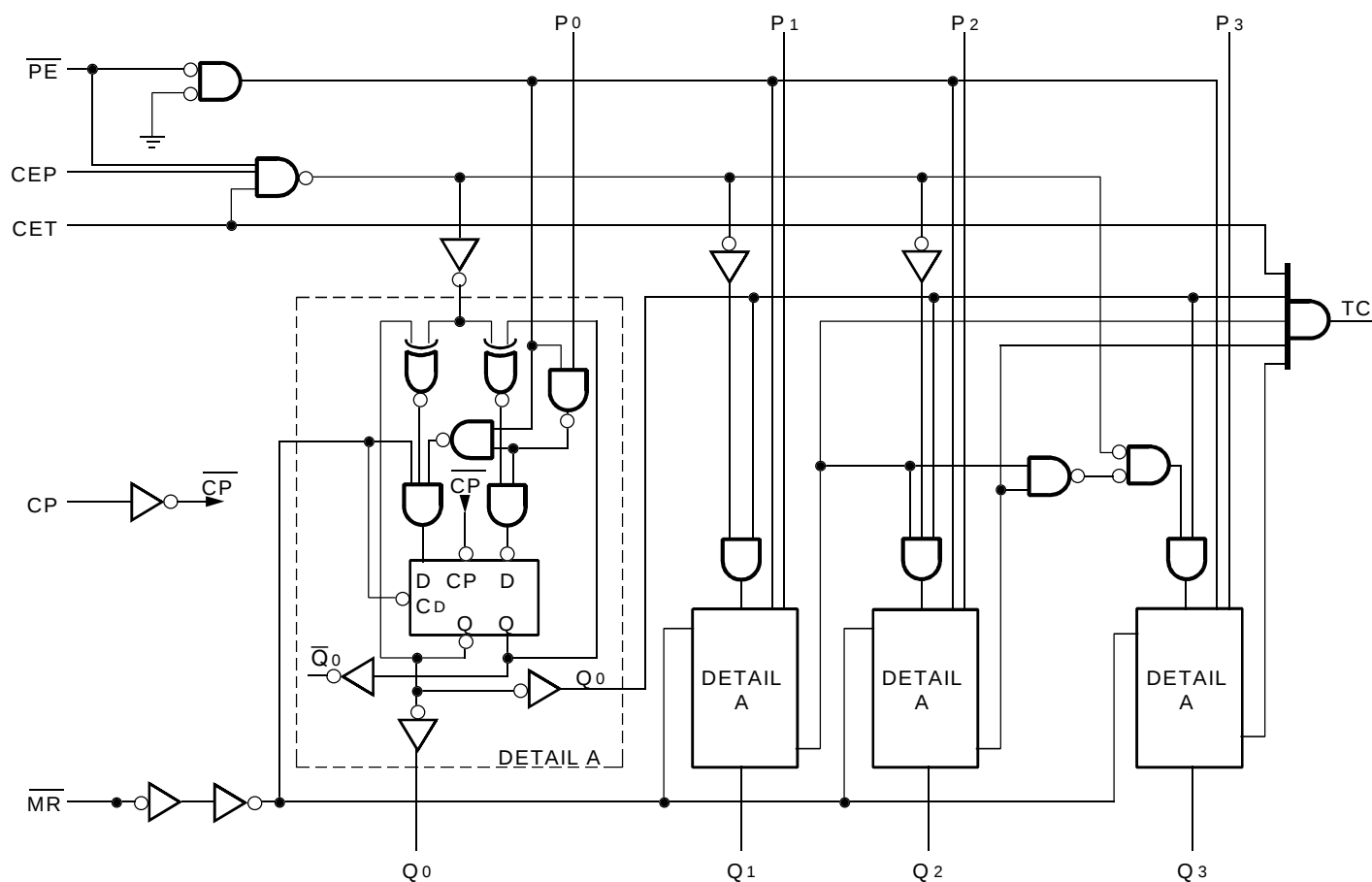
FEATURES:

- A and C speed grades
- Low input and output $\leq 1\mu\text{A}$ (max.)
- CMOS power levels
- True TTL input and output compatibility
 - – $V_{OH} = 3.3\text{V}$ (typ.)
 - – $V_{OL} = 0.3\text{V}$ (typ.)
- High drive outputs (-15mA I_{OH} , 48mA I_{OL})
- Meets or exceeds JEDEC standard 18 specifications
- Power off disable outputs permit "live insertion"
- Available in SOIC and QSOP packages

DESCRIPTION:

The IDT74FCT161T is a high-speed synchronous modulo-16 binary counter built using an advanced dual metal CMOS technology. It is synchronously presettable for application in programmable dividers and has two types of count enable inputs plus a terminal count output for versatility in forming synchronous multi-stage counters. The IDT74FCT161T has asynchronous Master Reset inputs that override all other inputs and force the outputs low.

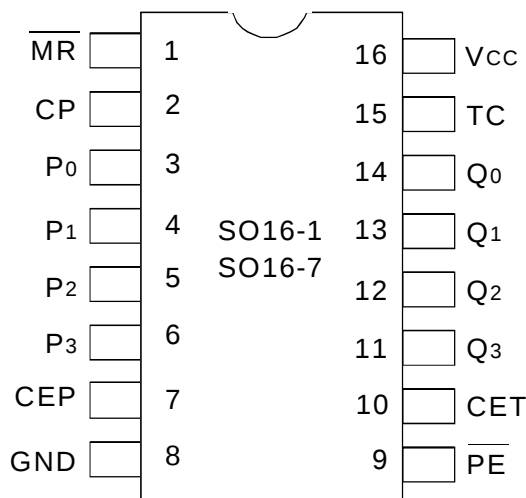
FUNCTIONAL BLOCK DIAGRAM



INDUSTRIAL TEMPERATURE RANGE

AUGUST 2000

PIN CONFIGURATION



SOIC/ QSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Rating	Max.	Unit
V _{TERM} ⁽²⁾	Terminal Voltage with Respect to GND	−0.5 to +7	V
V _{TERM} ⁽³⁾	Terminal Voltage with Respect to GND	−0.5 to V _{CC} +0.5	V
T _{STG}	Storage Temperature	−65 to +150	°C
I _{OUT}	DC Output Current	−65 to +120	mA

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by +0.5V unless otherwise noted.
- Inputs and V_{CC} terminals only.
- Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	6	10	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	8	12	pF

8T-link

NOTE:

- This parameter is measured at characterization but not tested.

PIN DESCRIPTION

Pin Names	Description
CEP	Count Enable Parallel Input
CET	Count Enable Trickle Input
CP	Clock Pulse Input (Active Rising Edge)
$\overline{MR}$	Asynchronous Master Reset Input (Active LOW)
P0-3	Parallel Data Inputs
$\overline{PE}$	Parallel Enable Input (Active LOW)
Q0-3	Flip-Flop Outputs
TC	Terminal Count Output

FUNCTION TABLE⁽¹⁾

$\overline{PE}$	CET	CEP	Action on the Rising Clock Edge(s)
X	X	X	Reset (Clear)
L	X	X	Load (P _n → Q _n)
H	H	H	Count (Increment)
H	L	X	No Change (Hold)
H	X	L	No Change (Hold)

NOTE:

- H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Industrial: $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = 5.0\text{V} \pm 5\%$

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level ⁽⁵⁾		2V	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current ⁽⁴⁾	$V_{CC} = \text{Max.}$	$V_I = 2.7\text{V}$	—	—	± 1	μA
I_{IL}	Input LOW Current ⁽⁴⁾	$V_{CC} = \text{Max.}$	$V_I = 0.5\text{V}$	—	—	± 1	μA
I_I	Input HIGH Current ⁽⁴⁾	$V_{CC} = \text{Max.}$, $V_I = V_{CC} (\text{Max.})$		—	—	± 1	μA
V_{IK}	Clamp Diode Voltage	$V_{CC} = \text{Min.}$, $I_N = -18\text{mA}$		—	-0.7	-1.2	V
I_{OS}	Short Circuit Current	$V_{CC} = \text{Max.}$ ⁽³⁾ , $V_O = \text{GND}$		-60	-120	-225	mA
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -8\text{mA}$	2.4	3.3	—	V
			$I_{OH} = -15\text{mA}$	2	3	—	V
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 48\text{mA}$	—	0.3	0.5	V
V_H	Input Hysteresis	—		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	$V_{CC} = \text{Max.}$ $V_{IN} = \text{GND}$ or V_{CC}		—	0.01	1	mA

NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 5.0\text{V}$, $+25^{\circ}\text{C}$ ambient.
- Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
- The test limit for this parameter is $\pm 5\mu\text{A}$ at $T_A = -55^{\circ}\text{C}$.
- Clock pin requires a minimum V_{IH} of 2.5V.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	$V_{CC} = \text{Max.}$ $V_{IN} = 3.4V^{(3)}$		—	0.5	2	mA
I_{CCD}	Dynamic Power Supply Current ⁽⁴⁾	$V_{CC} = \text{Max.}$, Outputs Open Load Mode $CEP = CET = \overline{PE} = \text{GND}$ $\overline{MR} = V_{CC}$ One Input Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current ⁽⁶⁾	$V_{CC} = \text{Max.}$, Outputs Open Load Mode $f_{CP} = 10\text{MHz}$ 50% Duty Cycle $CEP = CET = \overline{PE} = \text{GND}$ $\overline{MR} = V_{CC}$ One Bit Toggling at $f_i = 5\text{MHz}$ 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	1.5	3.5	mA
			$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	—	2	5.5	
		$V_{CC} = \text{Max.}$, Outputs Open Load Mode $f_{CP} = 10\text{MHz}$ 50% Duty Cycle $CEP = CET = \overline{PE} = \text{GND}$ $\overline{MR} = V_{CC}$ Four Bits Toggling at $f_i = 5\text{MHz}$ 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	3.8	7.3 ⁽⁵⁾	
			$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	—	5	12.3 ⁽⁵⁾	

NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 5.0V$, $+25^\circ\text{C}$ ambient.
- Per TTL driven input ($V_{IN} = 3.4V$). All other inputs at V_{CC} or GND .
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- $I_C = I_{\text{QUIESCENT}} + I_{\text{INPUTS}} + I_{\text{DYNAMIC}}$
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
 $I_{CC} = \text{Quiescent Current}$
 $\Delta I_{CC} = \text{Power Supply Current for a TTL High Input } (V_{IN} = 3.4V)$
 $D_H = \text{Duty Cycle for TTL Inputs High}$
 $N_T = \text{Number of TTL Inputs at } D_H$
 $I_{CCD} = \text{Dynamic Current Caused by an Input Transition Pair (HLH or LHL)}$
 $f_{CP} = \text{Clock Frequency for Register Devices (Zero for Non-Register Devices)}$
 $f_i = \text{Input Frequency}$
 $N_i = \text{Number of Inputs at } f_i$
 All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

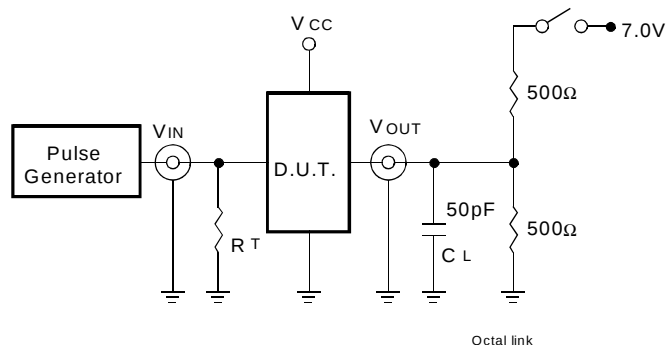
Symbol	Parameter	Condition ⁽¹⁾	IDT74FCT161T		IDT54FCT161AT		IDT74FCT161CT		Unit
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n ($\overline{PE}$ Input HIGH)	$C_L = 50\text{pF}$ $R_L = 500\Omega$	2	11	2	7.2	2	5.8	ns
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n ($\overline{PE}$ Input LOW)		2	9.5	2	6.2	2	5.8	ns
t_{PLH} t_{PHL}	Propagation Delay CP to TC		2	15	2	9.8	2	7.4	ns
t_{PLH} t_{PHL}	Propagation Delay CET to TC		1.5	8.5	1.5	5.5	1.5	5.2	ns
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n		2	13	2	8.5	2	6	ns
t_{PHL}	Propagation Delay $\overline{MR}$ to TC		2	11.5	2	7.5	2	7	ns
t_{SU}	Set-up Time, HIGH or LOW P_n to CP		5	—	4	—	4	—	ns
t_H	Hold Time, HIGH or LOW P_n to CP		1.5	—	1.5	—	1.5	—	ns
t_{SU}	Set-up Time, HIGH or LOW $\overline{PE}$ or $\overline{SR}$ to CP		11.5	—	9.5	—	9.5	—	ns
t_H	Hold Time, HIGH or LOW $\overline{PE}$ or $\overline{SR}$ to CP		1.5	—	1.5	—	1.5	—	ns
t_{SU}	Set-up Time, HIGH or LOW CEP or CET to CP		11.5	—	9.5	—	9.5	—	ns
t_H	Hold Time, HIGH or LOW CEP or CET to CP		0	—	0	—	0	—	ns
t_W	Clock Pulse Width (Load) HIGH or LOW		5	—	4 ⁽³⁾	—	4 ⁽³⁾	—	ns
t_W	Clock Pulse Width (Count) HIGH or LOW		7	—	6	—	6	—	ns
t_{PHL}	$\overline{MR}$ Pulse Width LOW		5	—	4 ⁽³⁾	—	4 ⁽³⁾	—	ns
t_{PHL}	Recovery Time $\overline{MR}$ to CP		6	—	5	—	5	—	ns

NOTES:

1. See test circuits and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This limit is guaranteed but not tested.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

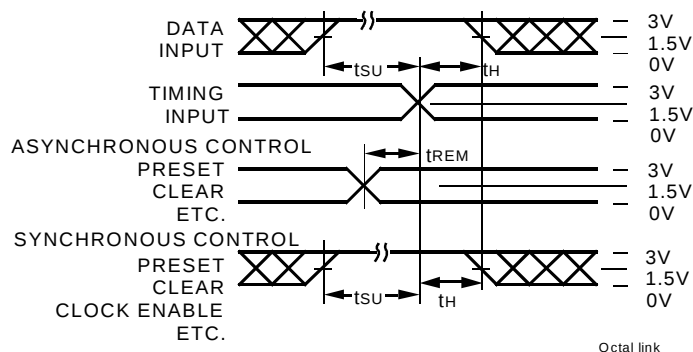
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DEFINITIONS:

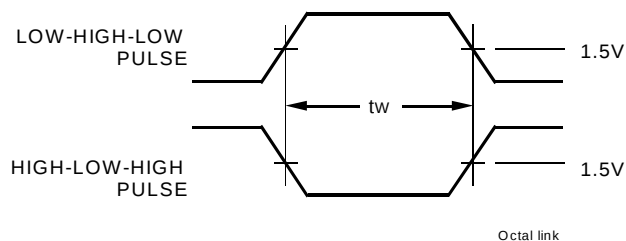
C_L = Load capacitance: includes jig and probe capacitance.

R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

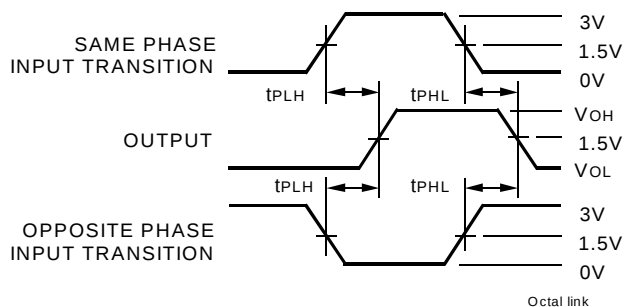
SET-UP, HOLD, AND RELEASE TIMES



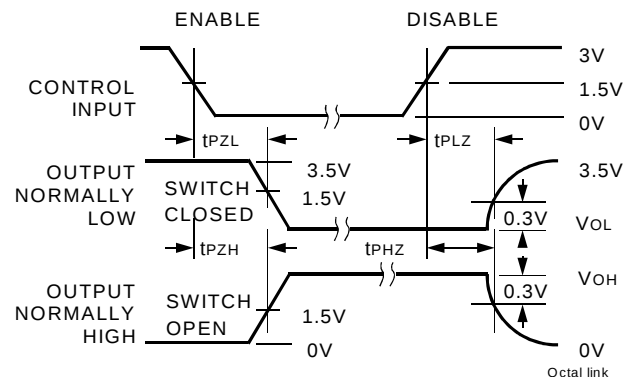
PULSE WIDTH



PROPAGATION DELAY



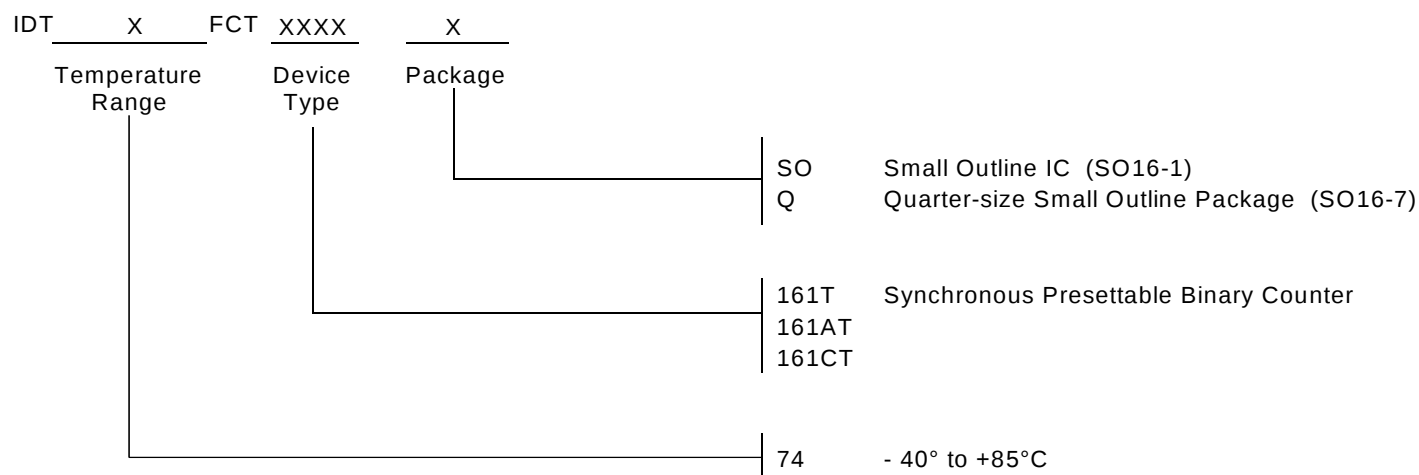
ENABLE AND DISABLE TIMES



NOTES:

- Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
- Pulse Generator for All Pulses: Rate $\leq 1.0\text{MHz}$; $t_F \leq 2.5\text{ns}$; $t_R \leq 2.5\text{ns}$

ORDERING INFORMATION



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