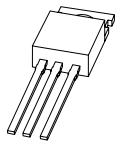


BTA312Y series C

12 A Three-quadrant triacs high commutation insulated

Rev. 01 — 27 September 2007 Product data sheet

1. Product profile

1.1 General description

Passivated, new generation, high commutation triacs in an internally insulated TO-220 plastic package

1.2 Features

- Very high commutation performance
- Isolated mounting base
- High immunity to dV/dt
- 2500 V RMS isolation voltage

1.3 Applications

- Motor control - e.g. washing machines
- Refrigeration compressors
- Non-linear rectifier-fed motor loads
- Lamp dimmers for US market

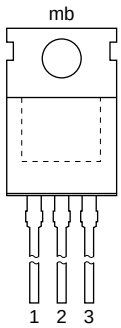
1.4 Quick reference data

- $V_{DRM} \leq 600$ V (BTA312Y-600C)
- $V_{DRM} \leq 800$ V (BTA312Y-800C)
- $I_{GT} \leq 35$ mA
- $I_{T(RMS)} \leq 12$ A
- $I_{TSM} \leq 100$ A (t = 20 ms)
- $I_{TSM} \leq 110$ A (t = 16.7 ms)

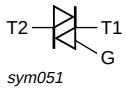
2. Pinning information

Table 1. Pinning

Pin	Description	Simplified outline	Symbol
1	main terminal 1 (T1)		
2	main terminal 2 (T2)		
3	gate (G)		
mb	mounting base; isolated		



SOT78D (TO-220)



3. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
BTA312Y-600C	TO-220	plastic single-ended package; isolated heatsink mounted; 1 mounting hole; 3-lead TO-220	SOT78D
BTA312Y-800C			

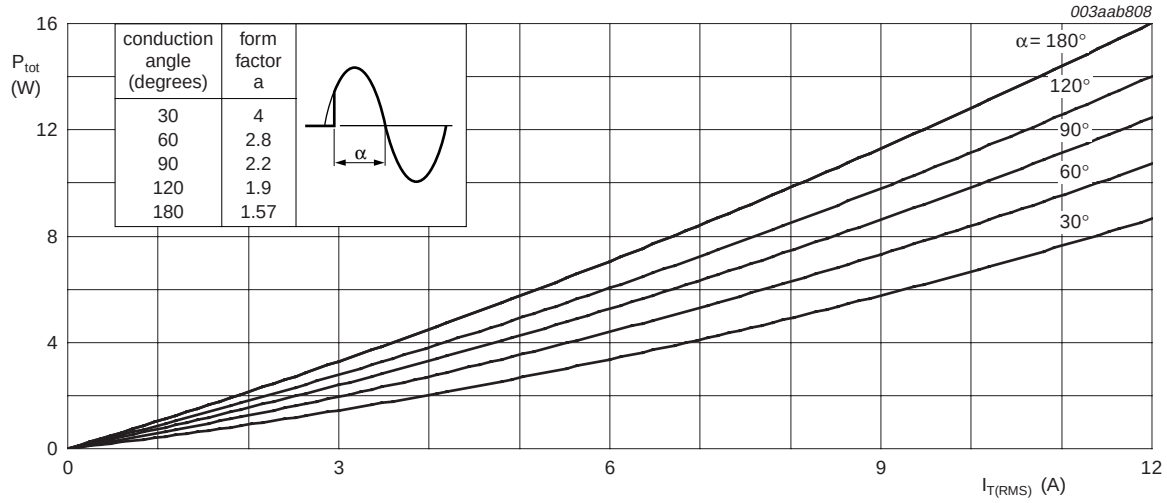
4. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

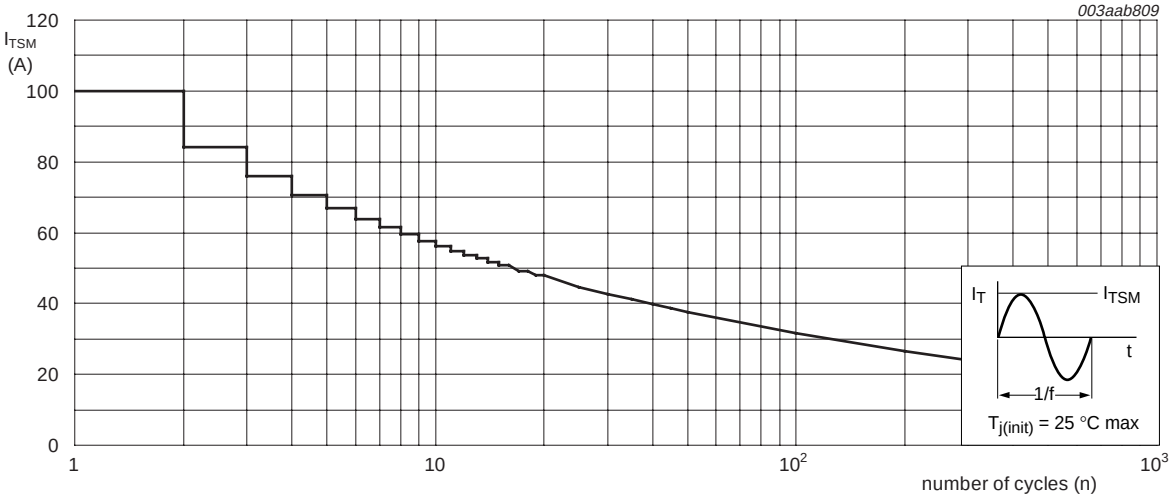
Symbol	Parameter	Conditions		Min	Max	Unit
V_{DRM}	repetitive peak off-state voltage	BTA312Y-600C;	[1]	-	600	V
		BTA312Y-800C;		-	800	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{mb} \leq 85$ °C; see Figure 4 and 5		-	12	A
I_{TSM}	non-repetitive peak on-state current	full sine wave; T_j = 25 °C prior to surge; see Figure 2 and 3				
		t = 20 ms		-	100	A
		t = 16.7 ms		-	110	A
I^2t	I^2t for fusing	t = 10 ms		-	50	A^2s
dI_T/dt	rate of rise of on-state current	I_{TM} = 20 A; I_G = 0.2 A; dI_G/dt = 0.2 A/µs		-	100	A/µs
I_{GM}	peak gate current			-	2	A
P_{GM}	peak gate power			-	5	W
$P_{G(AV)}$	average gate power	over any 20 ms period		-	0.5	W
T_{stg}	storage temperature			–40	+150	°C
T_j	junction temperature			-	125	°C

[1] Although not recommended, off-state voltages up to 800 V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 15 A/µs.



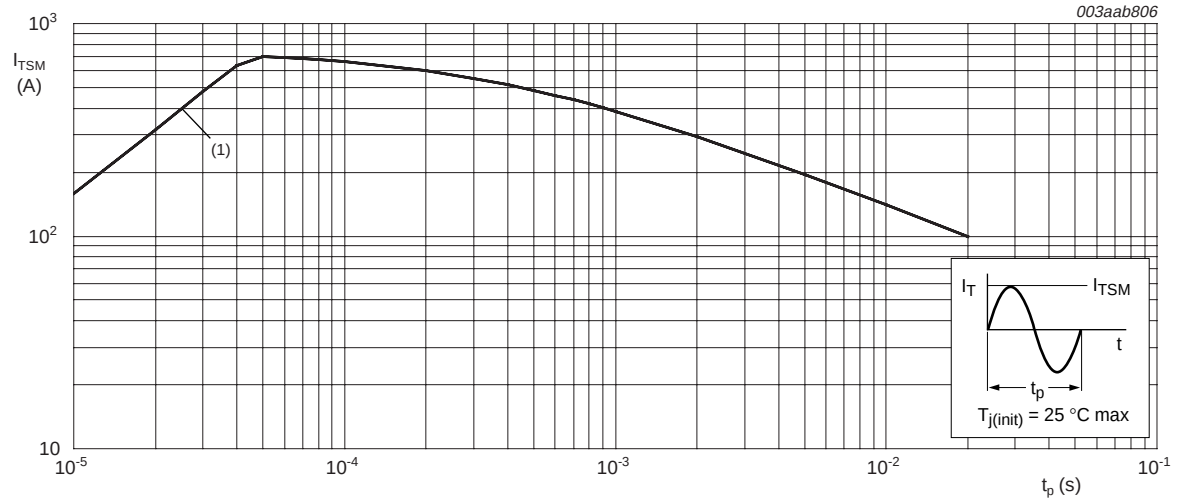
α = conduction angle

Fig 1. Total power dissipation as a function of RMS on-state current; maximum values



f = 50 Hz

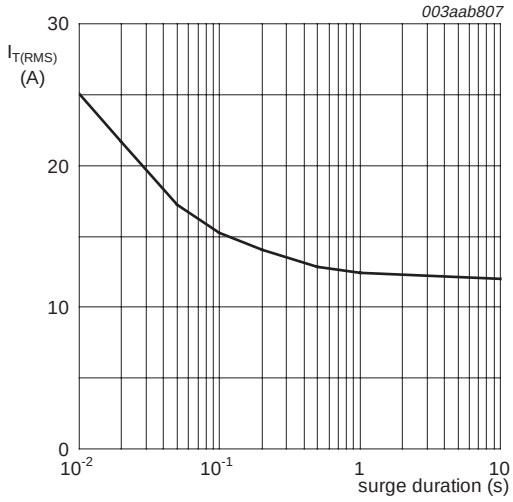
Fig 2. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values



$t_p \leq 20$ ms

(1) dI_T/dt limit

Fig 3. Non-repetitive peak on-state current as a function of pulse duration; maximum values



f = 50 Hz

T_{mb} = 85 °C

Fig 4. RMS on-state current as a function of surge duration; maximum values

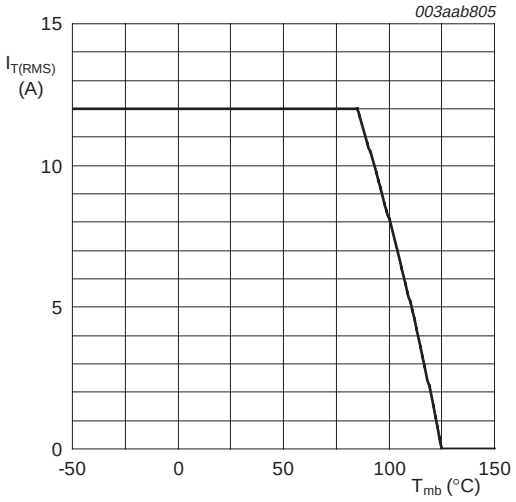


Fig 5. RMS on-state current as a function of mounting base temperature; maximum values

5. Thermal characteristics

Table 4. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	full cycle; see Figure 6	-	-	2.3	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	-	60	-	K/W

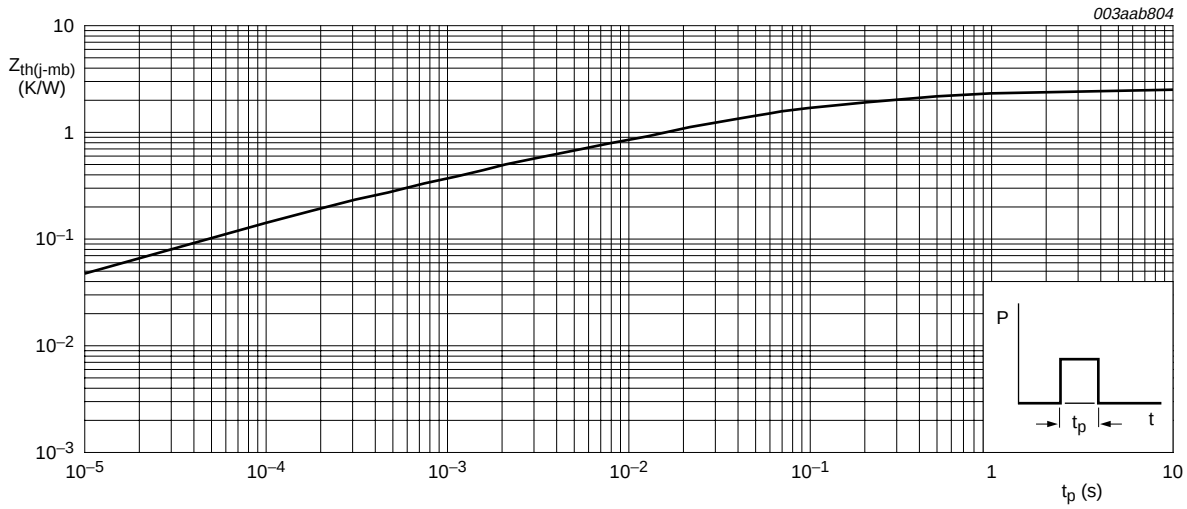


Fig 6. Transient thermal impedance from junction to mounting base as a function of pulse duration

6. Isolation characteristics

Table 5. Isolation limiting values and characteristics

T_h = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{isol(RMS)}$	RMS isolation voltage	from all three terminals to external heatsink; f = 50 Hz to 60 Hz; sinusoidal waveform; RH ≤ 65 %; clean and dust free	-	-	2500	V
C_{isol}	isolation capacitance	from pin 2 to external heatsink; f = 1 MHz	-	10	-	pF

7. Static characteristics

Table 6. Static characteristics

T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{GT}	gate trigger current	V_D = 12 V; I_T = 0.1 A; see Figure 8				
		T2+ G+	2	-	35	mA
		T2+ G–	2	-	35	mA
		T2– G–	2	-	35	mA
I_L	latching current	V_D = 12 V; I_{GT} = 0.1 A; see Figure 10				
		T2+ G+	-	-	50	mA
		T2+ G–	-	-	60	mA
		T2– G–	-	-	50	mA
I_H	holding current	V_D = 12 V; I_{GT} = 0.1 A; see Figure 11	-	-	35	mA
V_T	on-state voltage	I_T = 15 A; see Figure 9	-	1.3	1.6	V
V_{GT}	gate trigger voltage	V_D = 12 V; I_T = 0.1 A; see Figure 7	-	0.8	1.5	V
		V_D = 400 V; I_T = 0.1 A; T_j = 125 °C	0.25	0.4	-	V
I_D	off-state current	V_D = $V_{DRM(max)}$; T_j = 125 °C	-	0.1	0.5	mA

8. Dynamic characteristics

Table 7. Dynamic characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
dV_D/dt	rate of rise of off-state voltage	$V_{DM} = 0.67 \times V_{DRM(max)}$; $T_j = 125$ °C; exponential waveform; gate open circuit	500	-	-	V/µs
dI_{com}/dt	rate of change of commutating current	$V_{DM} = 400$ V; $T_j = 125$ °C; $I_{T(RMS)} = 12$ A; without snubber; gate open circuit	20	-	-	A/ms
t_{gt}	gate-controlled turn-on time	$I_{TM} = 20$ A; $V_D = V_{DRM(max)}$; $I_G = 0.1$ A; $dI_G/dt = 5$ A/µs	-	2	-	µs

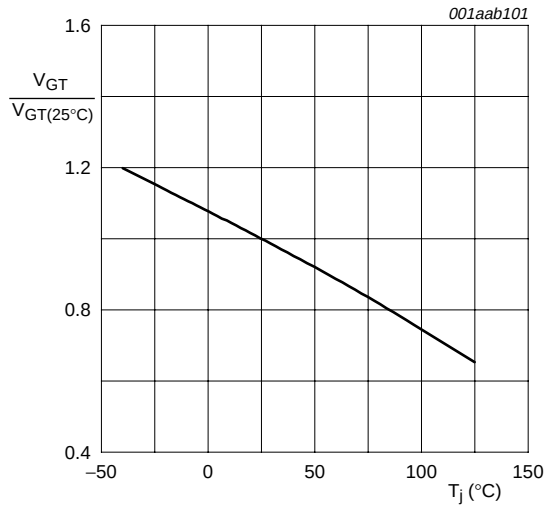
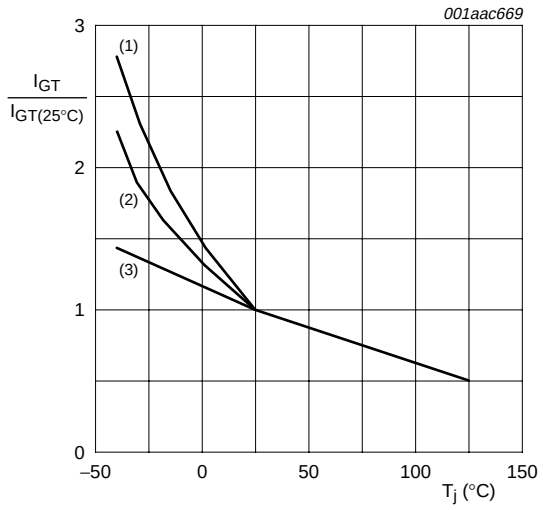
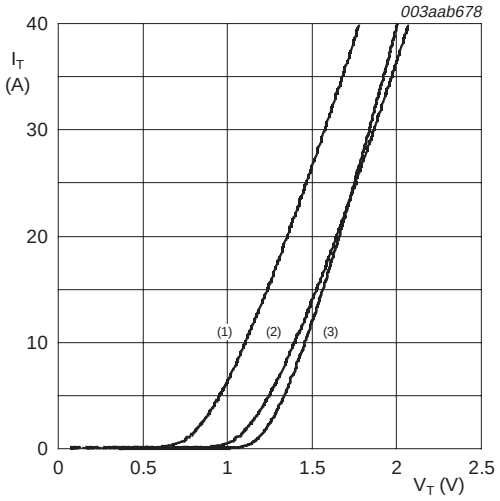


Fig 7. Normalized gate trigger voltage as a function of junction temperature



(1) T2– G–
(2) T2+ G–
(3) T2+ G+

Fig 8. Normalized gate trigger current as a function of junction temperature



V_o = 1.127 V

R_s = 0.027 Ω

(1) T_j = 125 °C; typical values

(2) T_j = 125 °C; maximum values

(3) T_j = 25 °C; maximum values

Fig 9. On-state current as a function of on-state voltage

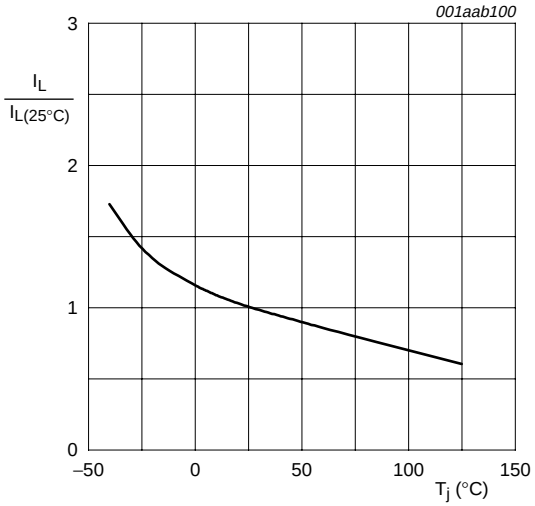


Fig 10. Normalized latching current as a function of junction temperature

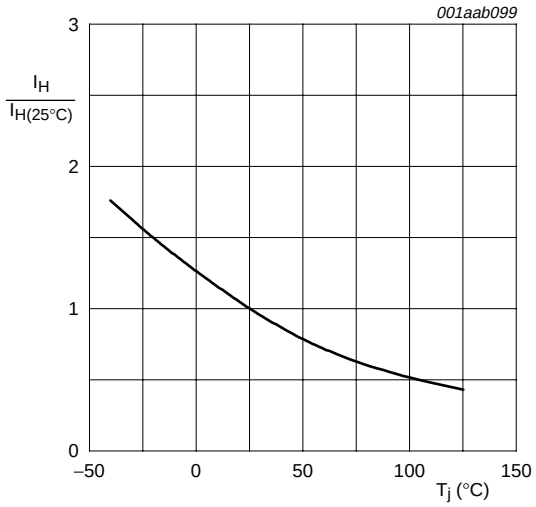
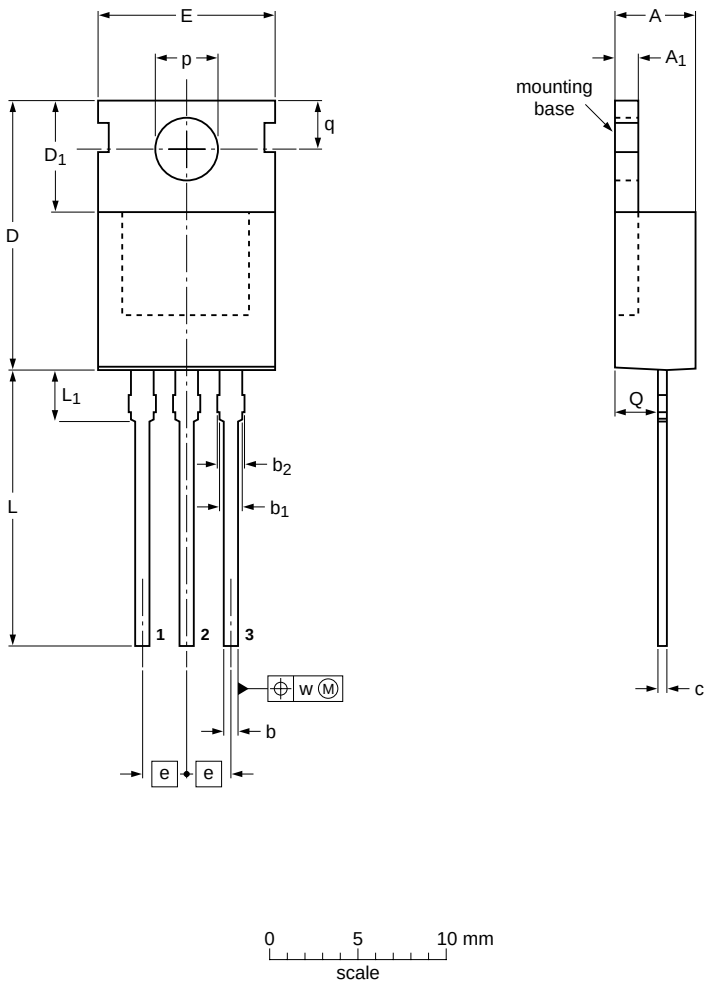


Fig 11. Normalized holding current as a function of junction temperature

9. Package outline

Plastic single-ended package; isolated heatsink mounted; 1 mounting hole; 3-lead TO-220 **SOT78D**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b	b_1	b_2	c	D	D_1 ref	E	e	L	L_1 ref	p	Q	q	w
mm	4.7 4.3	1.40 1.25	0.9 0.6	1.4 1.1	1.72 1.32	0.6 0.4	16.0 15.2	6.5	10.3 9.7	2.54	14.0 12.8	3.0	3.7 3.5	2.6 2.2	3.0 2.7	0.2

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT78D		TO-220				~~07-04-04~~ 07-07-10

Fig 12. Package outline SOT78D (3-lead TO-220)

10. Revision history

Table 8. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BTA312Y_SER_C_1	20070927	Product data sheet	-	-

11. Legal information

11.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

11.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

11.3 Disclaimers

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

General — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of a NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) may cause permanent damage to the device. Limiting values are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of this document is not implied. Exposure to limiting values for extended periods may affect device reliability.

Terms and conditions of sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, including those pertaining to warranty, intellectual property rights infringement and limitation of liability, unless explicitly otherwise agreed to in writing by NXP Semiconductors. In case of any inconsistency or conflict between information in this document and such terms and conditions, the latter will prevail.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

11.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

12. Contact information

For additional information, please visit: **http://www.nxp.com**

For sales office addresses, send an email to: **salesaddresses@nxp.com**

13. Contents

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 27 September 2007

Document identifier: BTA312Y_SER_C_1