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FAIRCHILD

SEMICONDUCTOR®

FDD6696/FDU6696

30V N-Channel PowerTrench$^\partial$ MOSFET

General Description

This N-Channel MOSFET has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low $R_{DS(ON)}$ and fast switching speed.

Applications

- DC/DC converter
- Motor drives

Features

- 50A, 30 V $R_{DS(ON)}$ = 8.0 mΩ @ V_{GS} = 10 V
                $R_{DS(ON)}$ = 10.7 mΩ @ V_{GS} = 4.5 V

- Low gate charge (17nC typical)

- Fast switching

- High performance trench technology for extremely low $R_{DS(ON)}$

G

S

D-PAK
(TO-252)

D

I-PAK
(TO-251AA)

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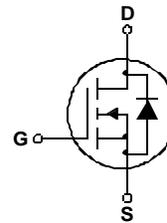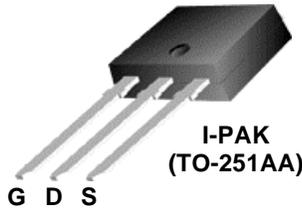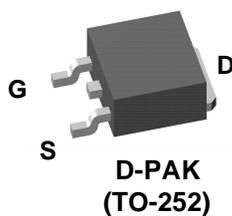
Absolute Maximum Ratings T_A=25°C unless otherwise noted

Symbol	Parameter			Ratings	Units
V_{DSS}	Drain-Source Voltage			30	V
V_{GSS}	Gate-Source Voltage			± 16	
I_D	Continuous Drain Current	@T_C=25°C	(Note 3)	50	A
		@T_A=25°C	(Note 1a)	13	
		Pulsed	(Note 1a)	100	
P_D	Power Dissipation	@T_C=25°C	(Note 3)	52	W
		@T_A=25°C	(Note 1a)	3.8	
		@T_A=25°C	(Note 1b)	1.6	
T_J, T_{STG}	Operating and Storage Junction Temperature Range			−55 to +175	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)		2.9	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)		40	
	Thermal Resistance, Junction-to-Ambient	(Note 1b)		96	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape width	Quantity
FDD6696	FDD6696	D-PAK (TO-252)	13"	12mm	2500 units
FDU6696	FDU6696	I-PAK (TO-251)	Tube	N/A	75

Electrical Characteristics

$T_A = 25°C$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Drain-Source Avalanche Ratings (Note 2)						
E_{AS}	Drain-Source Avalanche Energy	Single Pulse, $V_{DD} = 15$ V, $I_D = 13A$			165	mJ
I_{AS}	Drain-Source Avalanche Current				13	A
Off Characteristics						
BV_{DSS}	Drain–Source Breakdown Voltage	$V_{GS} = 0$ V, $\quad I_D = 250$ µA	30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250$ µA, Referenced to 25°C		23		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 24$ V, $\quad V_{GS} = 0$ V			10	µA
I_{GSSF}	Gate–Body Leakage	$V_{GS} = \pm 16$ V, $\quad V_{DS} = 0$ V			± 100	nA
On Characteristics (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, \quad I_D = 250$ µA	1	2	3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = 250$ µA, Referenced to 25°C		–5		mV/°C
$R_{DS(on)}$	Static Drain–Source On–Resistance	$V_{GS} = 10$ V, $\quad I_D = 13$ A $V_{GS} = 4.5$ V, $\quad I_D = 12$ A $V_{GS} = 10$ V, $\quad I_D = 13$ A, $T_J = 125°C$		6.7 8.6 10.2	8.0 10.7 15.0	mΩ
g_{FS}	Forward Transconductance	$V_{DS} = 5$ V, $\quad I_D = 13$ A		51		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{DS} = 15$ V, $\quad V_{GS} = 0$ V,		1715		pF
C_{oss}	Output Capacitance	$f = 1.0$ MHz		410		pF
C_{rss}	Reverse Transfer Capacitance			180		pF
R_G	Gate Resistance	$V_{GS} = 15$ mV, $\quad f = 1.0$ MHz		1.3		Ω
Switching Characteristics (Note 2)						
$t_{d(on)}$	Turn–On Delay Time	$V_{DD} = 15$ V, $\quad I_D = 13$ A,		13	23	ns
t_r	Turn–On Rise Time	$V_{GS} = 10$ V, $\quad R_{GEN} = 6$ Ω		4	9	ns
$t_{d(off)}$	Turn–Off Delay Time			27	43	ns
t_f	Turn–Off Fall Time			17	31	ns
Q_g	Total Gate Charge	$V_{DS} = 15V$, $\quad I_D = 13$ A,		17	24	nC
Q_{gs}	Gate–Source Charge	$V_{GS} = 5$ V		5		nC
Q_{gd}	Gate–Drain Charge			6		nC
Drain–Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain–Source Diode Forward Current				13	A
V_{SD}	Drain–Source Diode Forward Voltage	$V_{GS} = 0$ V, $\quad I_S = 13$ A $\quad$ (Note 2)		0.8	1.2	V
t_{rr}	Diode Reverse Recovery Time	$I_F = 13$ A,		27		nS
Q_{rr}	Diode Reverse Recovery Charge	$di_F/d_t = 100$ A/µs		15		nC

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.
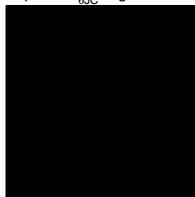
a) $R_{\theta JA} = 40°C/W$ when mounted on a $1in^2$ pad of 2 oz copper

b) $R_{\theta JA} = 96°C/W$ when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < 300µs, Duty Cycle < 2.0%

3. Maximum current is calculated as: $\sqrt{\dfrac{P_D}{R_{DS(ON)}}}$ where P_D is maximum power dissipation at $T_C = 25°C$ and $R_{DS(on)}$ is at $T_{J(max)}$ and $V_{GS} = 10V$. Package current limitation is 21A
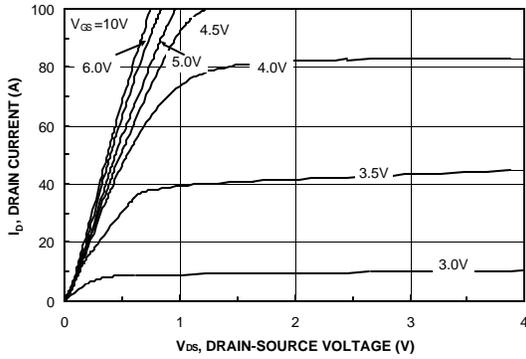
Typical Characteristics
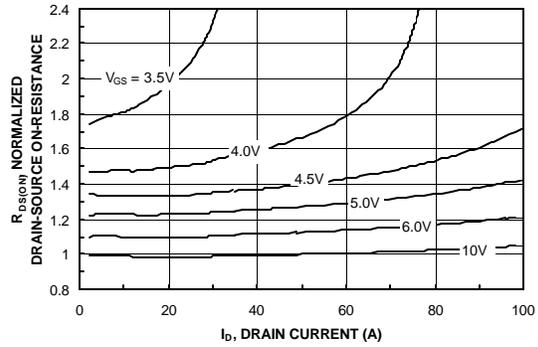
Figure 1. On-Region Characteristics

Figure 2. On-Resistance Variation with Drain Current and Gate Voltage
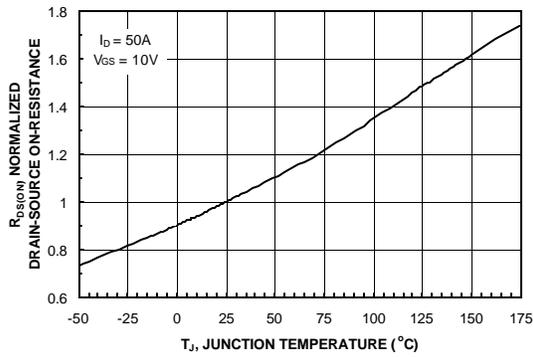
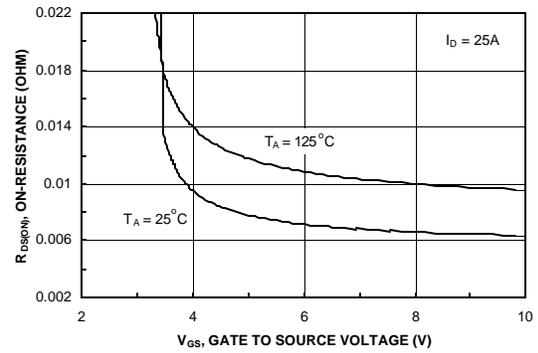**Figure 3. On-Resistance Variation with Temperature**
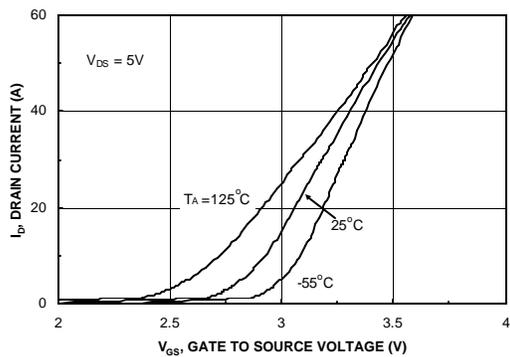
Figure 4. On-Resistance Variation with Gate-to-Source Voltage
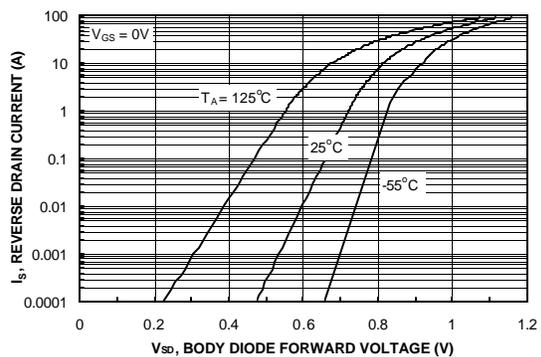
Figure 5. Transfer Characteristics

Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature
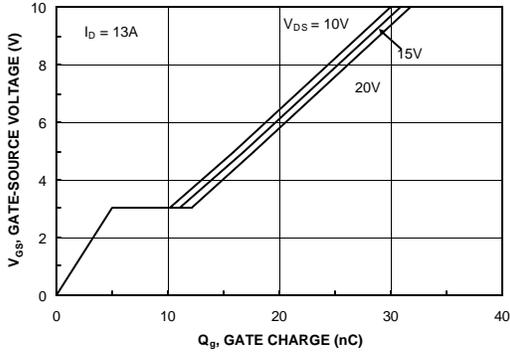
Typical Characteristics
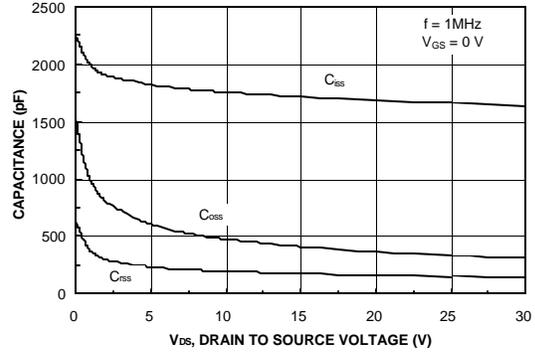

Figure 7. Gate Charge Characteristics

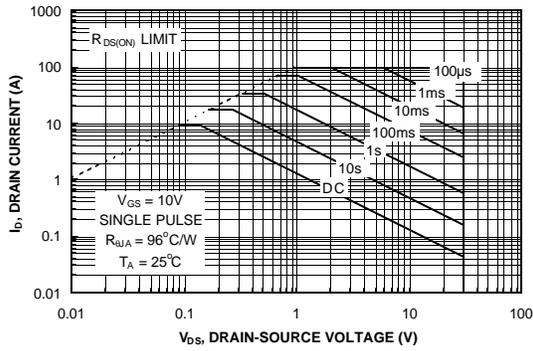Figure 8. Capacitance Characteristics
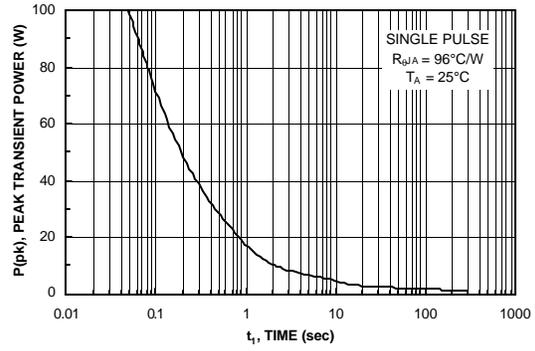

Figure 9. Maximum Safe Operating Area

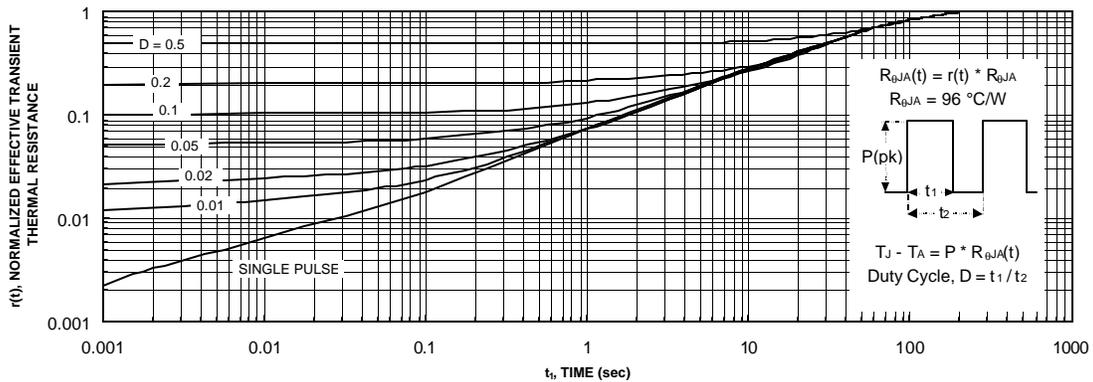Figure 10. Single Pulse Maximum Power Dissipation

Figure 11. Transient Thermal Response Curve

Thermal characterization performed using the conditions described in Note 1b.
Transient thermal response will change depending on the circuit board design.

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