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AD7691 FMC-SDP Interposer & Evaluation Board / Xilinx KC705 Reference Design

Supported Devices

- AD7691

Evaluation Boards

- EVAL-AD7691SDZ

Overview

This document presents the steps to setup an environment for using the **EVAL-AD7691SDZ** evaluation board together with the Xilinx KC705 FPGA board and the Xilinx Embedded Development Kit (EDK). Below is presented a picture of the EVAL-AD7691SDZ Evaluation Board with the Xilinx KC705 board.

For component evaluation and performance purposes, as opposed to quick prototyping, the user is directed to use the part evaluation setup. This consists of:

- 1. A controller board like the SDP-B (EVAL-SDP-CS1Z)
- 2. The component SDP compatible product evaluation board
- 3. Corresponding PC software (shipped with the product evaluation board)

The SDP-B controller board is part of Analog Devices System Demonstration Platform (SDP). It provides a high speed USB 2.0 connection from the PC to the component evaluation board. The PC runs the evaluation software. Each evaluation board, which is an SDP compatible daughter board, includes the necessary installation file required for performance testing.

Note: it is expected that the analog performance on the two platforms may differ.

28 Sep 2012 09:32 · Adrian Costina

Below is presented a picture of **SDP-B** Controller Board with the **EVAL-AD7691SDZ** Evaluation Board.

The AD7691 is an 18-bit, charge redistribution, successive approximation, analog-to-digital converter (ADC) that operates from a single power supply, VDD, between 2.3 V and 5 V. It contains a low power, high speed, 18-bit sampling ADC with no missing codes, an internal conversion clock, and a versatile serial interface port. On the CNV rising edge, it samples the voltage difference between the IN+ and IN− pins. The voltages on these pins swing in opposite phases between 0 V and REF. The reference voltage, REF, is applied externally and can be set up to the supply voltage. The power of the AD7691 scales linearly with the throughput.

The EVAL-AD7691SDZ evaluation board is a member of a growing number of boards available for the SDP. It was designed to help customers evaluate performance or quickly prototype new AD7691 circuits and reduce design time. When using this evaluation board with the SDP board or Xilinx KC705 board, apply +7.5V as +Vs, a voltage between -2V and -5V as -Vs and +2.5V as VDD.

More information

- AD7691 Product Info - pricing, samples, datasheet
- EVAL-AD7691SDZ evaluation board user guide

- Xilinx KC705 FPGA board

Getting Started

The first objective is to ensure that you have all of the items needed and to install the software tools so that you are ready to create and run the evaluation project.

Required Hardware

- Xilinx KC705 FPGA board
- FMC-SDP adapter board
- **EVAL-AD7691SDZ** evaluation board

Required Software

- Xilinx ISE 13.4
- A UART terminal (ex. TeraTerm / Hyperterminal).

Downloads

- Reference Design Files

The following table presents a short description the reference design archive contents.

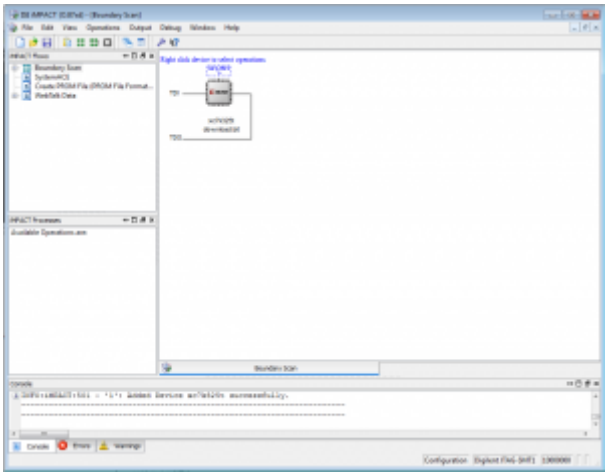
Folder	Description
Bit	Contains the KC705 configuration file that can be used to program the system for quick evaluation.
DataCapture	Contains the script used to read data from the ADC and save it into a file on the PC.
Hdl	Contains the HDL driver for the AD7691 ADC.
Microblaze	Contains the EDK 13.2 project for the Microblaze softcore that will be implemented in the KC705 FPGA.
Software	Contains the source files of the software project that will be run by the Microblaze processor.

Run the Demonstration Project

Hardware Setup

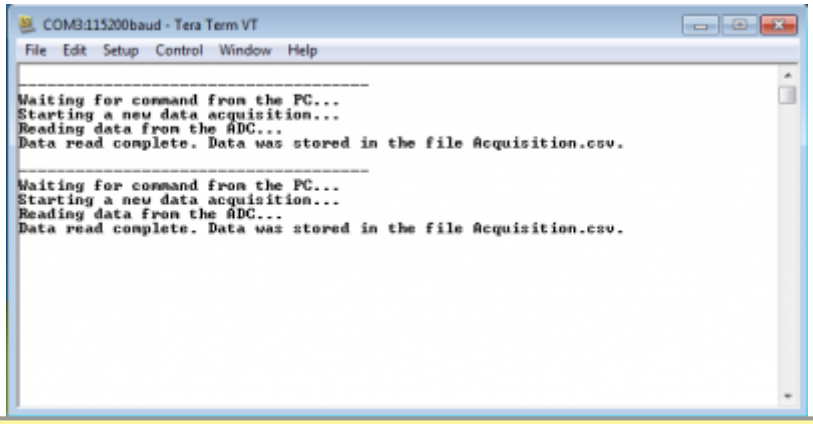
Before connecting the ADI evaluation board to the Xilinx KC705 make sure that the VADJ_FPGA voltage of the KC705 is set to 3.3V. For more details on how to change the setting for VADJ_FPGA visit the Xilinx KC705 product page.

- Use the FMC-SDP interposer to connect the ADI evaluation board to the Xilinx KC705 board on the FMC LPC connector.
- Connect the JTAG and UART cables to the KC705 and power up the FPGA board.
- Start IMPACT, and double click "*Boundary Scan*". Right click and select *Initialize Chain*. The program should recognize the Kintex 7 device (see screenshot below).



- Program the KC705 FPGA using the "*Bit/download.bit*" file provided in the reference design archive.
- Power the ADI evaluation board.
- Start a UART terminal and set the baud rate to 115200 bps.

At this point everything is set up and it is possible to start the evaluation of the ADI hardware. To capture data from the ADC run the *data_capture.bat* script located in the *DataCapture* folder from the reference design .zip file. Every time the script is run a new batch of 8192 samples are read from the ADC at the ADC's maximum sampling rate and saved into the *Acquisition.csv* file located in the same folder as the data capture script. On the UART terminal messages will be displayed to show the status of the program running on the FPGA as shown in the picture below.



The first time the data capture script is run it is possible that an error will occur while the script is trying to connect to the system. Just run the script again and the error shouldn't appear anymore.

More information

- ask questions about the FPGA reference design
- Example questions:
  - *An error occurred while fetching this feed:* http://ez.analog.com/community/feeds/allcontent/atom?community=2061

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