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May 2015

FDMS8820

N-Channel PowerTrench[®] MOSFET 30 V, 160 A, 2.0 mΩ

Features

- Max $r_{DS(on)}$ = 2.0 mΩ at $V_{GS} = 10\text{ V}$, $I_D = 28\text{ A}$
- Max $r_{DS(on)}$ = 2.4 mΩ at $V_{GS} = 4.5\text{ V}$, $I_D = 25\text{ A}$
- Advanced Package and Silicon combination for low $r_{DS(on)}$ and high efficiency
- Next generation enhanced body diode technology, engineered for soft recovery
- MSL1 robust package design
- 100% UIL tested
- RoHS Compliant

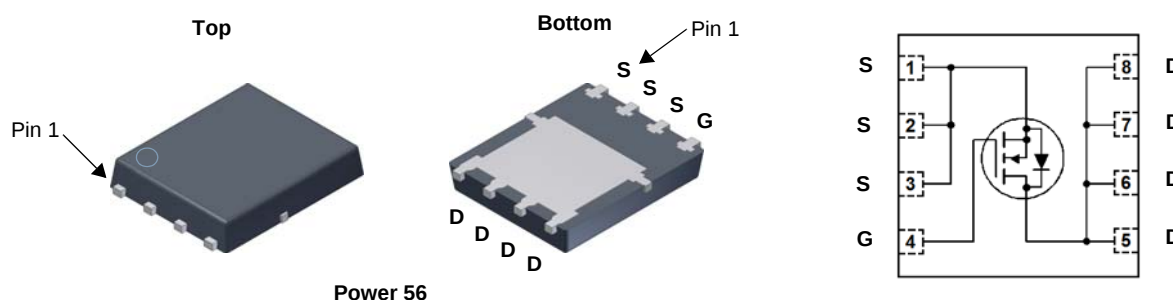


General Description

This N-Channel MOSFET has been designed specifically to improve the overall efficiency and to minimize switch node ringing of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low $r_{DS(on)}$, fast switching speed and body diode reverse recovery performance.

Applications

- VRM Vcore Switching For Desktop And Server
- OringFET / Load Switching
- DC-DC Conversion



MOSFET Maximum Ratings $T_A = 25\text{ }^{\circ}\text{C}$ unless otherwise noted.

Symbol	Parameter	Ratings	Units
V_{DS}	Drain to Source Voltage	30	V
V_{GS}	Gate to Source Voltage (Note 4)	± 20	V
I_D	Drain Current -Continuous $T_C = 25\text{ }^{\circ}\text{C}$ (Note 6)	160	A
	-Continuous $T_C = 100\text{ }^{\circ}\text{C}$ (Note 6)	101	
	-Continuous $T_A = 25\text{ }^{\circ}\text{C}$ (Note 1a)	28	
	-Pulsed (Note 5)	634	
E_{AS}	Single Pulse Avalanche Energy (Note 3)	294	mJ
P_D	Power Dissipation $T_C = 25\text{ }^{\circ}\text{C}$	78	W
	Power Dissipation $T_A = 25\text{ }^{\circ}\text{C}$ (Note 1a)	2.5	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	$^{\circ}\text{C}$

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	1.6	$^{\circ}\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	50	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMS8820	FDMS8820	Power 56	13 "	12 mm	3000 units

Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\ \mu\text{A}$, $V_{GS} = 0\ \text{V}$	30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, referenced to 25°C		19		mV/ $^\circ\text{C}$
I_{BSS}	Zero Gate Voltage Drain Current	$V_{DS} = 24\ \text{V}$, $V_{GS} = 0\ \text{V}$			1	μA
I_{GSS}	Gate to Source Leakage Current, Forward	$V_{GS} = 20\ \text{V}$, $V_{DS} = 0\ \text{V}$			100	nA

On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250\ \mu\text{A}$	1.2	1.5	2.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, referenced to 25°C		-6		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\ \text{V}$, $I_D = 28\ \text{A}$		1.4	2.0	m Ω
		$V_{GS} = 4.5\ \text{V}$, $I_D = 25\ \text{A}$		1.8	2.4	
		$V_{GS} = 10\ \text{V}$, $I_D = 28\ \text{A}$, $T_J = 125^\circ\text{C}$		2.0	2.8	
g_{FS}	Forward Transconductance	$V_{DS} = 5\ \text{V}$, $I_D = 28\ \text{A}$		76		S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 15\ \text{V}$, $V_{GS} = 0\ \text{V}$, $f = 1\ \text{MHz}$		3995	5315	pF
C_{oss}	Output Capacitance			1295	1725	pF
C_{rss}	Reverse Transfer Capacitance			177	270	pF
R_g	Gate Resistance		0.1	1.1	2.5	Ω

Switching Characteristics

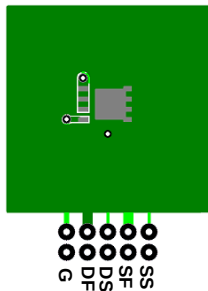
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 15\ \text{V}$, $I_D = 28\ \text{A}$, $V_{GS} = 10\ \text{V}$, $R_{GEN} = 6\ \Omega$		14	25	ns
t_r	Rise Time			7.7	16	ns
$t_{d(off)}$	Turn-Off Delay Time			41	66	ns
t_f	Fall Time			6.4	13	ns
Q_g	Total Gate Charge	$V_{GS} = 0\ \text{V}$ to $10\ \text{V}$	$V_{DD} = 15\ \text{V}$, $I_D = 28\ \text{A}$	63	88	nC
Q_g	Total Gate Charge	$V_{GS} = 0\ \text{V}$ to $4.5\ \text{V}$		30	42	nC
Q_{gs}	Gate to Source Charge			9.8		nC
Q_{gd}	Gate to Drain "Miller" Charge			8.2		nC

Drain-Source Diode Characteristics

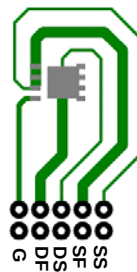
V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0\ \text{V}$, $I_S = 2.0\ \text{A}$ (Note 2)		0.7	1.1	V
		$V_{GS} = 0\ \text{V}$, $I_S = 28\ \text{A}$ (Note 2)		0.8	1.2	
t_{rr}	Reverse Recovery Time	$I_F = 28\ \text{A}$, $di/dt = 100\ \text{A}/\mu\text{s}$		43	69	ns
Q_{rr}	Reverse Recovery Charge			27	43	nC

Notes:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta CA}$ is determined by the user's board design.



a. 50 $^\circ\text{C}/\text{W}$ when mounted on a 1 in² pad of 2 oz copper



b. 125 $^\circ\text{C}/\text{W}$ when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300 μs , Duty cycle < 2.0%.

3. E_{AS} of 294 mJ is based on starting $T_J = 25^\circ\text{C}$; N-ch: $L = 3\ \text{mH}$, $I_{AS} = 14\ \text{A}$, $V_{DD} = 30\ \text{V}$, $V_{GS} = 10\ \text{V}$. 100% test at $L = 0.1\ \text{mH}$, $I_{AS} = 45\ \text{A}$.

4. As an N-ch device, the negative V_{GS} rating is for low duty cycle pulse occurrence only. No continuous rating is implied.

5. Pulsed I_D please refer to SOA curve for more details.

6. Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted.

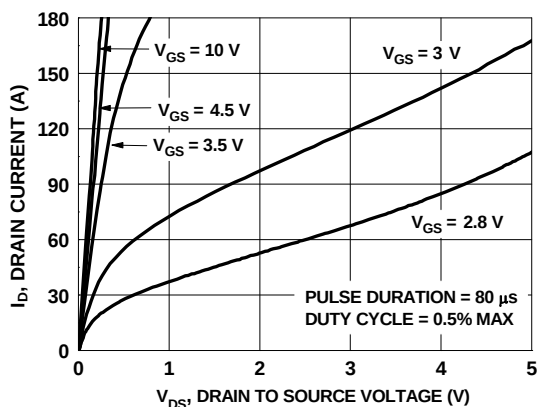


Figure 1. On Region Characteristics

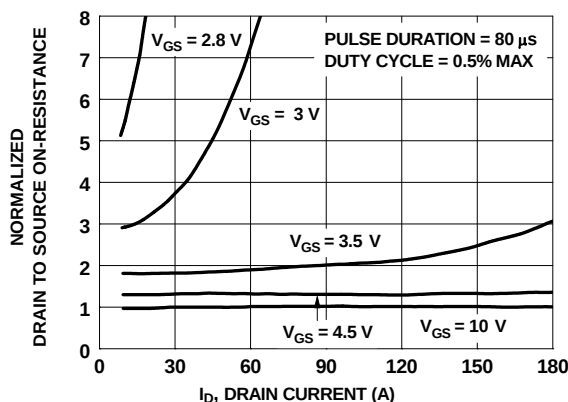


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

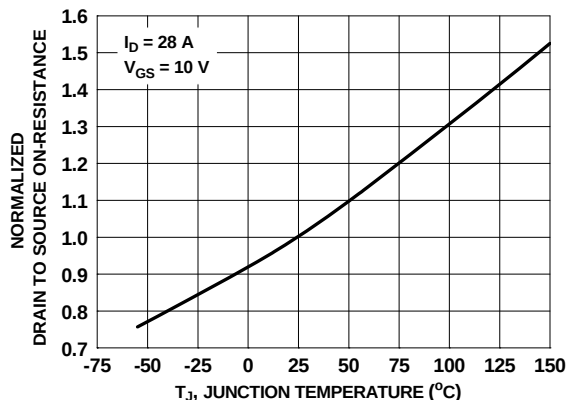


Figure 3. Normalized On Resistance vs. Junction Temperature

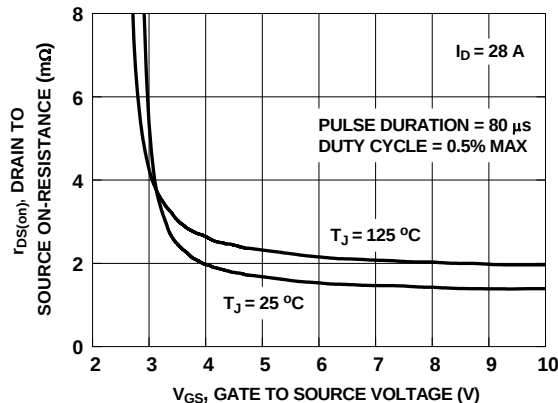


Figure 4. On-Resistance vs. Gate to Source Voltage

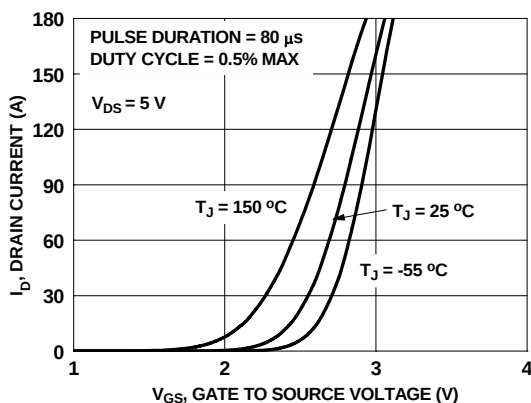


Figure 5. Transfer Characteristics

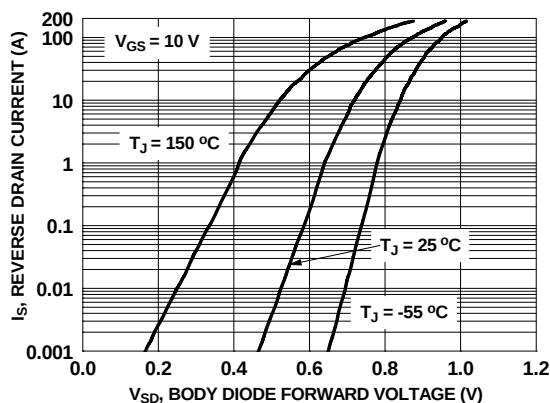


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted.

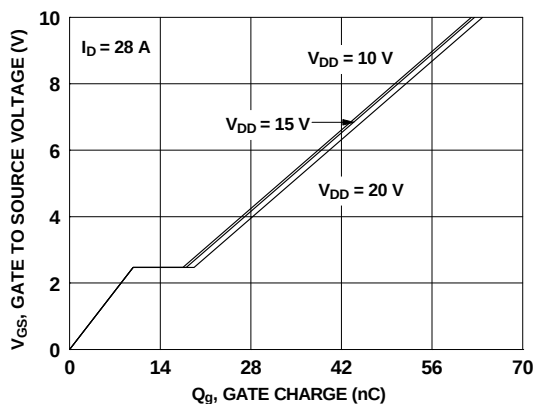


Figure 7. Gate Charge Characteristics

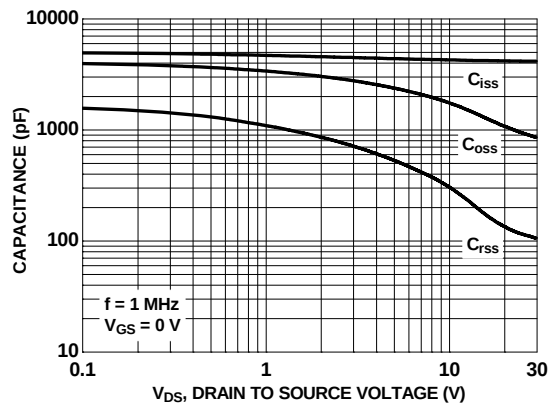


Figure 8. Capacitance vs. Drain to Source Voltage

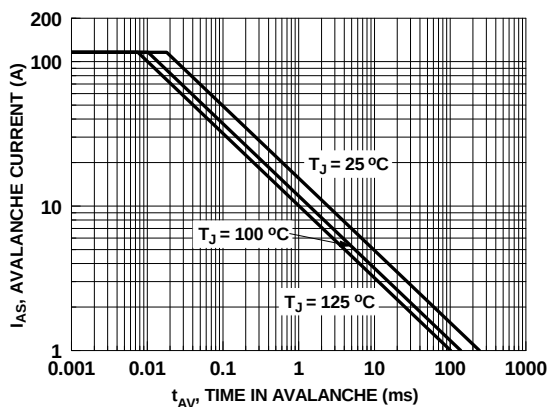


Figure 9. Unclamped Inductive Switching Capability

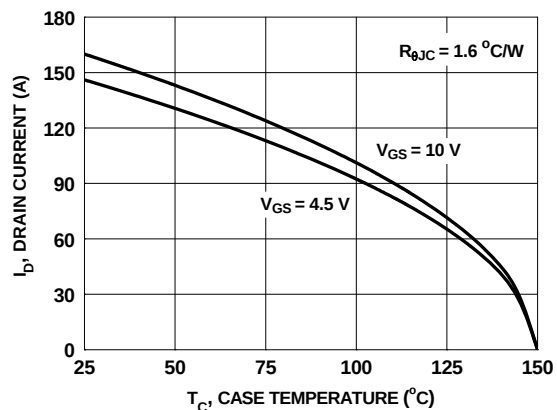


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

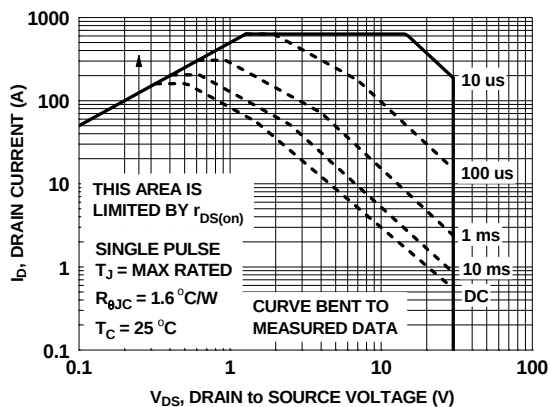


Figure 11. Forward Bias Safe Operating Area

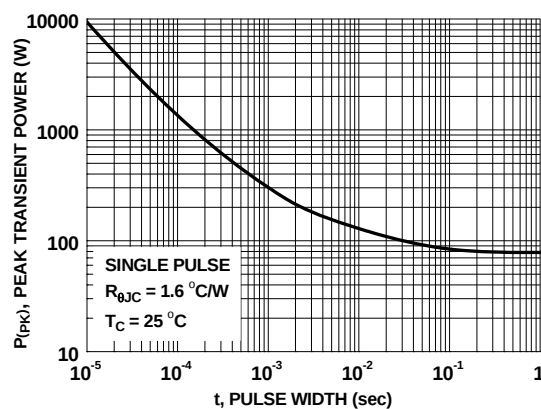


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics $T_J = 25\text{ }^{\circ}\text{C}$ unless otherwise noted.

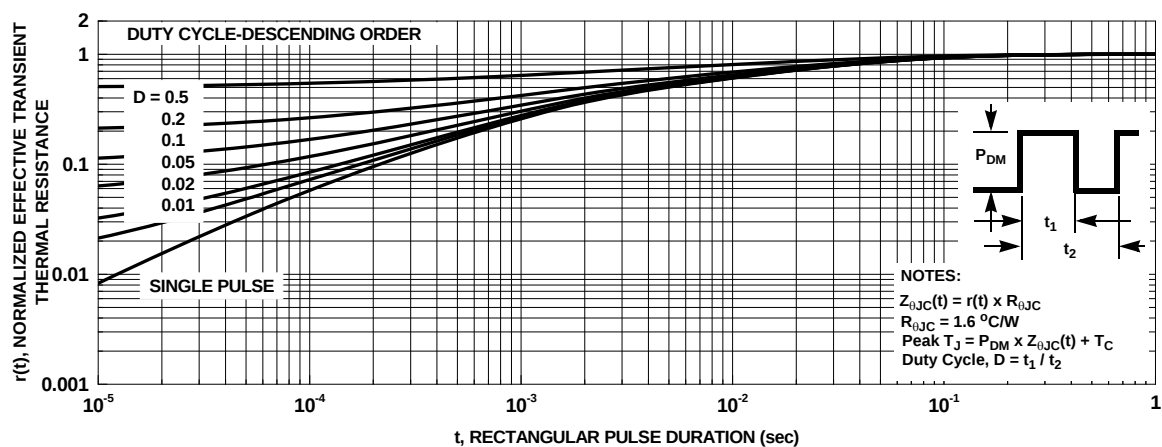
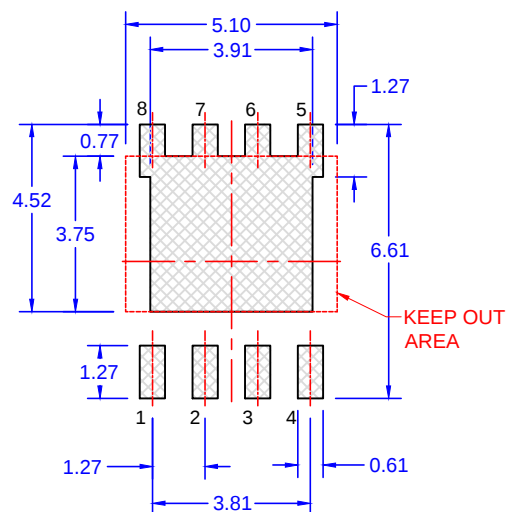


Figure 13. Junction-to-Case Transient Thermal Response Curve

A mechanical drawing of a rectangular package. The drawing shows a top-down view of the package with a central crosshair indicating the center. The package has a width of 5.10 and a height of 6.15. The center of the package is marked with a red dashed line. The package is labeled with 'PKG C' at the top center and 'PKG C' on the left side. The package has four pins, numbered 1, 4, 5, and 8, located at the corners. The pins are labeled with their respective numbers: 1 at the bottom left, 4 at the bottom right, 5 at the top right, and 8 at the top left. The package is labeled with 'A' at the top right and 'B' at the bottom right. The package is labeled with '5.10' at the top and '6.15' at the bottom. The package is labeled with 'PKG C' at the top center and 'PKG C' on the left side.

SEE
DETAIL B

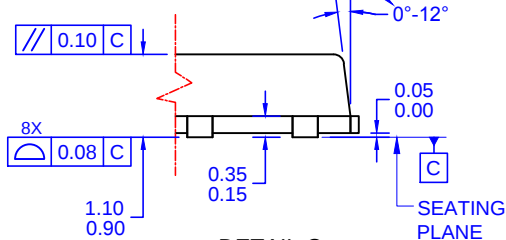
5.85
5.65



5.00
4.80

SEE
DETAIL C

OPTIONAL DRAFT
ANGLE MAY APPEAR
ON FOUR SIDES
OF THE PACKAGE



Technical drawing of a mechanical part with dimensions and a 0°-12° taper.

[illegible]

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