

1. General description

Planar passivated guaranteed commutation triac in a SOT223 surface mountable plastic package for use in motor control circuits or with other highly inductive loads. This triac balances the requirements of commutation performance and gate sensitivity and is intended for interfacing with low power drivers, including micro controllers.

2. Features and benefits

- 3Q technology for improved noise immunity
- Direct triggering from low power drivers and logic ICs
- High commutation capability with sensitive gate
- High immunity to false turn-on by dV/dt with sensitive gate
- Planar passivated for voltage ruggedness and reliability
- Sensitive gate for easy logic level triggering
- Surface mountable package

3. Applications

- General purpose motor controls
- Small loads in washing machines
- Rectifier-fed DC inductive loads e.g. DC motors and solenoids

4. Quick reference data

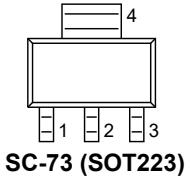
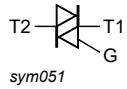
Table 1. Quick reference data

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-------------------------------|--------------------------------------|--|-----|-----|-----|------------------|
| V_{DRM} | repetitive peak off-state voltage | | - | - | 600 | V |
| $I_{T(RMS)}$ | RMS on-state current | full sine wave; $T_{sp} \leq 108^\circ\text{C}$; Fig. 1 ; Fig. 2 ; Fig. 3 | - | - | 1 | A |
| I_{TSM} | non-repetitive peak on-state current | full sine wave; $T_{j(\text{init})} = 25^\circ\text{C}$; $t_p = 16.7\text{ ms}$ | - | - | 11 | A |
| | | full sine wave; $T_{j(\text{init})} = 25^\circ\text{C}$; $t_p = 20\text{ ms}$; Fig. 4 ; Fig. 5 | - | - | 10 | A |
| T_j | junction temperature | | - | - | 125 | $^\circ\text{C}$ |
| Static characteristics | | | | | | |
| I_{GT} | gate trigger current | $V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2+ G+; $T_j = 25^\circ\text{C}$; Fig. 9 | - | - | 10 | mA |
| | | $V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2+ G-; $T_j = 25^\circ\text{C}$; Fig. 9 | - | - | 10 | mA |

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|--------------------------------|---------------------------------------|---|--|-----|-----|-----|------------------|
| | | $V_D = 12 \text{ V}$; $I_T = 0.1 \text{ A}$; T2- G-; $T_j = 25 \text{ }^\circ\text{C}$; Fig. 9 | | - | - | 10 | mA |
| I_H | holding current | $V_D = 12 \text{ V}$; $T_j = 25 \text{ }^\circ\text{C}$; Fig. 11 | | - | - | 12 | mA |
| V_T | on-state voltage | $I_T = 2 \text{ A}$; $T_j = 25 \text{ }^\circ\text{C}$; Fig. 12 | | - | 1.2 | 1.5 | V |
| Dynamic characteristics | | | | | | | |
| dV_D/dt | rate of rise of off-state voltage | $V_{DM} = 600 \text{ V}$; $T_j = 125 \text{ }^\circ\text{C}$; (67% of V_{DRM}); exponential waveform; gate open circuit | | 30 | - | - | V/ μs |
| dI_{com}/dt | rate of change of commutating current | $V_D = 400 \text{ V}$; $T_j = 125 \text{ }^\circ\text{C}$; $I_{T(RMS)} = 1 \text{ A}$; $dV_{com}/dt = 20 \text{ V}/\mu\text{s}$; (snubberless condition); gate open circuit | | 2 | - | - | A/ms |

5. Pinning information

Table 2. Pinning information

| Pin | Symbol | Description | Simplified outline | Graphic symbol |
|-----|--------|---|---|--|
| 1 | T1 | main terminal 1 | | |
| 2 | T2 | main terminal 2 | | |
| 3 | G | gate | | |
| 4 | mb | mounting base; connected to main terminal 2 |  SC-73 (SOT223) |  sym051 |

6. Ordering information

Table 3. Ordering information

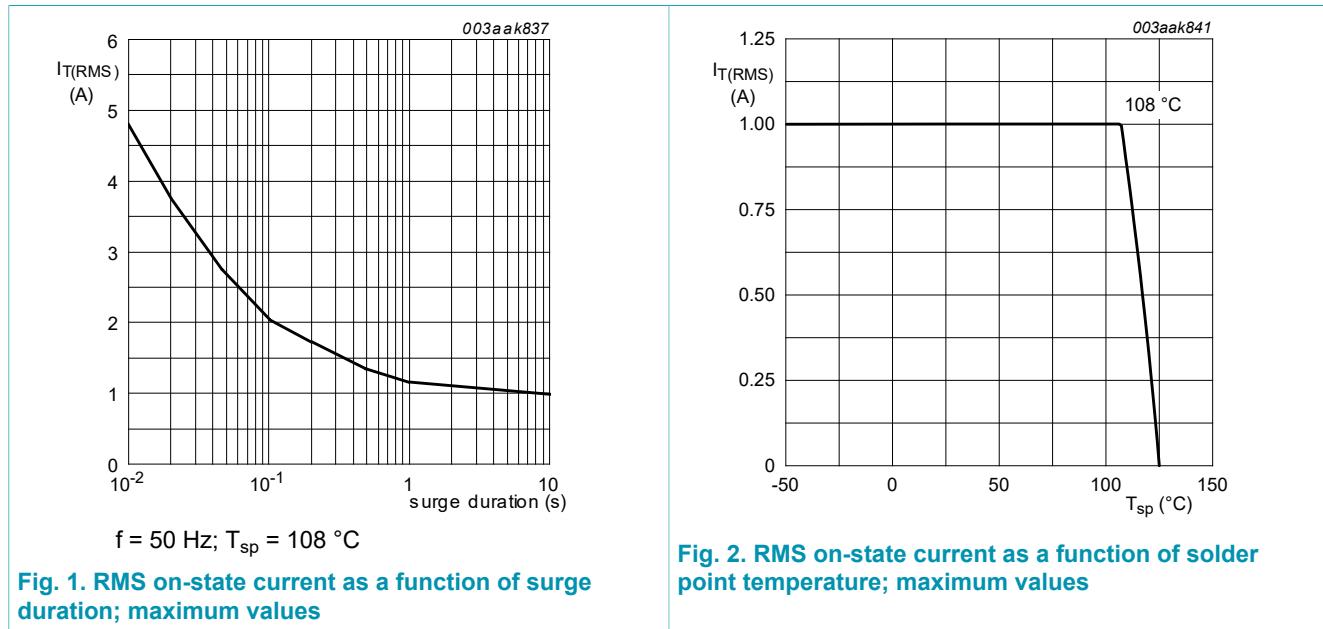
| Type number | Package | | |
|--------------|---------|--|---------|
| | Name | Description | Version |
| BTA204W-600E | SC-73 | plastic surface-mounted package with increased heatsink; 4 leads | SOT223 |

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|--------------|--------------------------------------|--|-----|-----|------------------------|
| V_{DRM} | repetitive peak off-state voltage | | - | 600 | V |
| $I_{T(RMS)}$ | RMS on-state current | full sine wave; $T_{sp} \leq 108^\circ\text{C}$; Fig. 1 ; Fig. 2 ; Fig. 3 | - | 1 | A |
| I_{TSM} | non-repetitive peak on-state current | full sine wave; $T_{j(\text{init})} = 25^\circ\text{C}$; $t_p = 16.7\text{ ms}$ | - | 11 | A |
| | | full sine wave; $T_{j(\text{init})} = 25^\circ\text{C}$; $t_p = 20\text{ ms}$; Fig. 4 ; Fig. 5 | - | 10 | A |
| I^2t | I^2t for fusing | $t_p = 10\text{ ms}$; SIN | - | 0.5 | A^2s |
| dI_T/dt | rate of rise of on-state current | $I_G = 0.2\text{ A}$ | - | 100 | $\text{A}/\mu\text{s}$ |
| I_{GM} | peak gate current | | - | 2 | A |
| P_{GM} | peak gate power | | - | 5 | W |
| $P_{G(AV)}$ | average gate power | over any 20ms period | - | 0.5 | W |
| T_{stg} | storage temperature | | -40 | 150 | $^\circ\text{C}$ |
| T_j | junction temperature | | - | 125 | $^\circ\text{C}$ |



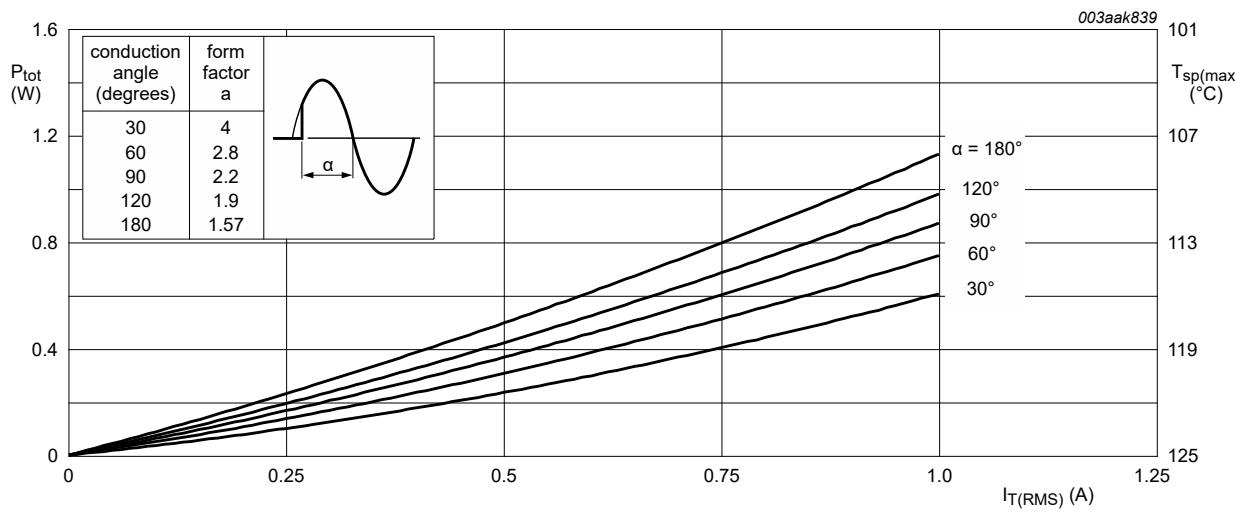


Fig. 3. Total power dissipation as a function of RMS on-state current; maximum values

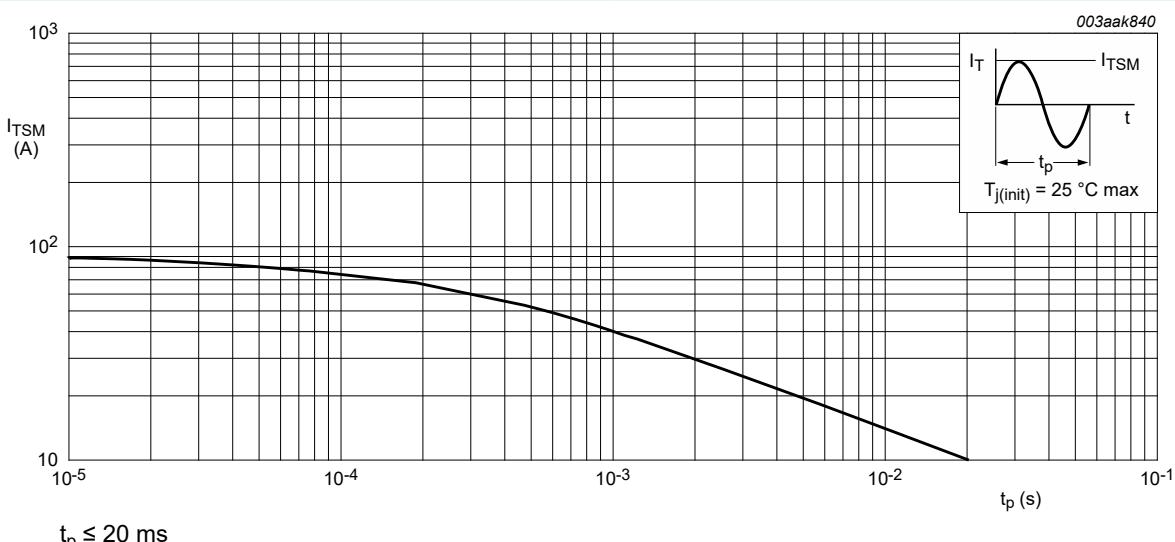


Fig. 4. Non-repetitive peak on-state current as a function of pulse width; maximum values

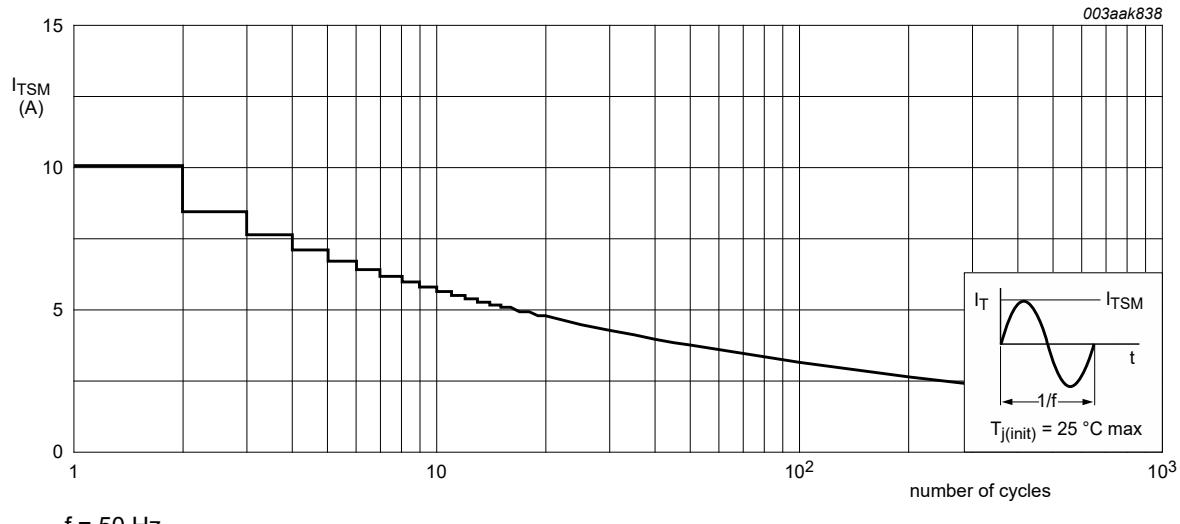


Fig. 5. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values

8. Thermal characteristics

Table 5. Thermal characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------------|--|---|-----|-----|-----|------|
| $R_{th(j-sp)}$ | thermal resistance from junction to solder point | full cycle or half cycle; Fig. 6 | - | - | 15 | K/W |
| $R_{th(j-a)}$ | thermal resistance from junction to ambient free air | in free air; printed circuit board mounted; minimum footprint; Fig. 7 | - | 156 | - | K/W |
| | | in free air; printed circuit board mounted; pad area; Fig. 8 | - | 70 | - | K/W |

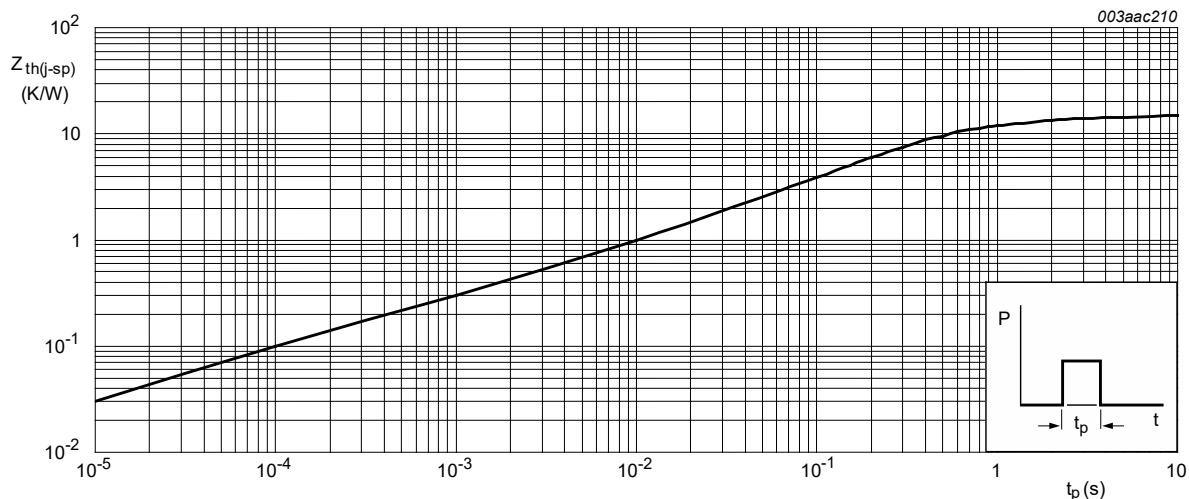
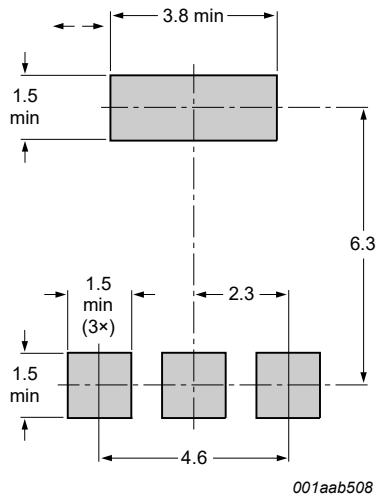
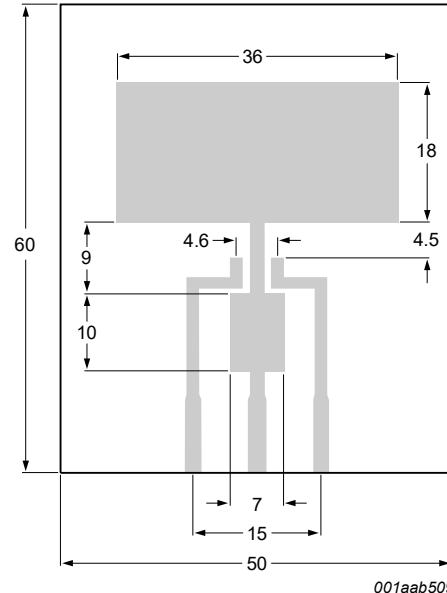


Fig. 6. Transient thermal impedance from junction to solder point as a function of pulse width



All dimensions are in mm

Fig. 7. Minimum footprint SOT223



All dimensions are in mm

Printed circuit board:
FR4 epoxy glass (1.6 mm thick), copper laminate
(35 μ m thick)

Fig. 8. Printed circuit board pad area: SOT223

9. Characteristics

Table 6. Characteristics

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|--------------------------------|---------------------------------------|--|--|------|-----|-----|------------|
| Static characteristics | | | | | | | |
| I_{GT} | gate trigger current | $V_D = 12 \text{ V}$; $I_T = 0.1 \text{ A}$; $T2+ G+$; $T_j = 25 \text{ }^\circ\text{C}$; Fig. 9 | | - | - | 10 | mA |
| | | $V_D = 12 \text{ V}$; $I_T = 0.1 \text{ A}$; $T2+ G-$; $T_j = 25 \text{ }^\circ\text{C}$; Fig. 9 | | - | - | 10 | mA |
| | | $V_D = 12 \text{ V}$; $I_T = 0.1 \text{ A}$; $T2- G-$; $T_j = 25 \text{ }^\circ\text{C}$; Fig. 9 | | - | - | 10 | mA |
| I_L | latching current | $V_D = 12 \text{ V}$; $I_G = 0.1 \text{ A}$; $T2+ G-$; $T_j = 25 \text{ }^\circ\text{C}$; Fig. 10 | | - | - | 12 | mA |
| | | $V_D = 12 \text{ V}$; $I_G = 0.1 \text{ A}$; $T2+ G+$; $T_j = 25 \text{ }^\circ\text{C}$; Fig. 10 | | - | - | 18 | mA |
| | | $V_D = 12 \text{ V}$; $I_G = 0.1 \text{ A}$; $T2- G-$; $T_j = 25 \text{ }^\circ\text{C}$; Fig. 10 | | - | - | 12 | mA |
| I_H | holding current | $V_D = 12 \text{ V}$; $T_j = 25 \text{ }^\circ\text{C}$; Fig. 11 | | - | - | 12 | mA |
| V_T | on-state voltage | $I_T = 2 \text{ A}$; $T_j = 25 \text{ }^\circ\text{C}$; Fig. 12 | | - | 1.2 | 1.5 | V |
| V_{GT} | gate trigger voltage | $V_D = 12 \text{ V}$; $I_T = 0.1 \text{ A}$; $T_j = 25 \text{ }^\circ\text{C}$; Fig. 13 | | - | 0.7 | 1 | V |
| | | $V_D = 400 \text{ V}$; $I_T = 0.1 \text{ A}$; $T_j = 125 \text{ }^\circ\text{C}$; Fig. 13 | | 0.25 | 0.4 | - | V |
| I_D | off-state current | $V_D = 600 \text{ V}$; $T_j = 125 \text{ }^\circ\text{C}$ | | - | 0.1 | 0.5 | mA |
| Dynamic characteristics | | | | | | | |
| dV_D/dt | rate of rise of off-state voltage | $V_{DM} = 600 \text{ V}$; $T_j = 125 \text{ }^\circ\text{C}$; (67% of V_{DRM}); exponential waveform; gate open circuit | | 30 | - | - | V/ μ s |
| dl_{com}/dt | rate of change of commutating current | $V_D = 400 \text{ V}$; $T_j = 125 \text{ }^\circ\text{C}$; $I_{T(RMS)} = 1 \text{ A}$; $dV_{com}/dt = 20 \text{ V}/\mu\text{s}$; (snubberless condition); gate open circuit | | 2 | - | - | A/ms |

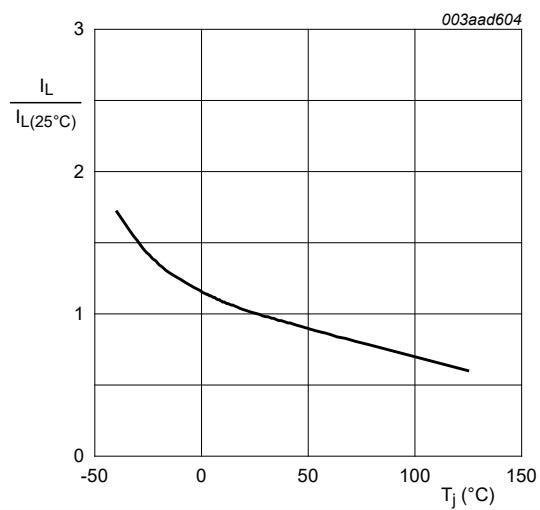
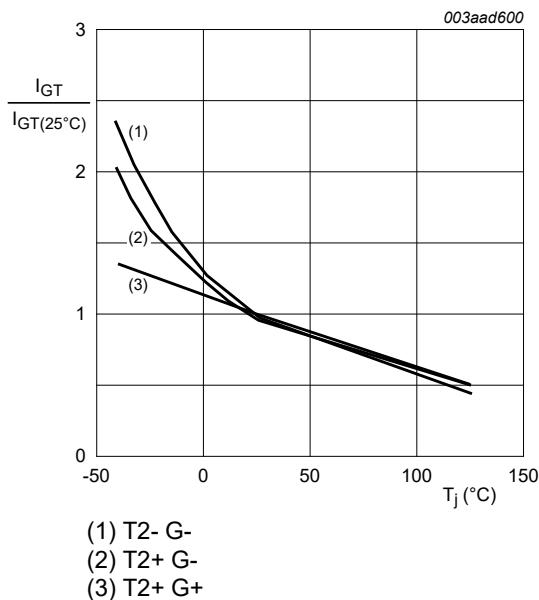


Fig. 10. Normalized latching current as a function of junction temperature

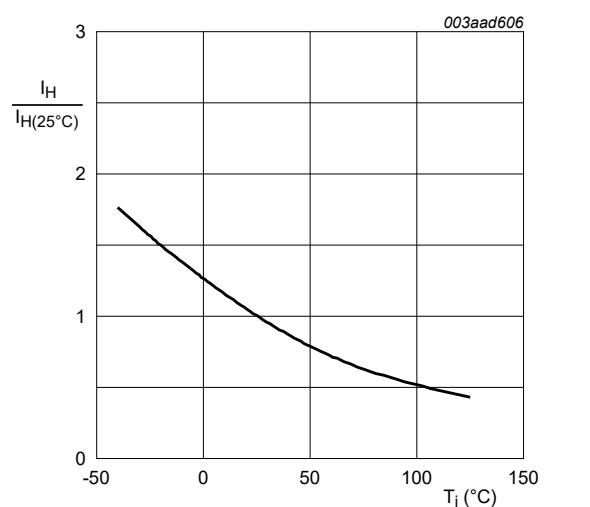


Fig. 11. Normalized holding current as a function of junction temperature

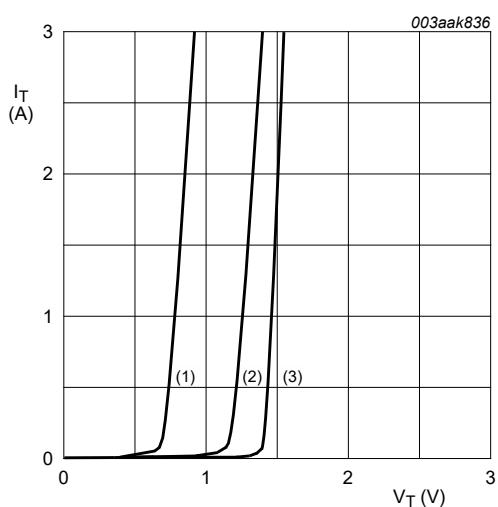


Fig. 12. On-state current as a function of on-state voltage

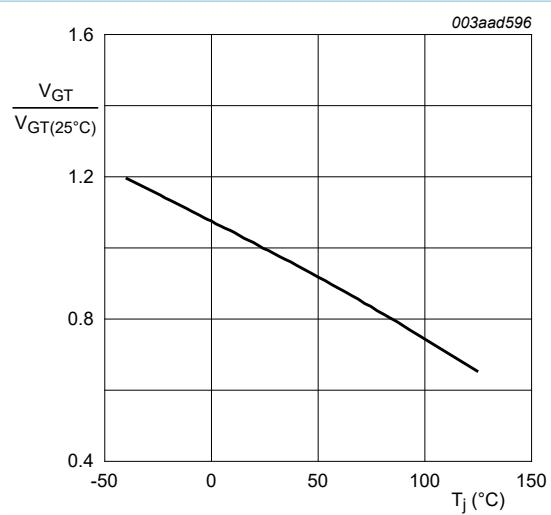


Fig. 13. Normalized gate trigger voltage as a function of junction temperature

10. Package outline

Plastic surface-mounted package with increased heatsink; 4 leads

SOT223

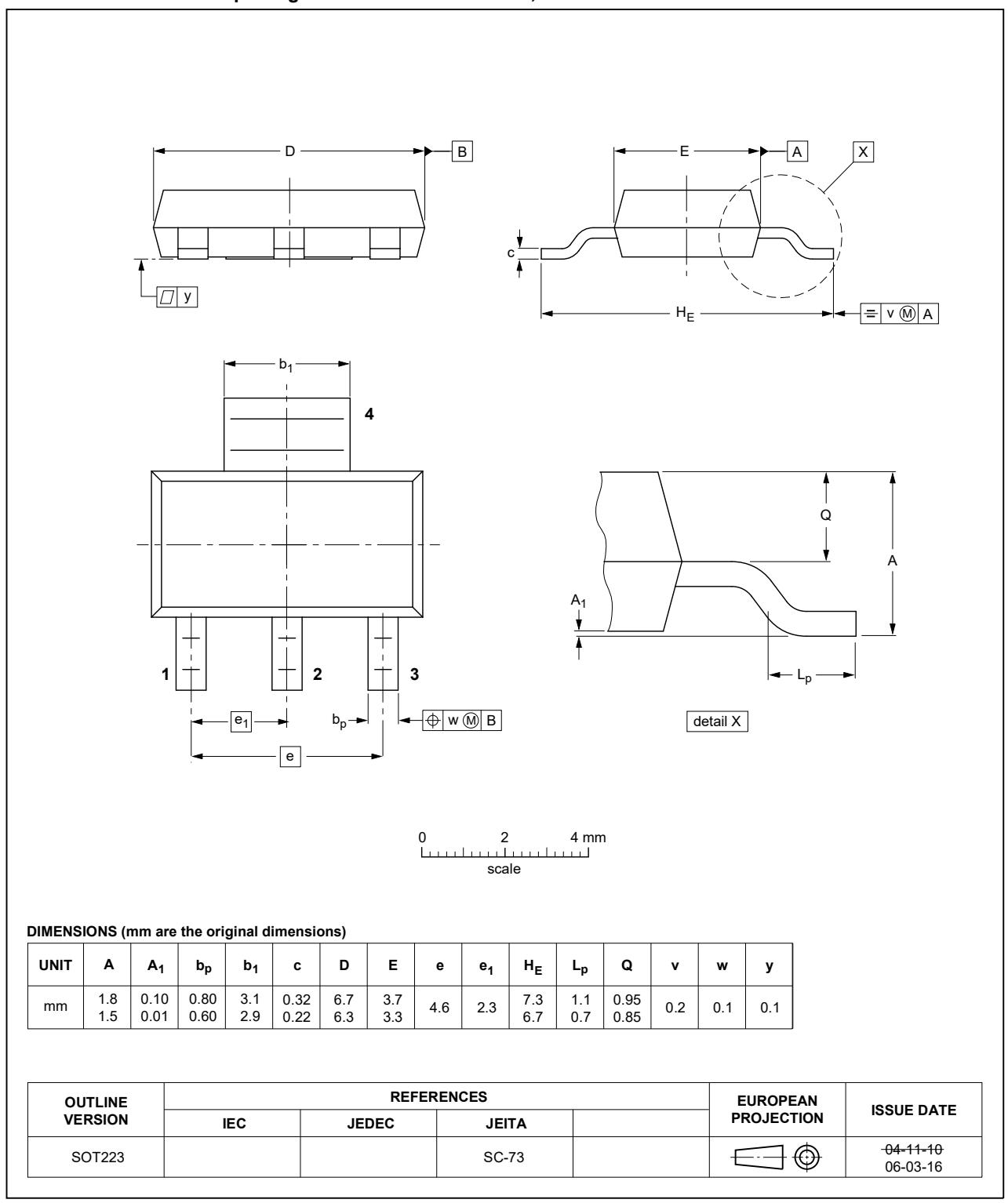


Fig. 14. Package outline SC-73 (SOT223)

11. Package outline (minimized)

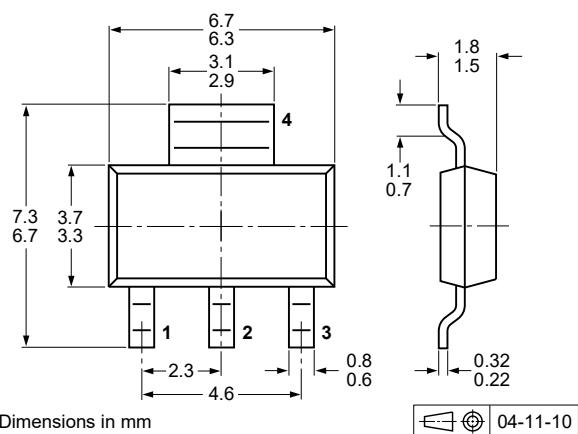


Fig. 15. Package outline SC-73 (SOT223)

12. Soldering

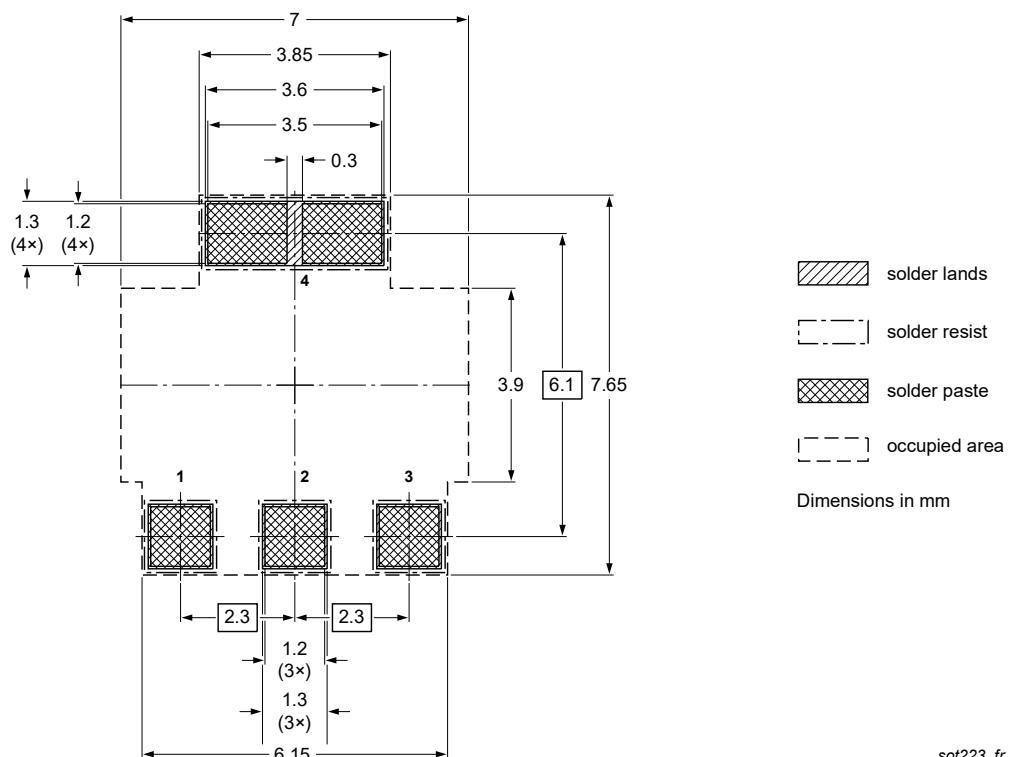


Fig. 16. Reflow soldering footprint for SC-73 (SOT223)

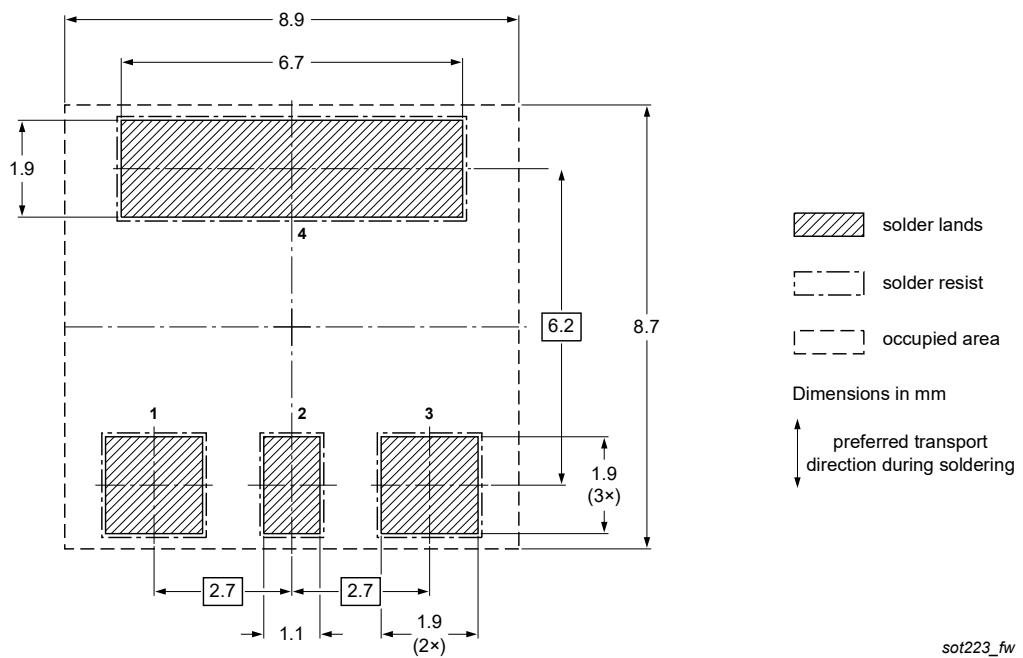


Fig. 17. Wave soldering footprint for SC-73 (SOT223)

13. Legal information

Data sheet status

| Document status [1][2] | Product status [3] | Definition |
|--------------------------------|--------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
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