



STB75NF75L

N-channel 75V - 0.009Ω - 75A - D²PAK
STripFET™ II Power MOSFET

Features

Type	V _{DSS}	R _{DS(on)}	I _D
STB75NF75L	75V	<0.011Ω	75A

- Exceptional dv/dt capability
- 100% avalanche tested
- Low threshold drive

Description

This MOSFET series realized with STMicroelectronics unique STripFET process has specifically been designed to minimize input capacitance and gate charge. It is therefore suitable as primary switch in advanced high-efficiency, high-frequency isolated DC-DC converters for Telecom and Computer applications. It is also intended for any applications with low gate drive requirements.

Applications

- Switching applications

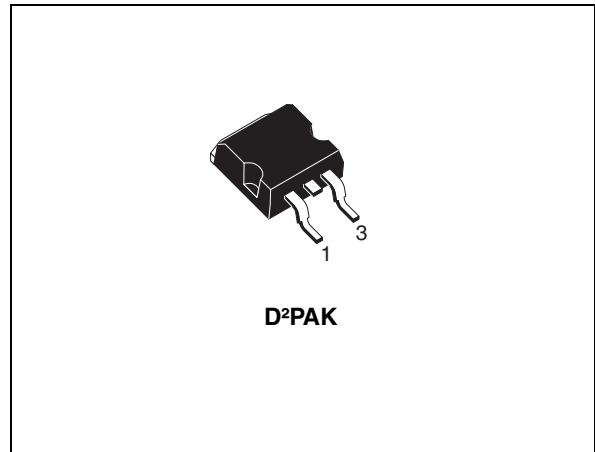


Figure 1. Internal schematic diagram

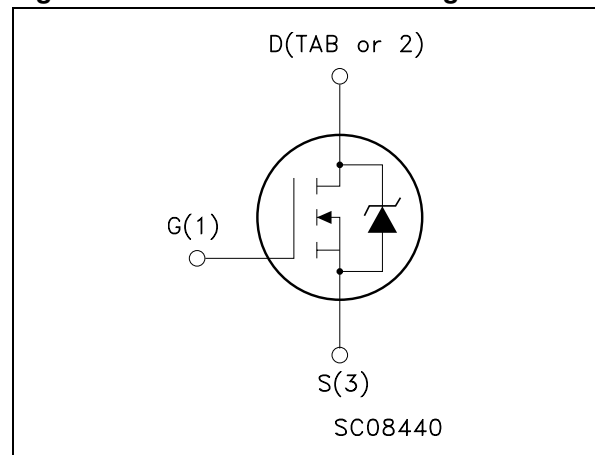


Table 1. Device summary

Order code	Marking	Package	Packaging
STB75NF75LT4	B75NF75L	D ² PAK	Tape & reel

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage ($V_{GS} = 0$)	75	V
V_{GS}	Gate-source voltage	± 15	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25^\circ\text{C}$	75	A
I_D	Drain current (continuous) at $T_C = 100^\circ\text{C}$	70	A
$I_{DM}^{(2)}$	Drain current (pulsed)	300	A
P_{TOT}	Total dissipation at $T_C = 25^\circ\text{C}$	300	W
	Derating factor	2	W/°C
$dv/dt^{(3)}$	Peak diode recovery voltage slope	10	V/ns
$E_{AS}^{(4)}$	Single pulse avalanche energy	680	mJ
T_J T_{stg}	Operating junction temperature Storage temperature	-55 to 175	°C

1. Current limited by package
2. Pulse width limited by safe operating area
3. $I_{SD} \leq 75\text{A}$, $di/dt \leq 500\text{A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq T_{JMAX}$
4. Starting $T_J = 25^\circ\text{C}$, $I_D = 37.5\text{A}$, $V_{DD} = 30\text{V}$

Table 3. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance junction-case Max	0.5	°C/W
R_{thJA}	Thermal resistance junction-ambient Max	62.5	°C/W
T_I	Maximum lead temperature for soldering purpose	300	°C

2 Electrical characteristics

($T_{CASE}=25^{\circ}\text{C}$ unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 250\mu\text{A}$, $V_{GS} = 0$	75			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = \text{Max rating}$, $V_{DS} = \text{Max rating @ } 125^{\circ}\text{C}$			1 10	μA μA
I_{GSS}	Gate body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 15\text{V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\mu\text{A}$	1		2.5	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{V}$, $I_D = 37.5\text{A}$ $V_{GS} = 5\text{V}$, $I_D = 37.5\text{A}$		0.009 0.010	0.011 0.013	Ω Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} = 15\text{V}$, $I_D = 37.5\text{A}$		120		S
C_{iss}	Input capacitance	$V_{DS} = 25\text{V}$, $f = 1\text{ MHz}$, $V_{GS} = 0$		4300		pF
C_{oss}	Output capacitance			660		pF
C_{rss}	Reverse transfer capacitance			205		pF
Q_g	Total gate charge	$V_{DD} = 60\text{V}$, $I_D = 75\text{A}$		75	90	nC
Q_{gs}	Gate-source charge	$V_{GS} = 5\text{V}$		18		nC
Q_{gd}	Gate-drain charge	see Figure 15		31		nC

1. Pulsed: pulse duration=300 μs , duty cycle 1.5%

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 40\text{V}$, $I_D = 37.5\text{A}$, $R_G = 4.7\Omega$, $V_{GS} = 4.5\text{V}$ see Figure 14		35		ns
t_r	Rise time			155		ns
$t_{d(off)}$	Turn-off delay time			110		ns
t_f	Fall time			60		ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
I_{SD}	Source-drain current				75	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				300	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 75A$, $V_{GS} = 0$			1.3	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD} = 75A$, $di/dt = 100A/\mu s$, $V_{DD} = 24V$, $T_J = 150^\circ C$ see Figure 16		120 500 9		ns nC A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

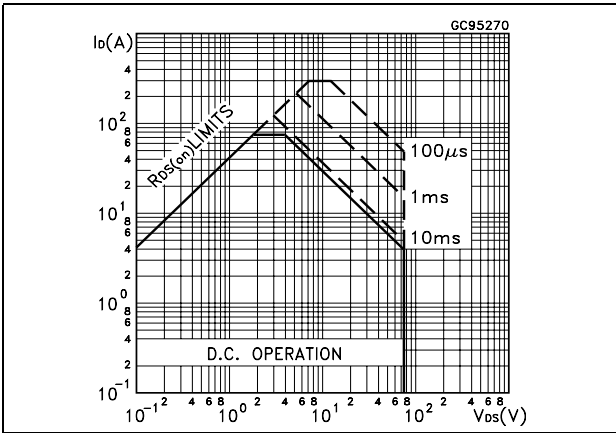


Figure 3. Thermal impedance

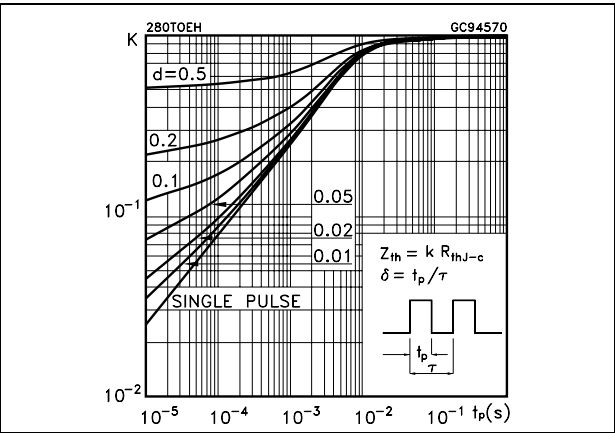


Figure 4. Output characteristics

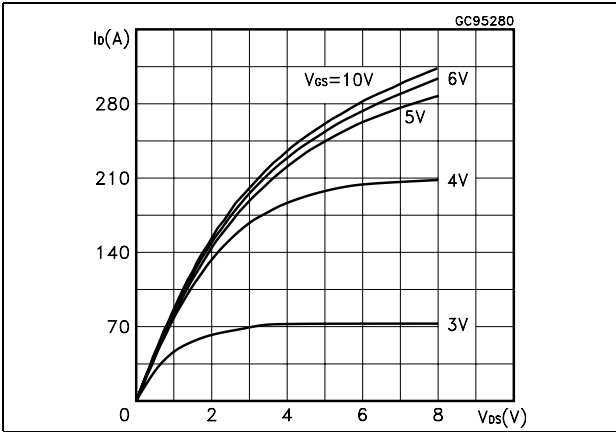


Figure 5. Transfer characteristics

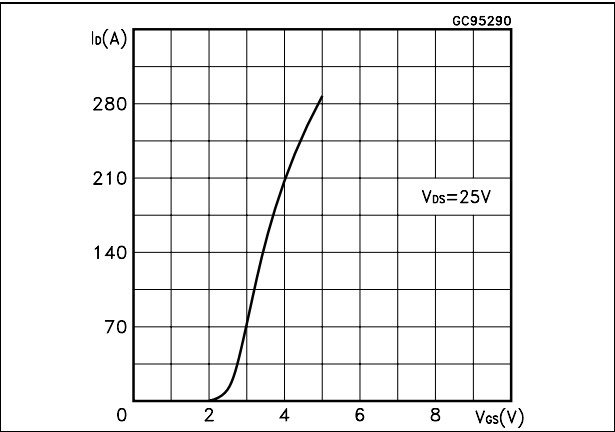


Figure 6. Transconductance

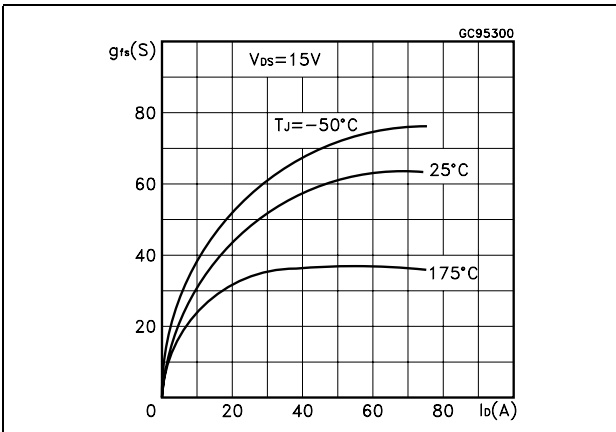


Figure 7. Static drain-source on resistance

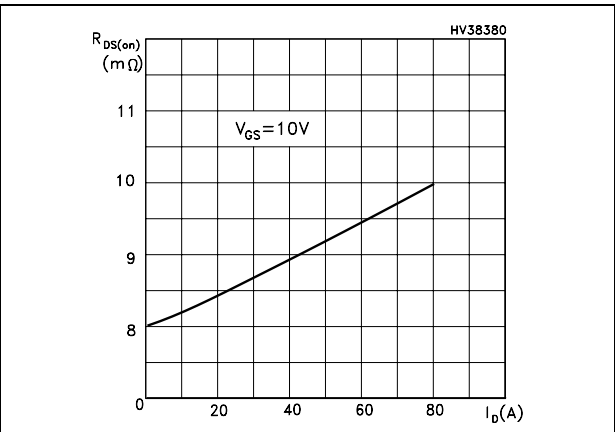


Figure 8. Gate charge vs gate-source voltage Figure 9. Capacitance variations

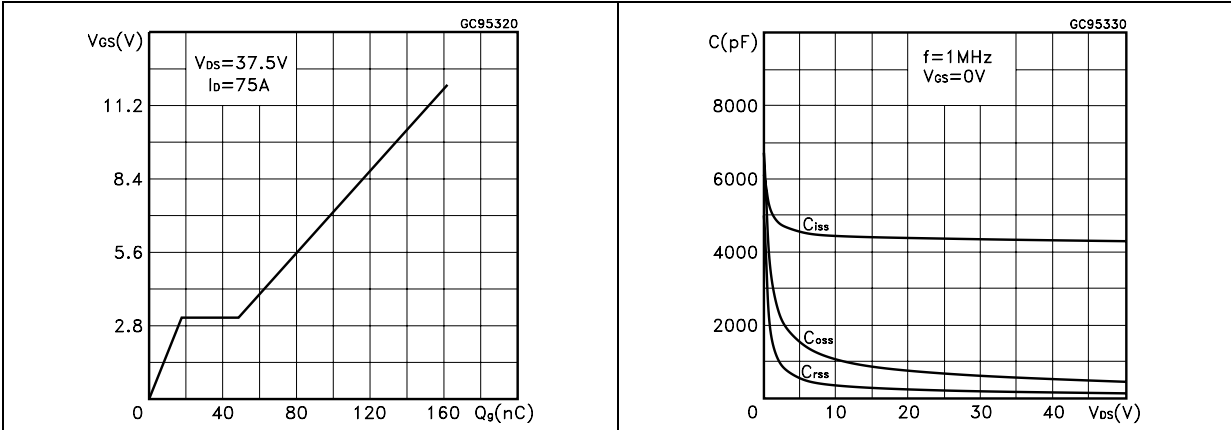


Figure 10. Normalized gate threshold voltage vs temperature Figure 11. Normalized on resistance vs temperature

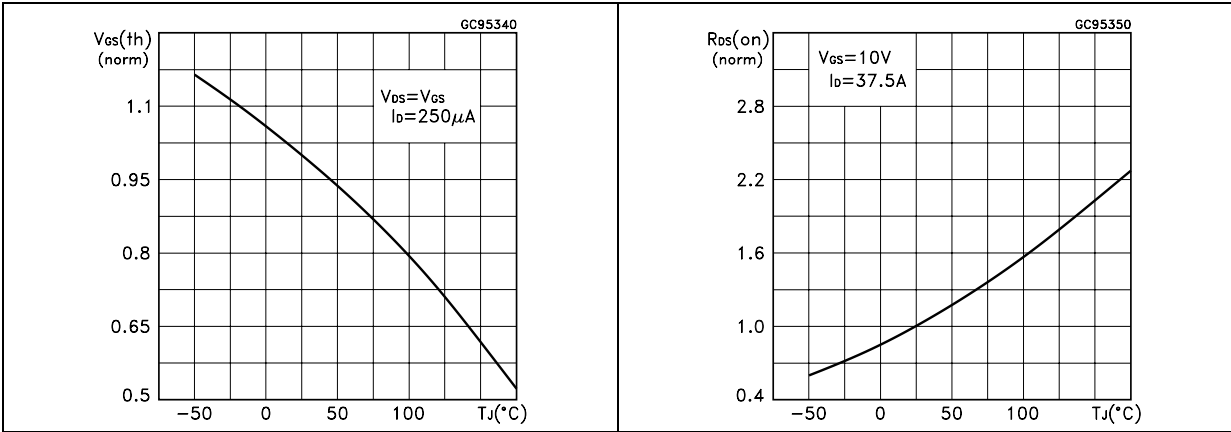
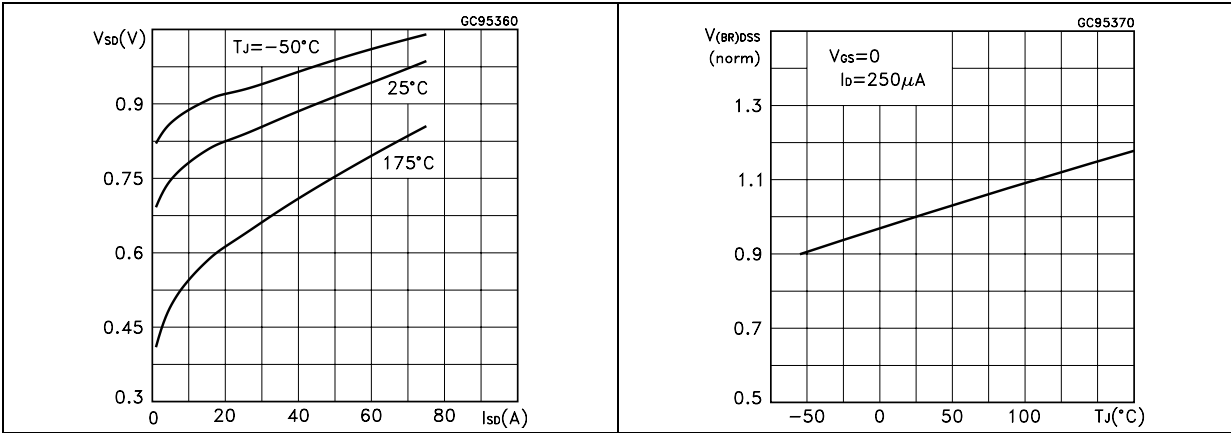


Figure 12. Source-drain diode forward characteristics Figure 13. Normalized $B_{V_{DS}}$ vs temperature



3 Test circuit

Figure 14. Switching times test circuit for resistive load

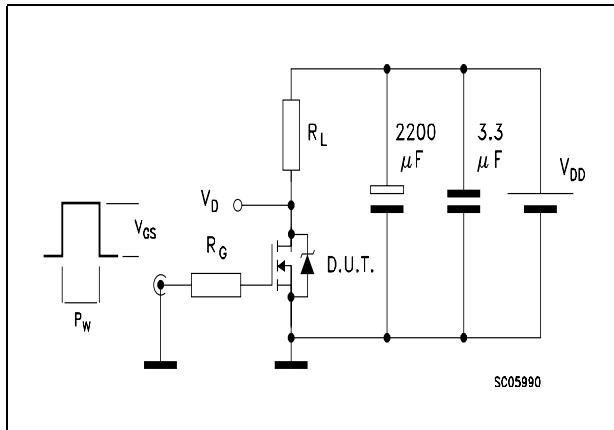


Figure 15. Gate charge test circuit

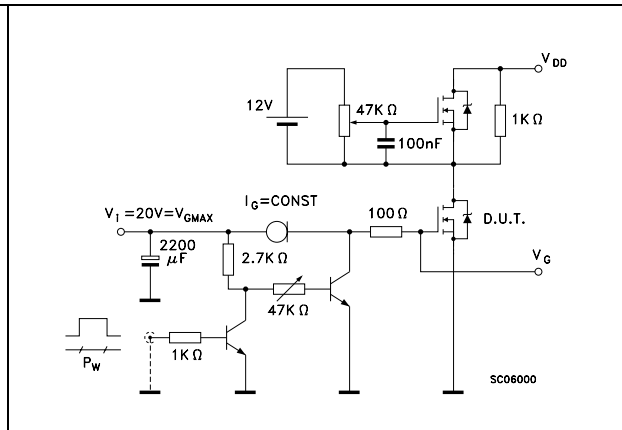


Figure 16. Test circuit for inductive load switching and diode recovery times

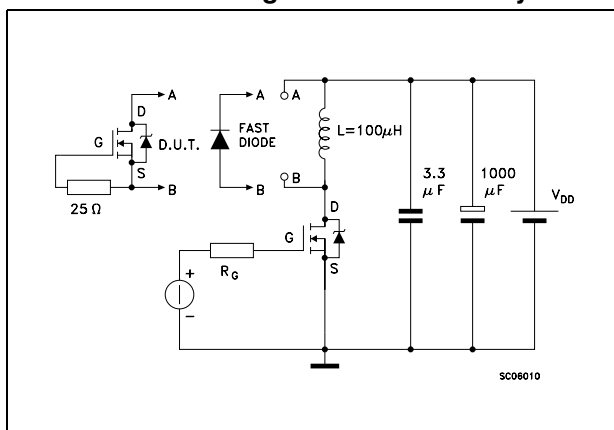


Figure 17. Unclamped Inductive load test circuit

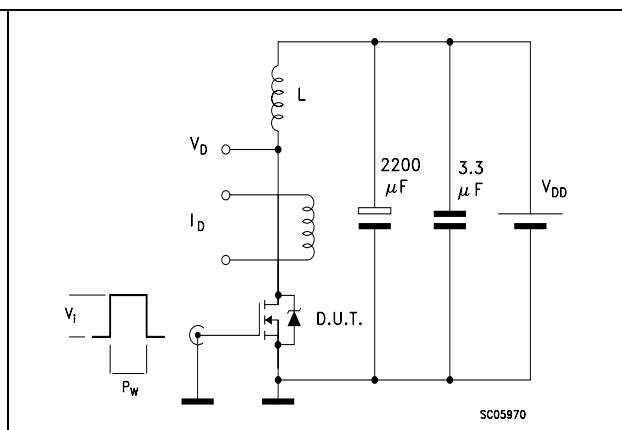
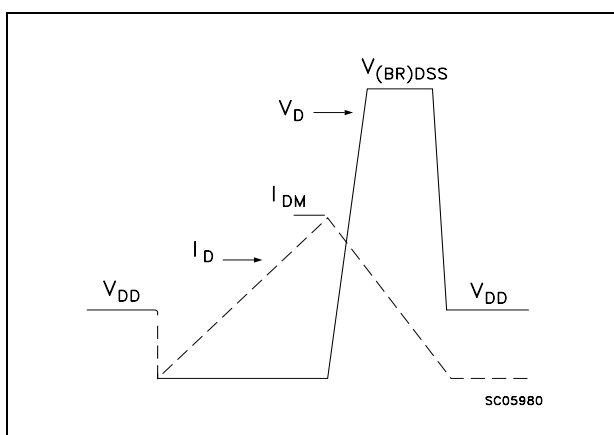


Figure 18. Unclamped inductive waveform

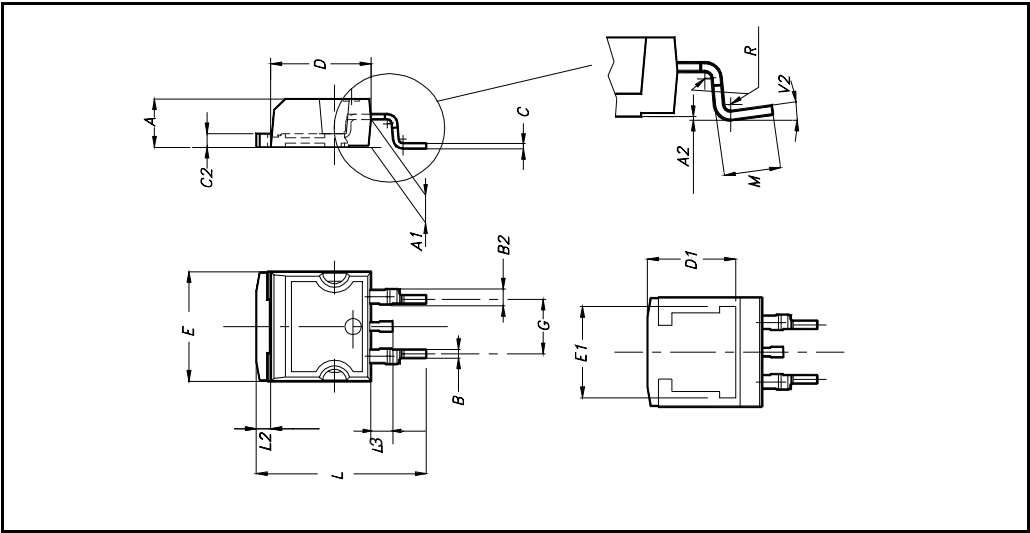


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

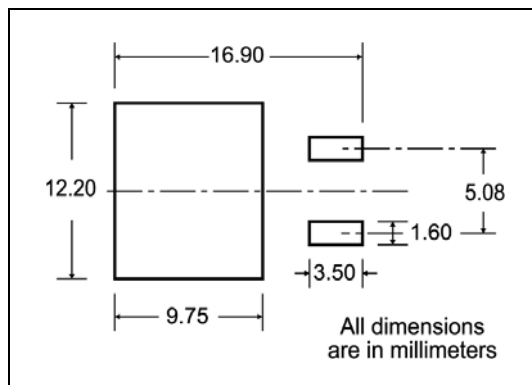
D²PAK MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
A1	2.49		2.69	0.098		0.106
A2	0.03		0.23	0.001		0.009
B	0.7		0.93	0.027		0.036
B2	1.14		1.7	0.044		0.067
C	0.45		0.6	0.017		0.023
C2	1.23		1.36	0.048		0.053
D	8.95		9.35	0.352		0.368
D1		8			0.315	
E	10		10.4	0.393		
E1		8.5			0.334	
G	4.88		5.28	0.192		0.208
L	15		15.85	0.590		0.625
L2	1.27		1.4	0.050		0.055
L3	1.4		1.75	0.055		0.068
M	2.4		3.2	0.094		0.126
R		0.4			0.015	
V2	0°		4°			

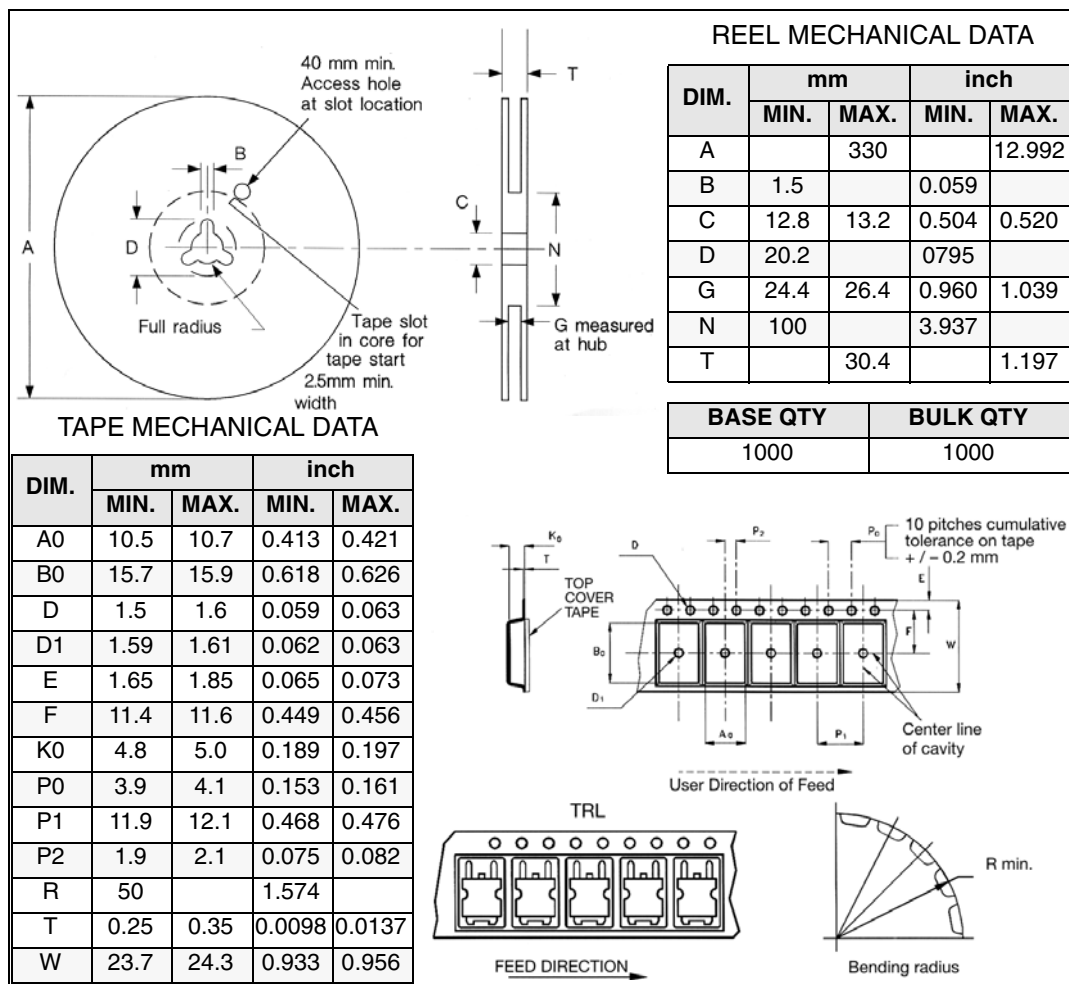


5 Packaging mechanical data

D²PAK FOOTPRINT



TAPE AND REEL SHIPMENT



* on sales type

6 Revision history

Table 8. Revision history

Date	Revision	Changes
21-Jun-2004	1	First release
02-Oct-2006	2	New template, no content change
13-Jul-2007	3	New updates on Table 7

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