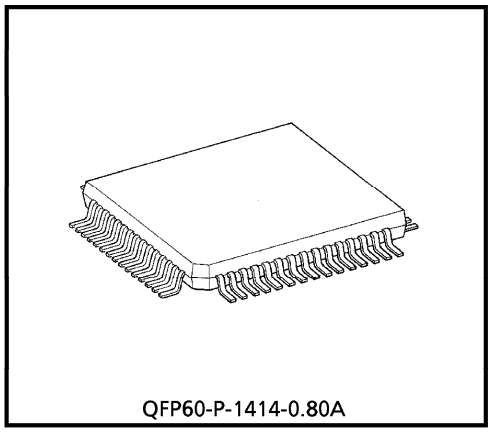
TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC9304F

SINGLE CHIP DTS MICRO CONTROLLER WITH BUILT-IN PRESCALER · PLL · LCD DRIVER (DTS-10)



QFP60-P-1414-0.80A

Weight : 0.85g (Typ.)

TC9304F is 4bit CMOS microcontroller with built-in prescaler, PLL, LCD driver for single-chip digital tuning system.

CPU has 4bit parallel addition and subtraction (AI / SI instructions), logical operation (OR and AN instructions), plural bit judge, comparission instructions (TM, SL instructions) and time base function.

The package is of 60-pin mini-flat type, and is provided with the abundant I / O ports and exclusive key-input ports controlled by the powerful input / output instructions (IO, KEY instructions) and with the abundant exclusive LCD output terminals of 1 / 2 duty and 1 / 2 bias drive.

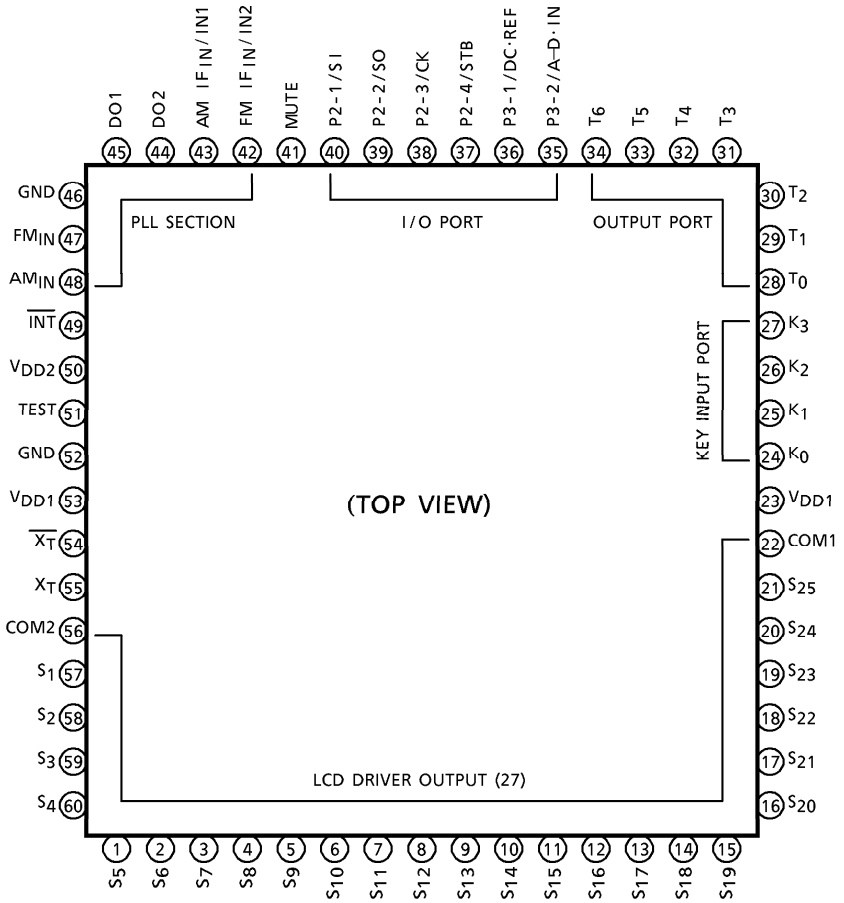
2 modulus prescaler, PLL circuit and IF counter for generating the auto-stop signal through counting IF at each band of FM or AM are incorporated. In addition, the serial bus control function (SIO instruction) for powerfully controlling the peripheral IC and the 4bit A / D converter applicable to the measurement of the electric field intensity through inputting the signal meter output are incorporated resulting in making many functions necessary for the digital tuning system provided.

FEATURES

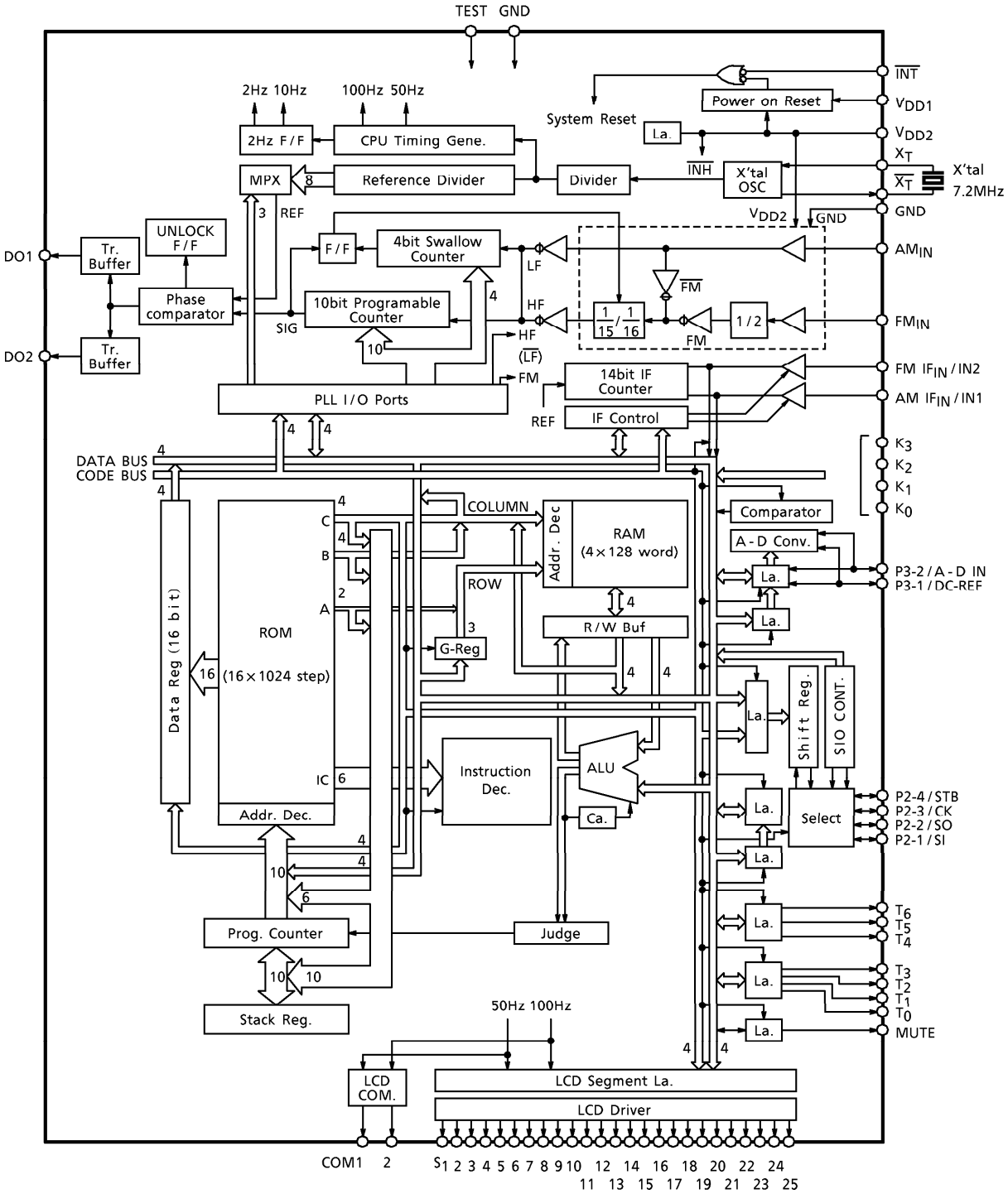
- 4bit microcontroller for single-chip digital tuning system.
- 5V ± 10% single power supply. CMOS structure with low power dissipation.
- Built-in prescaler (at FM, max. 140MHz direct input), PLL and LCD driver (1 / 2 duty, 1 / 2 bias driving frequency : 50Hz).
- Backup of data memory (RAM) and of various kinds of ports is easy (with V_{DD2} terminal).
- Program memory (ROM) : 16 bits × 1024 steps.
- Data memory (RAM) : 4 bits × 128 words.
- 62 kinds of powerful instruction sets (All are single-word instructions).

- Instruction execution time 44.4μs (7.2MHz crystal connection).
- Abundant instructions of addition and subtraction (12 kinds of addition instructions, 12 kinds of subtraction instructions).
- Power compound decision instructions (TMTR, TMFR, TMT and TMF instructions).
- Data transfer in the same low address is possible.
- Indirect data transfer between registers is possible. (MVRD, MVRS, MVGD and MVGS instructions).
- Powerful 16 general registers (Located in RAM).
- Stack level : 1 level.
- No concept of page or field is in program memory (ROM), and JUMP and CAL instructions can freely be executed in 1024 steps.
- Built-in IF counter in each band of FM and AM (FM IF_{IN}, AM IF_{IN}).
- Independent frequency input terminal at FM and AM (FM_{IN}, AM_{IN}), and two phase-comparator outputs (DO1, DO2).
- 8 kinds of reference frequency can be selected with program.
- Pulse swallow method and direct dividing method are selectable according to receiving band.
- IF correction at FM band is possible.
- Powerful serial bus control function is built-in (I/O port-2 terminal is changed over for use).
- Powerful input/output instructions (IO, KEY and SIO instructions).
- Exclusive use input ports for key input (K_0~K_3), and exclusive use terminals of LCD driver abundant as 25.
- IF counters (AM IF_{IN}, FM IF_{IN}) and input ports (IN1, IN2) can be selected with program for use.
- Abundant I/O ports as 14 (ports capable of input/output setting by the unit of 1bit : 6, exclusive use ports for output : 8).
- Clock stop is possible with instruction (at CKSTP instruction : power supply current 1μA max.).
- 2Hz timer F/F and 10Hz interval pulse output are incorporated. (internal port for time base).
- Locked condition of PLL can be detected.
- At MW_{9K} (REF = 9kHz), IF of IF counter can be selected among 450kHz, 459kHz and 468kHz.
- Built-in 4bit A/D converter (I/O port-3 terminal (P3-1, P3-2) are changed over with program for use).

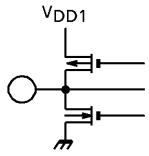
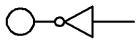
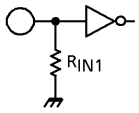
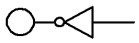
PIN CONNECTION

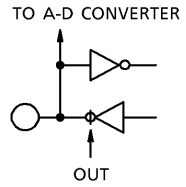
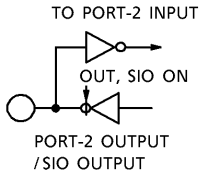
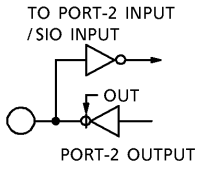
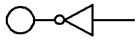
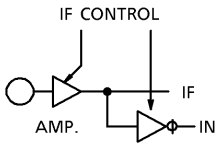


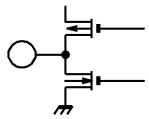
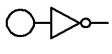
BLOCK DIAGRAM

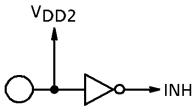
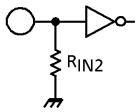


PIN FUNCTION

PIN No.	SYMBOL	PIN NAME	FUNCTION AND OPERATION	REMARKS
22 56	COM1 COM2	LCD Common Output	Common signal output terminal for LCD. Indication of max. 50 segments is possible with the matrix of S_1~S_{25}. Levels of three values of V_{DD1}, 1/2V_{DD1} and GND are output at this terminal with 5ms interval and 50Hz cycle. (Note) Output is automatically fixed at "L" level at system reset, CKSTP instruction execution and DISP OFF execution.	
57~60 1~21	S_1~S_4 S_5~S_{25}	LCD Segment Output	Segment signal output terminal for LCD. Indication of max. 50 segments is possible with the matrix of COM1 and COM2. The data for these terminals are output through the execution of SEG instruction (COM1 system) and MARK instruction (COM2 system). By means of preparing decode pattern in ROM area and using DAL instruction, segment decoding can be carried out. (Note) Output is automatically set at "L" level at the time of system reset and execution of CKSTP instruction and DISP OFF.	
24~27	K_0~K_3	Key Input Port	4bit input port for key matrix input. When key instruction specifying this port at operand part is executed, data of these terminals are read in RAM. All these terminals have built-in pulldown resistances. Usually output ports of T_0~T_6 are used.	
28~34	T_0~T_6	Key Timing Output Port	Output ports of 4 bits (T_0~T_3) and 3 bits (T_4~T_6). These are usually used as key return timing output signals of key matrix.	

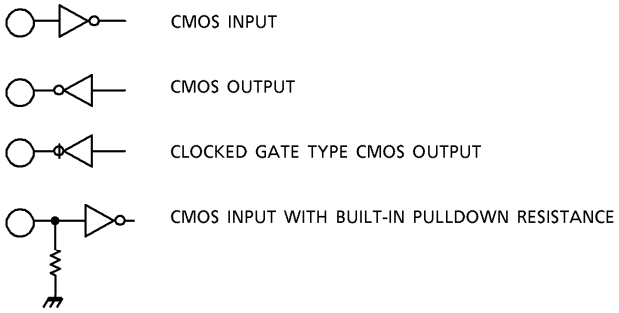
PIN No.	SYMBOL	PIN NAME	FUNCTION AND OPERATION	REMARKS
35 36	P3-2 /A-D·IN P3-1 /DC·REF	I/O Port-3 A-D /Analog Voltage Input /Reference Voltage Input	2bit I/O port. This port can specify input/output of every 1 bit. This specification is performed by the contents of internal port called PORT-2 I/O CONTROL. These terminals are used also for analog input of built-in 4bit A-D converter. Switching control to A-D converter input is also carried out by the contents of PORT-3 I/O CONTROL port. Built-in A-D converter is of successive comparison method by the program. P3-1 becomes reference voltage input and P3-2 becomes analog comparison voltage input.	
37~40	P2-4/STB P2-3/CK P2-2/SO P2-1/SI	I/O Port-2 /Strobe Pulse Output /Serial Clock Output /Serial Data Output /Serial Data Input	4bit I/O port. This port can specify input/output of every 1 bit. This specification is performed by the contents of internal port called PORT-2 I/O CONTROL. This terminal is also used as serial interface (SIO). Switching control of SIO is carried out by the contents of SIO ON bit. Peripheral option IC can Powerfully be controlled by means of using this serial. Interface and executing SIO instruction. Two kinds of modes $\overline{NCD}$/NCD can be selected by the program for serial transfer method.	 
41	MUTE	Muting Signal Output Port	1bit output port. This is usually used as muting control signal output.	
42 43	FM IF_{IN} /IN2 AM IF_{IN} /IN1	FM IF Signal Input/Input Port-2 AM IF Signal Input/Input Port-1	IF signal input terminal of IF counter for detecting autostop independently of each band of FM or AM. These terminals have built-in amplifiers and operate with C-connection and small amplitude. These terminals can be used as input parts by the program and this selection is made by the contents of IN CONTROL port.	

PIN No.	SYMBOL	PIN NAME	FUNCTION AND OPERATION	REMARKS
44 45	DO2 DO1	Phase Comparator Output	Phase comparator output terminal of PLL. DO1 and DO2 are parallel output. Therefore, optimum filter constant can be set for each band of FM / AM.	V_{DD1} 
46	GND	Prescaler Section Grounding Terminal	Exclusive use grounding terminal for built-in prescaler.	—
47	FM_{IN}	FM Local Signal Input	Prescaler input terminal at FM band. Local oscillation output (VCO output) of 50~140MHz is input. This terminal has built-in amplifier and operates with C-connection and small amplitude.	—
48	AM_{IN}	AM Local Signal Input	Programmable counter input terminal at AM band. Direct-dividing method (LF mode) and pulse-swallow method (HF mode) can freely be changed over. In direct-dividing method, local oscillation output (VCO output) of 0.5~10MHz is input, and in pulse-swallow method, local oscillation output of 5~60MHz is input. This terminal has built-in amplifier and operates with C-connection and small amplifier.	—
49	$\overline{INT}$	Initializing Input	System reset signal input terminal of device. During $\overline{INT}$ is at "L" level, reset is applied, and when "H" level is reached, program starts from address 0. When voltage of 0V→4.5V is impressed at V_{DD1}, since system reset is usually applied (power-on reset), this terminal is fixed at "H" level to be used. (Note) After system reset, I / O port is set to input mode. Since output condition of output port is unstable, initialization with program is required according to necessity.	

PIN No.	SYMBOL	PIN NAME	FUNCTION AND OPERATION	REMARKS
50	V_{DD2}	Prescaler Section Power Impressing Terminal ($\overline{INH}$ input terminal)	Power impressing terminal of prescaler part. Usually voltage of 5V ± 10% is impressed. Impress voltage of $V_{DD2} \leqq V_{DD1}$. This terminal is commonly used as input terminal of $\overline{INH}$ port and is also signal input terminal for selecting radio mode. Radio-on mode or radio-off mode is judged to have been made respectively at "H" level or "L" level. When CKSTP instruction is used in program and when this CKSTP instruction is executed during V_{DD2} terminal is at "L" level, memory backup state can be made with low consumption current (1μA or under) by means of stopping internal clock generator and CPU operation. At this time, all the output terminals (indication output, output port, etc) become "L" level. (Note) CKSTP instruction is valid when V_{DD2} terminal is at "L" level, and performs the same operation as that of NOOP instruction when executed at "H" level.	
51	TEST	Test Mode Control Input	Input terminal for controlling test mode. At "H" level, test mode is made, and at "L" level or NC state, normal operation is carried out. (Pulldown resistance is incorporated.) In test mode, device operates as evaluator chip, and program evaluation is made possible on EPROM base through combination with external simulation board.	
54 55	$\overline{X_T}$ X_T	Crystal Oscillating Terminal	Connecting terminal of crystal oscillator. Crystal of 7.2MHz is connected. At execution of CKSTP instruction, oscillation is automatically stopped.	—
52	GND	Grounding Terminal	Grounding terminal of CPU and PLL parts.	—

PIN No.	SYMBOL	PIN NAME	FUNCTION AND OPERATION	REMARKS
23 53	V_{DD1}	Power Impressing Terminal	Power impressing terminals of CPU and PLL parts. At PLL operation, voltage of 5V ± 10% is impressed. In backup state (at execution of CKSTP instruction), voltage can be reduced down to 2V. When voltage of 0V→4.5V is impressed at this terminal, system reset is applied to device and program starts from address 0. (power-on reset) (Note) Carry out power-on reset from the state of V_{DD2} = "L" level. (Note) At turning power supply ON, since contents of each port (output port, internal port, etc) are indefinite, initialization is required according to necessity.	—

(Supplementation)



MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Power Supply Voltage	V_{DD}	− 0.3~6.0	V
Input Voltage	V_{IN}	− 0.3~V_{DD} + 0.3	V
Power Dissipation	P_D	400	mW
Operating Temperature	T_{opr}	− 40~85	°C
Storage Temperature	T_{stg}	− 65~150	°C

ELECTRICAL CHARACTERISTICS (Unless otherwise specified, Ta = 25°C, $V_{DD1} = V_{DD2} = 5V$)

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
V_{DD1} [Power impressing terminal of CPU part]								
Operational Power Supply Range		V_{DD1}	—	At CPU, PLL operation *	4.5	5.0	5.5	V
Memory Holding Voltage Range		I_{HD}	—	Crystal oscillation stops	2.0	~	5.5	V
Operating Power Supply Current		I_{DD1}	—	At CPU, PLL operation	—	1.0	3.0	mA
Memory Holding Power Supply Current		I_{HD1}	—	V_{DD1} = 5V, Crystal oscillation stop	—	0.07	1.0	μA
		I_{HD2}	—	V_{DD1} = 2V Crystal oscillation stop	—	—	0.5	
Crystal Oscillation Frequency		f_{XT}	—	*	—	7.2	—	MHz
V_{DD2} [Power impressing terminal of PLL part]								
PLL Operating Power Supply Voltage		V_{DD2}	—	Providing $V_{DD2} \leqq V_{DD1}$ *	4.5	5.0	5.5	V
PLL Operating Power Supply Current		I_{DD2}	—	At inputting FM_{IN} = 120MHz	—	15	25	mA
$\overline{INH}$ Input Voltage	"H" Level	V_{IH2}	—	—	4.3	~	5.0	V
	"L" Level	V_{IL2}	—	—	0	~	2.7	
PLL operating frequency range								
FM_{IN}		f_{FM1}	—	$V_{IN} = 0.5V_{p-p}$ *	50	~	140	MHz
AM_{IN} (HF mode)		f_{HF}	—	$V_{IN} = 0.3V_{p-p}$ *	5	~	60	MHz
AM_{IN} (LF mode)		f_{LF}	—	$V_{IN} = 0.3V_{p-p}$ *	0.5	~	10	MHz
FM IF_{IN}		f_{IF} (FM)	—	$V_{IN} = 0.3V_{p-p}$ *	10	~	12	MHz
AM IF_{IN}		f_{IF} (AM)	—	$V_{IN} = 0.3V_{p-p}$ *	400	~	500	kHz

(Note) Items marked with * are guaranteed within the range of $V_{DD1} = V_{DD2} = 4.5$~5.5V, Ta = − 40~85°C.

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
PLL operating input amplitude							
FM_{IN}	V_{IN1} (FM)	—	f_{IN} = 50~140MHz *	0.5	~	V_{DD} – 0.5	V_{p-p}
AM_{IN} (HF Mode)	V_{IN} (HF)	—	f_{IN} = 5~60MHz *	0.3	~	V_{DD} – 0.5	V_{p-p}
AM_{IN} (LF Mode)	V_{IN} (LF)	—	f_{IN} = 0.5~10MHz *	0.3	~	V_{DD} – 0.5	V_{p-p}
FM IF_{IN}	V_{IN} (FM IF)	—	f_{IN} = 10~12MHz, Typ. 10.7MHz *	0.3	~	V_{DD} – 0.5	V_{p-p}
AM IF_{IN}	V_{IN} (AM IF)	—	f_{IN} = 400~500kHz, Typ. 450kHz *	0.3	~	V_{DD} – 0.5	V_{p-p}
LCD common output (COM1, COM2)							
Output Current "H" Level	I_{OH1}	—	V_{OH} = 4.5V	– 350	– 900	—	μA
Output Current "L" Level	I_{OL1}	—	V_{OL} = 0.5V	350	900	—	μA
1/2 Bias Voltage	V_{BS}	—	—	2.40	2.50	2.60	V
LCD segment output (S_1~S_{25})							
Output Current "H" Level	I_{OH2}	—	V_{OH} = 4.5V	– 150	– 450	—	μA
Output Current "L" Level	I_{OL2}	—	V_{OL} = 0.5V	150	450	—	μA
MUTE, T_0~T_6 ports							
Output Current "H" Level	I_{OH3}	—	V_{OH} = 4.5V	– 0.9	– 2.5	—	mA
Output Current "L" Level	I_{OL3}	—	V_{OL} = 0.5V	0.7	2.0	—	mA
P2-1~P2-4 (SO, CK, STB), P3-1~P3-2 ports							
Output Current "H" Level	I_{OH4}	—	V_{OH} = 4.0V	– 1.0	– 3.0	—	mA
Output Current "L" Level	I_{OL4}	—	V_{OL} = 1.0V	1.0	3.0	—	mA
Key Input Port (K_0~K_3)							
Input Voltage "H" Level	V_{IH1}	—	—	3.5	—	5.0	V
Input Voltage "L" Level	V_{IL1}	—	—	0	—	1.5	V
Pulldown Resistance	R_{IN1}	—	—	50	100	150	kΩ

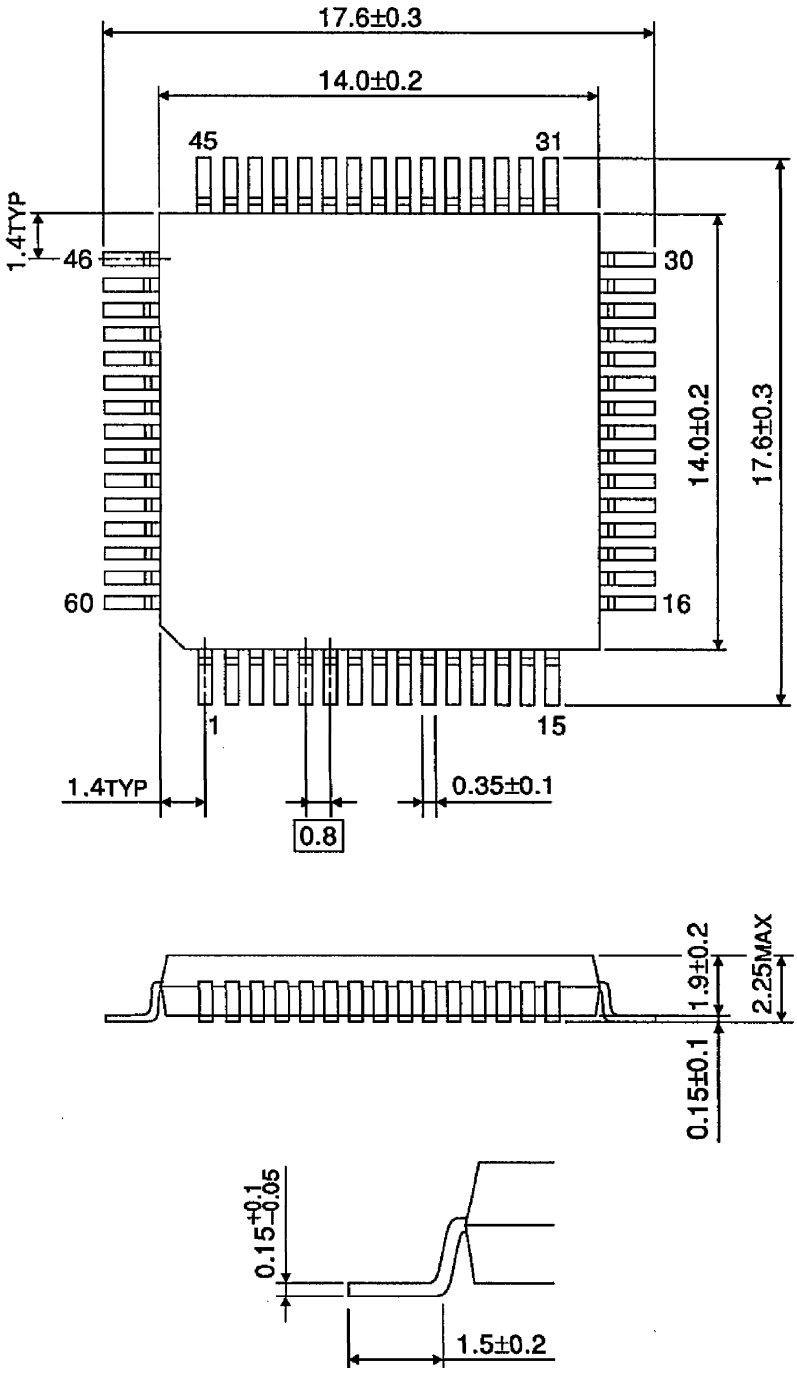
(Note) Items marked with * are guaranteed within the range of $V_{DD1} = V_{DD2}$ = 4.5~5.5V, Ta = – 40~85°C.

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
$\overline{INT}$, P2-1~P2-4 (SI), P3-1~P3-2 ports, IN1~IN2								
Input Voltage	"H" Level	V_{IH1}	—	—	3.5	~	5.0	V
	"L" Level	V_{IL1}	—	—	0	~	1.5	
Input Leak Current	"H" Level	I_{IH1}	—	V_{IH} = 5.0V	—	—	1.0	μA
	"L" Level	I_{IL1}	—	V_{IL} = 0V	—	—	− 1.0	
DO output								
Output Current	"H" Level	I_{OH5}	—	V_{OH} = 4.0V	− 1.0	− 3.0	—	mA
	"L" Level	I_{OL5}	—	V_{OL} = 1.0V	1.0	3.0	—	
Tri-state Leak Current		I_{TL}	—	V_{TLH} = 5.0V, V_{TLL} = 0V		—	±0.1	μA
A-D converter (DC·REF, A-D·IN)								
DC·REF Built-in Ladder Resistance		$\overline{R_L}$	—	—	25	40	60	kΩ
DC·REF Input Voltage Range		V_{REF}	—	—	1.0	~	3.0	V
Resolution		V_{RES}	—	—	—	V_{REF} / 16	—	V
IF_{IN}, X_T Input Feedback Resistance		R_f	—	—	500	1000	1500	kΩ
TEST Input Pulldown Resistance		R_{IN2}	—	—	15	30	60	kΩ

(Note) Items marked with * are guaranteed within the range of $V_{DD1} = V_{DD2} = 4.5 \sim 5.5V$, Ta = − 40~85°C.

PACKAGE DIMENSIONS

QFP60-P-1414-0.80A Unit : mm



Weight : 0.85g (Typ.)

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