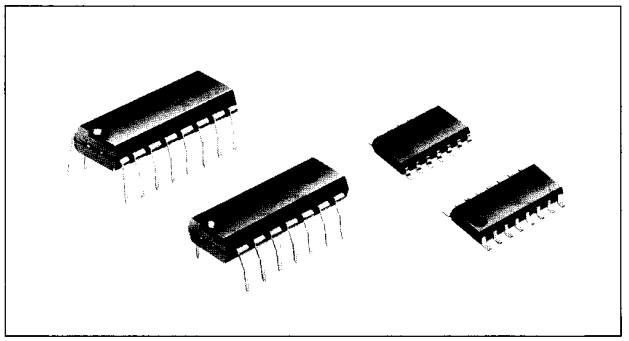
BU4000B Series



The BU4000B is a series of CMOS ICs characterized by low voltage and low power consumption. In addition to a wide supply range, the BU4000B is compatible with the general-purpose 4000B series. Another feature of the series is that it can drive LS-TTL ICs directly. The BU4000B is available in standard DIP and mini-flat (MF) packages.

Features

1. Low power consumption.
2. Wide supply voltage range.
3. High input impedance.
4. High fan-out.
5. Capable of directly driving LS-TTL1 and LS-TTL2.

BU4000B Series Product Summary

☆Under development

Category	Type	Function	Block diagram	Package	
				Configuration	No. of pins
Analog switches/multiplexers	BU4016B	Quad bilateral switch	Fig. 16	DIP/MF	14
	BU4066B	Quad bilateral switch	Fig. 17	DIP/MF	14
	BU4051B	8-channel analog multiplexer/demultiplexer	Fig. 18	DIP/MF	16
	BU4052B	Dual 4-channel analog multiplexer/demultiplexer	Fig. 19	DIP/MF	16
	BU4053B	Triple 2-channel analog multiplexer/demultiplexer	Fig. 20	DIP/MF	16
	BU4551B	Quad 2-channel analog multiplexer/demultiplexer	Fig. 21	DIP/MF	16
Gates	BU4001B	Quad 2-input NOR gate	Fig. 22	DIP/MF	14
	BU4011B	Quad 2-input NAND gate	Fig. 23	DIP/MF	14
	BU4030B	Quad exclusive-OR gate	Fig. 24	DIP/MF	14
	BU4070B	Quad exclusive-OR gate	Fig. 25	DIP/MF	14
	BU4081B	Quad 2-input AND gate	Fig. 26	DIP/MF	14
	BU4093B	Quad 2-input NAND Schmitt trigger	Fig. 27	DIP/MF	14
	☆BU4049UB	Hex inverting buffer/converter	Fig. 28	DIP/MF	16
	BU4069UB	Hex inverter	Fig. 29	DIP/MF	14
	☆BU4503B	Hex tristate buffer	Fig. 30	DIP/MF	16
	BU4584B	Hex Schmitt trigger	Fig. 31	DIP/MF	14
Flip-flops	BU4013B	Dual D-type flip-flop	Fig. 32	DIP/MF	14
	☆BU4027B	Dual J-K master-slave flip-flop	Fig. 33	DIP/MF	16
Shift registers/counters	BU4015B	Dual 4-bit static shift register	Fig. 34	DIP/MF	16
	☆BU4021B	8-stage static shift register	Fig. 35	DIP/MF	16
	☆BU4516B	Binary up/down counter	Fig. 36	DIP/MF	16
Monostable multivibrator	BU4538B	Dual precision monostable multivibrator	Fig. 37	DIP/MF	16
Decoder	BU4028B	BCD to decimal decoder	Fig. 38	DIP/MF	16
Latch	BU4042B	Quad D-latch	Fig. 39	DIP/MF	16
Others	☆BU4007UB	Dual complementary pair plus inverter	Fig. 40	DIP/MF	14

Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Limits	Unit
Supply voltage	V_{DD}	−0.3~16	V
Input voltage	V_{IN}	−0.3~V_{DD}+0.3	V
Power dissipation	Pd	550(for both DIP and MF)	mW
Storage temperature	Tstg	−55~150	°C

Recommended Operating Conditions

Parameter	Symbol	Limits	Unit	Conditions
Supply voltage	V_{DD}	3~16	V	—
Input voltage	V_{IN}	0~V_{DD}	V	—
Operating temperature	Topr	−40~85*	°C	—

*For an extended operating temperature range, consult your local ROHM representative.

Electrical Characteristics/DC Characteristics (Ta=25°C, V_{SS}=0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions V_{DD}(V)	Conditions V_{IN}(V)	Conditions
Input high voltage (Type B)	V_{IH}	3.5	2.75	—	V	5	—	—
		7.0	5.50	—		10		
		11.0	8.25	—		15		
Input high voltage (Type UB)		4.0	2.75	—		5	—	—
		8.0	5.50	—		10		
		12.5	8.25	—		15		
Input low voltage (Type B)	V_{IL}	—	2.25	1.5	V	5	—	—
		—	4.50	3.0		10		
		—	6.75	4.0		15		
Input low voltage (Type UB)		—	2.25	1.0		5	—	—
		—	4.50	2.0		10		
		—	6.75	2.5		15		
Output high voltage	V_{OH}	4.95	5.00	—	V	5	0, V_{DD}	I_O=0mA
		9.95	10.00	—		10		
		14.95	15.00	—		15		
Output low voltage	V_{OL}	—	0.00	0.05	V	5	0, V_{DD}	I_O=0mA
		—	0.00	0.05		10		
		—	0.00	0.05		15		
Output high current	I_{OH}	−0.16	—	—	mA	5	0, V_{DD}	V_{OH}=4.6V
		−0.4	—	—		10		V_{OH}=9.5V
		−1.2	—	—		15		V_{OH}=13.5V
Output low current	I_{OL}	0.44	—	—	mA	5	0, V_{DD}	V_{OL}=0.4V
		1.1	—	—		10		V_{OL}=0.5V
		3.0	—	—		15		V_{OL}=1.5V
Input current	I_{IN}	—	—	±0.3	μA	5	0, V_{DD}	—
Power consumption (Gates)	I_{DD}	—	—	1.0	μA	5	0, V_{DD}	—
		—	—	2.0		10		
		—	—	4.0		15		
Power consumption (Flip-fops, buffers)		—	—	4.0		5		
		—	—	8.0		10		
		—	—	16.0		15		
Power consumption (MSI)		—	—	20		5		
		—	—	40		10		
		—	—	80		15		

Electrical Characteristics/Switching Characteristics (Ta=25°C, V_{SS}=0V)

Prameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	
						V_{DD}	
Output rise time	Tr	—	180	400	ns	5	C_L=50pF
		—	90	200		10	
		—	65	160		15	
Output fall time	Tf	—	100	200	ns	5	C_L=50pF
		—	50	100		10	
		—	40	80		15	
Maximum clock frequency	fφmax.	—	2.0	—	MHz	5	C_L=50pF
		—	6.0	—		10	
		—	7.5	—		15	

Dimensions (Unit: mm)

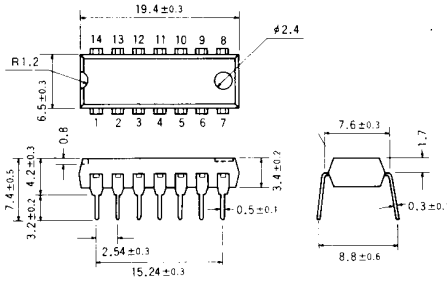


Fig. 1 14-pin DIP

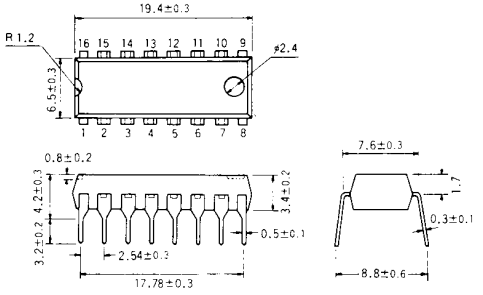


Fig. 2 16-pin DIP

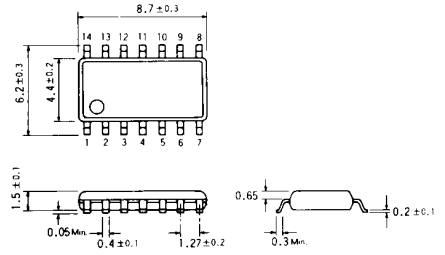


Fig. 3 14-pin MF

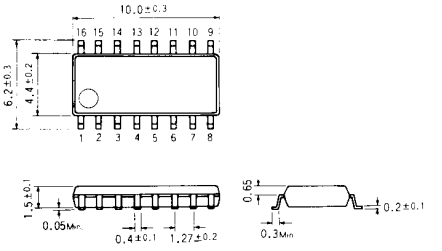


Fig. 4 16-pin MF

Electrical Characteristic Curves

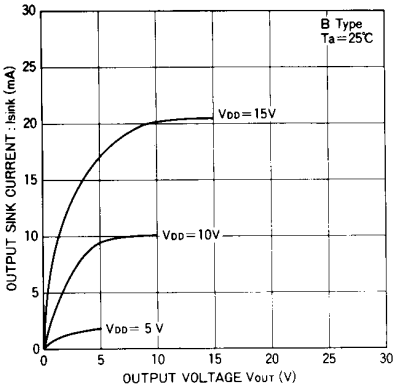


Fig. 5 Output sink current vs. output voltage

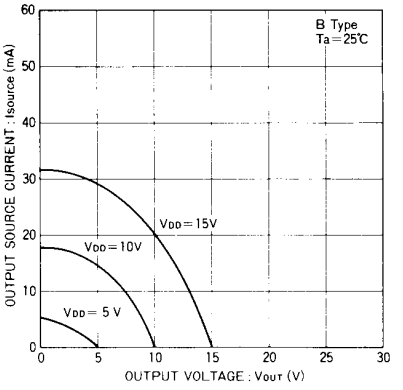


Fig. 6 Output source current vs. output voltage

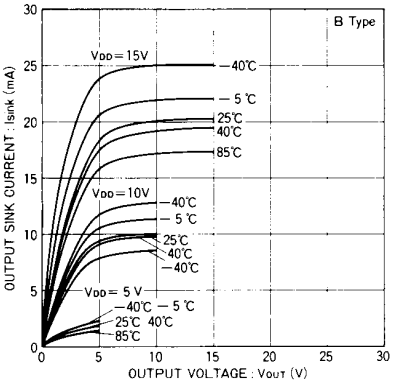


Fig. 7 Output sink current vs. output voltage

Electrical Characteristic Curves

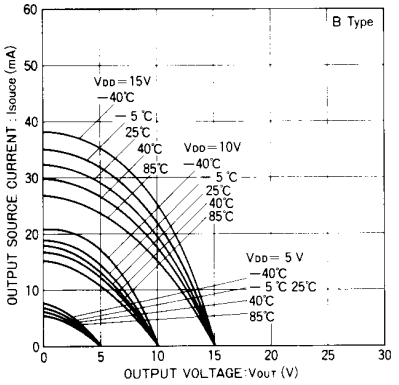


Fig. 8 Output source current vs. output voltage

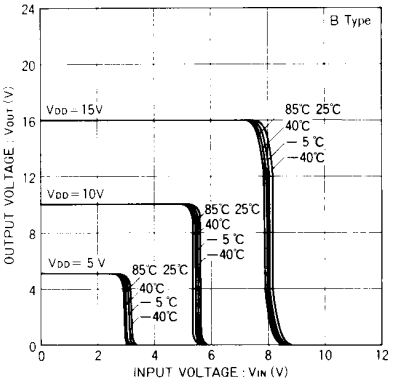


Fig. 9 Output voltage vs. input voltage

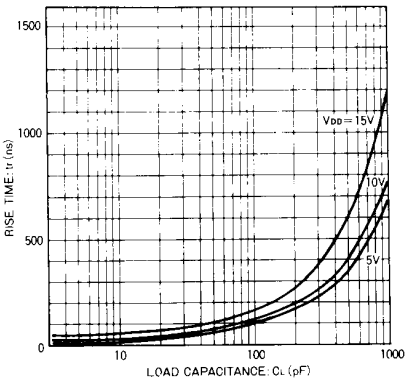


Fig. 10 Rise time vs. load capacitance

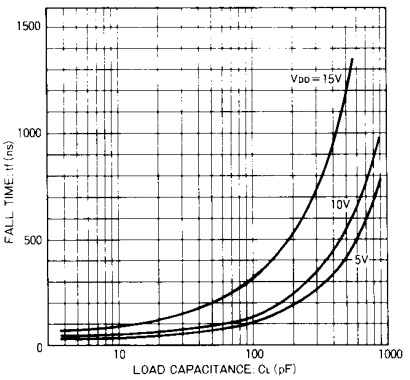


Fig. 11 Fall time vs. load capacitance

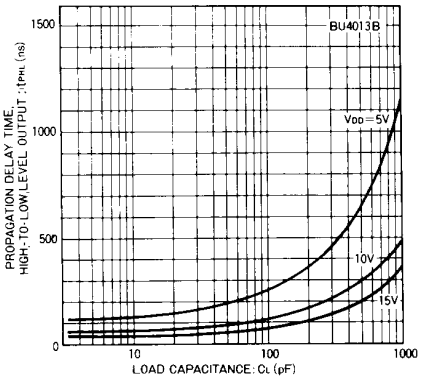


Fig. 12 Propagation delay time, high-to-low output vs. load capacitance

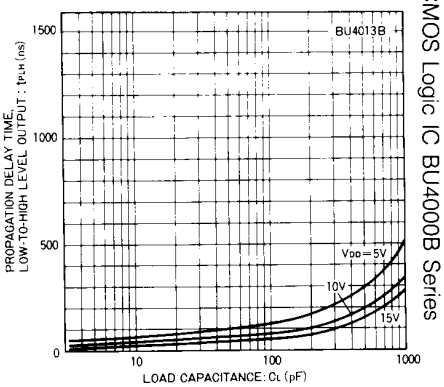


Fig. 13 Propagation delay time, low-to-high output vs. load capacitance

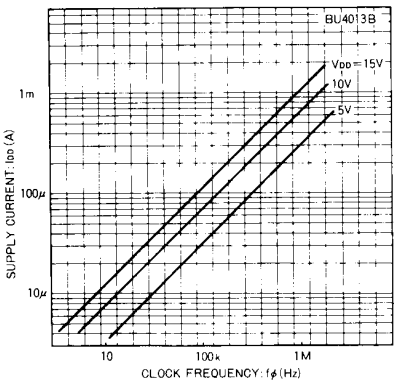


Fig. 14 Supply current vs. clock frequency

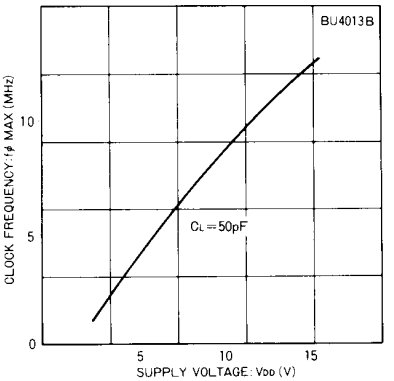


Fig. 15 Clock frequency vs. supply voltage

Block Diagrams

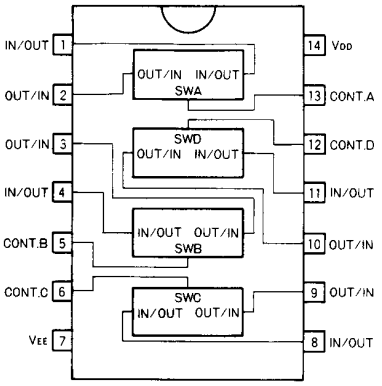


Fig. 16 BU4016B

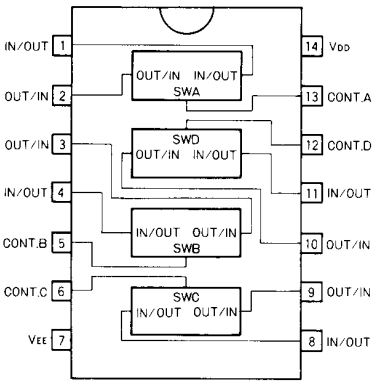


Fig. 17 BU4066B

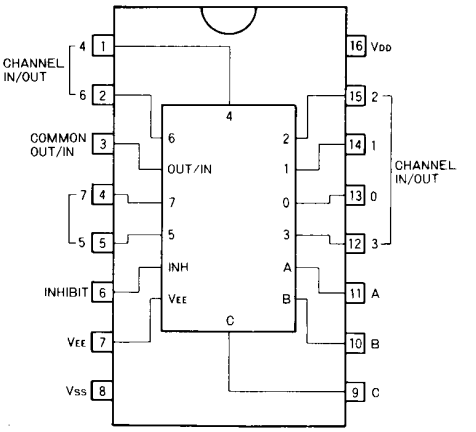


Fig. 18 BU4051B

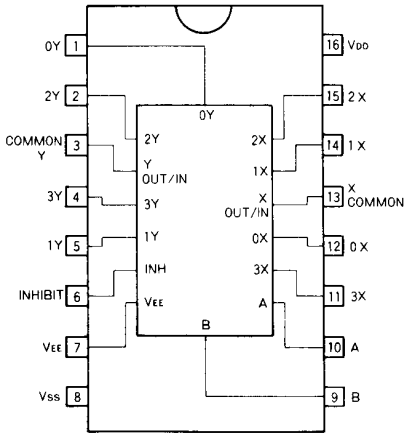


Fig. 19 BU4052B

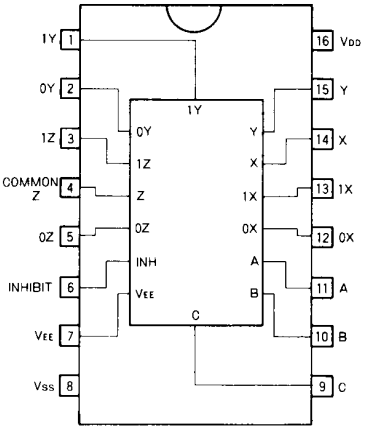


Fig. 20 BU4053B

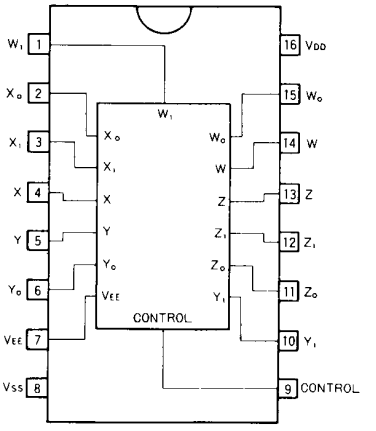


Fig. 21 BU4551B

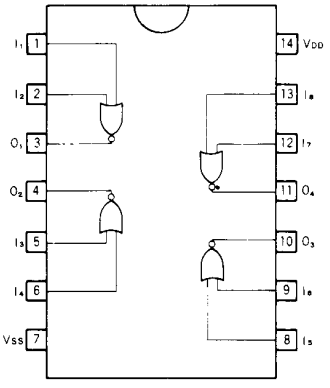


Fig. 22 BU4001B

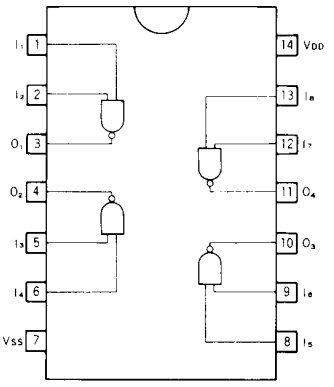


Fig. 23 BU4011B

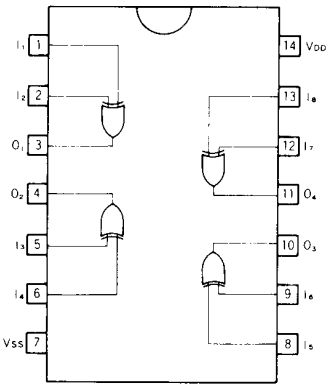


Fig. 24 BU4030B

Block Diagrams

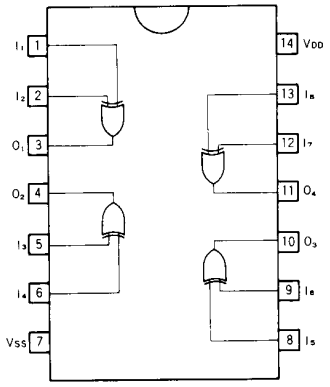


Fig. 25 BU4070B

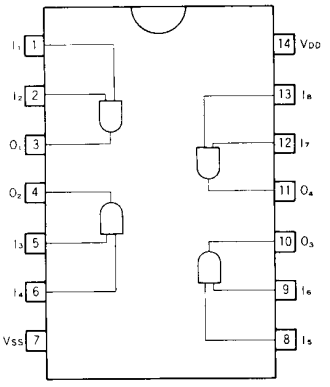


Fig. 26 BU4081B

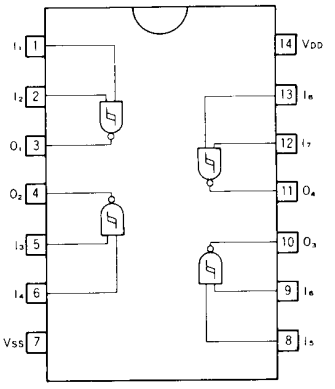


Fig. 27 BU4093B

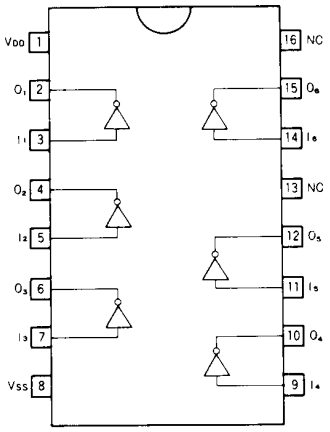


Fig. 28 BU4049UB

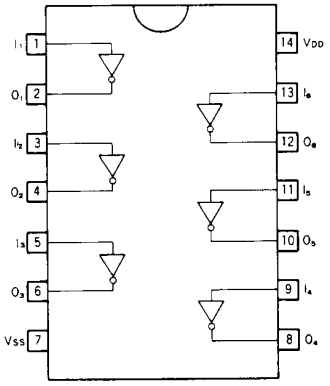


Fig. 29 BU4069UB

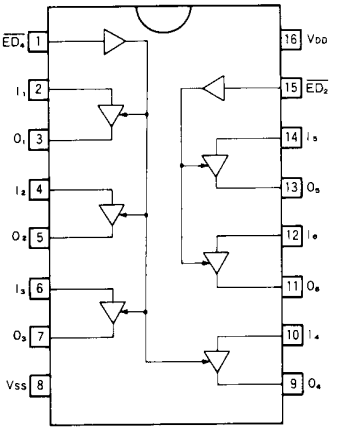


Fig. 30 BU4503B

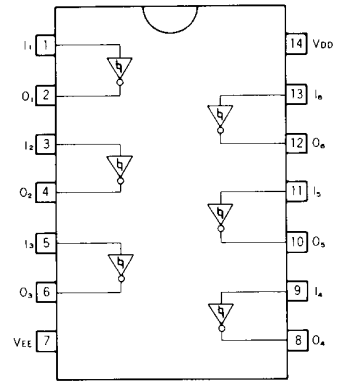


Fig. 31 BU4584B

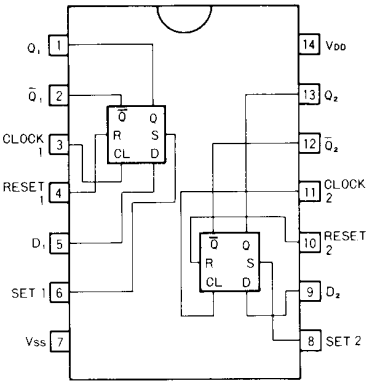


Fig. 32 BU4013B

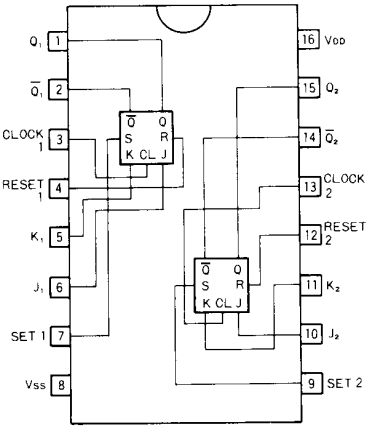


Fig. 33 BU4027B

Block Diagrams

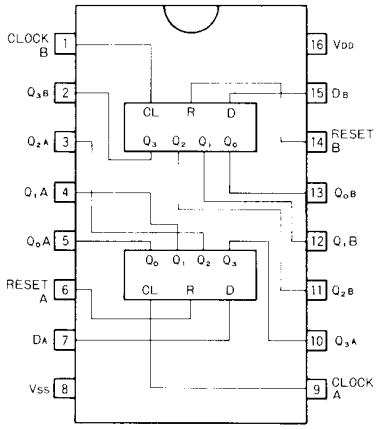


Fig. 34 BU4015B

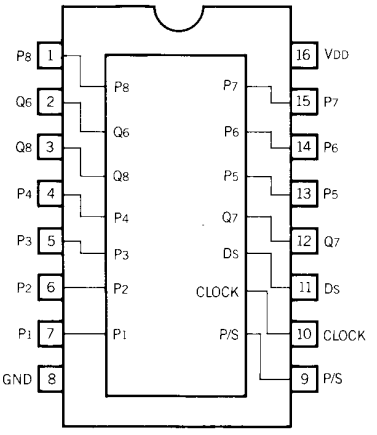


Fig. 35 BU4021B

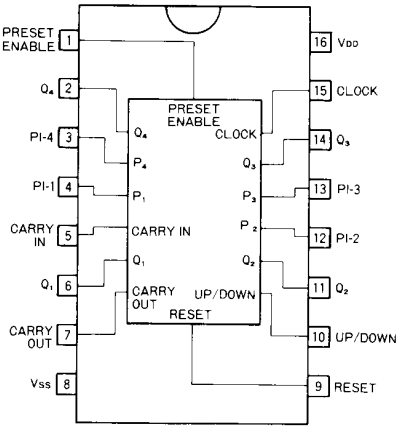


Fig. 36 BU4516B

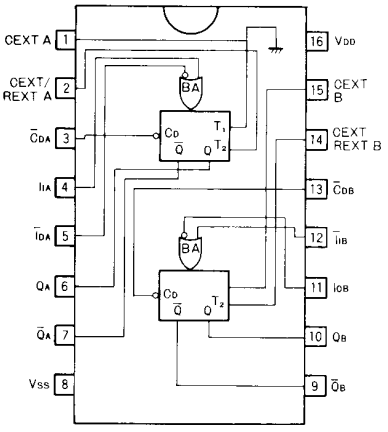


Fig. 37 BU4538B

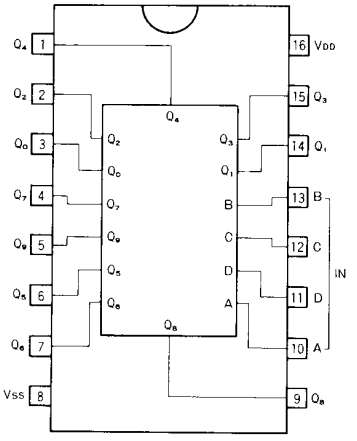


Fig. 38 BU4028B

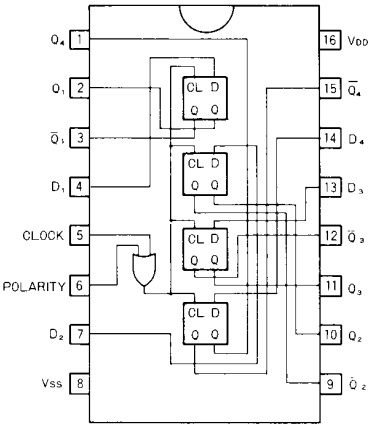


Fig. 39 BU4042B

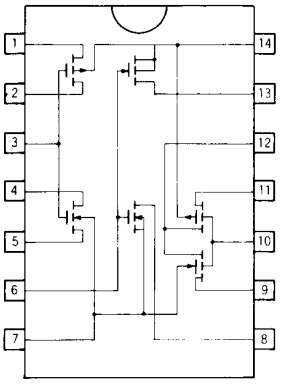


Fig. 40 BU4007UB