ISSUE6 March 1997

Features

- Formats data as per X.25 (CCITT) level-2 standards
- Go-Ahead sequence generation and detection
- Single byte address recognition
- Microprocessor port and directly accessible registers for flexible operation and control
- 19 byte FIFO in both send and receive paths
- Handshake signals for multiplexing data links
- High speed serially clocked output (2.5 Mbps)
- ST-BUS compatibility with programmable channel selection for data and separate timeslot for control information
- Independent watchdog timer
- Facility to disable protocol functions
- Low power ISO-CMOS technology

Applications

- Data link controllers and protocol generators
- Digital sets, PBXs and private packet networks
- D-channel controller for ISDN basic access
- C-channel controller to Digital Network Interface Circuits (typically MT8972)
- Interprocessor communication

Ordering Information

MT8952BE	28 Pin Plastic DIP
MT8952BP	28 Pin PLCC
MT8952BS	28 Pin SOIC

-40°C to 85°C

Description

The MT8952B HDLC Protocol Controller frames and formats data packets according to X.25 (Level 2) Recommendations from the CCITT.

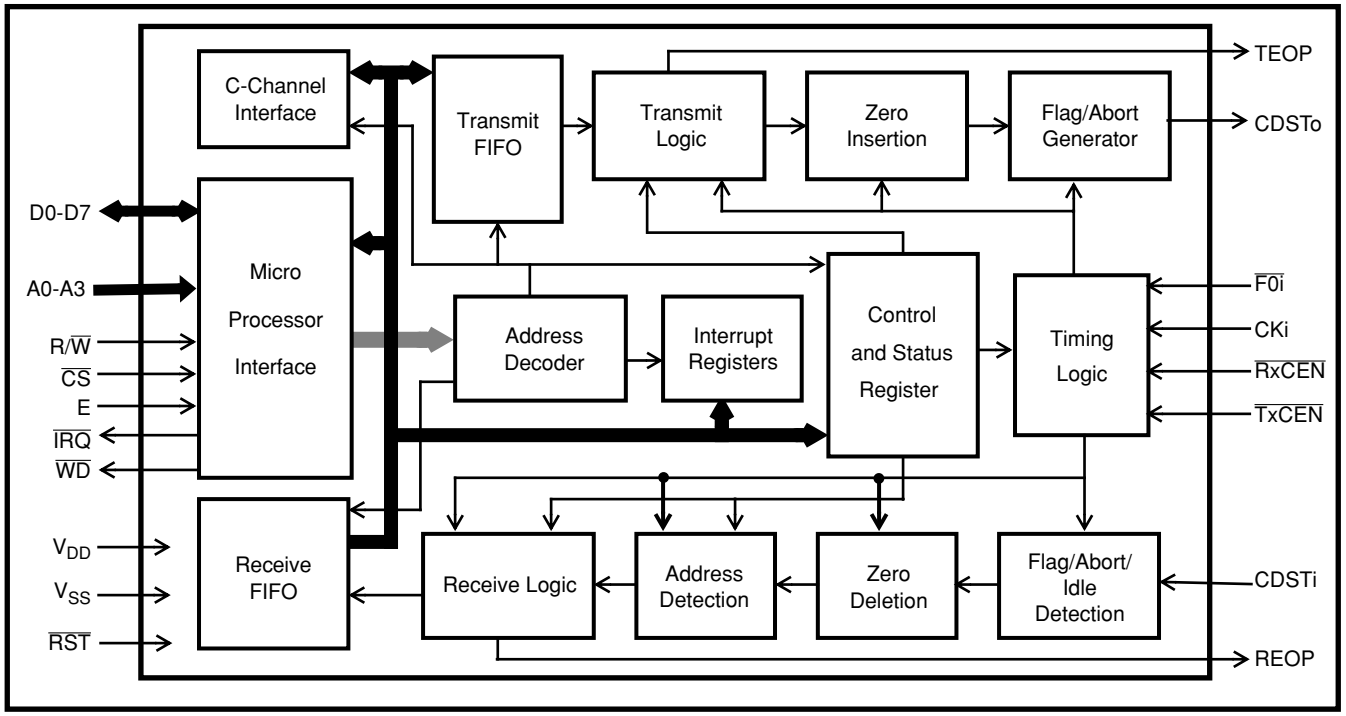


Figure 1 - Functional Block Diagram

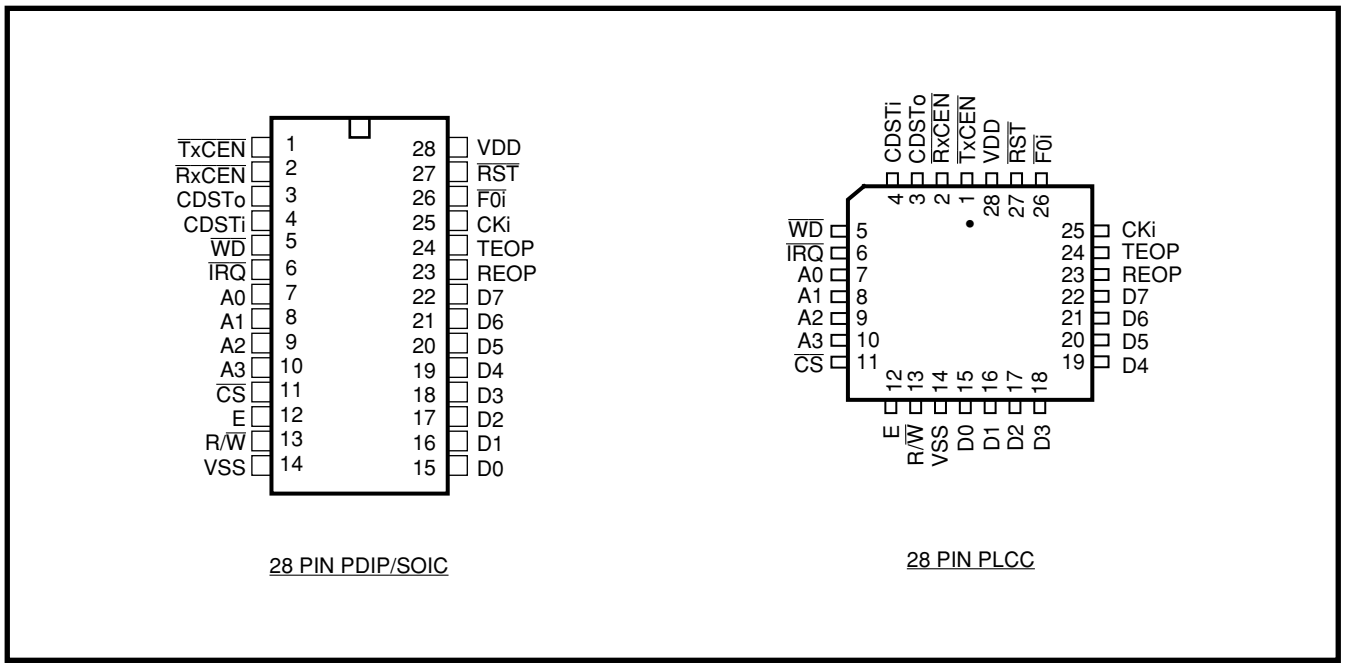


Figure 2 - Pin Connections

Pin Description

Pin No.	Name	Description
1	$\overline{\text{TxCEN}}$	**Transmit Clock Enable -** This active LOW input enables the transmit section in the External Timing Mode. When LOW, CDSTo is enabled and when HIGH, CDSTo is in high impedance state. If the Protocol Controller is in the Internal Timing Mode, this input is ignored.
2	$\overline{\text{RxCEN}}$	**Receive Clock Enable -** This active LOW input enables the receive section in the External Timing Mode. When LOW, CDSTi is enabled and when HIGH, the clock to the receive section is inhibited. If the Protocol Controller is in the Internal Timing Mode, this input is ignored.
3	CDSTo	**C and D channel Output in ST-BUS format** - This is the serial formatted data output from the transmitter in NRZ form. It is in ST-BUS format if the Protocol Controller is in Internal Timing Mode with the data in selected timeslots (0,2,3 and 4) and the C-channel information in timeslot No. 1. If the Protocol Controller is in External Timing Mode, the formatted data is output on the rising edge of the clock (CKi) when $\overline{\text{TxCEN}}$ LOW. If $\overline{\text{TxCEN}}$ is HIGH, CDSTo is in high impedance state.
4	CDSTi	**C and D channel Input in ST-BUS format -** This is the serial formatted data input to the receiver in NRZ form. It must be in ST-BUS format if the Protocol Controller is in Internal Timing Mode with the input data in selected timeslots (0,2,3 and 4) and the C-channel information in timeslot No.1. If the Controller is in External Timing Mode, the serial input data is sampled on the falling edge of the clock CKi when $\overline{\text{RxCEN}}$ is LOW. If $\overline{\text{RxCEN}}$ is HIGH, the clock to receive section is inhibited.
5	$\overline{\text{WD}}$	**Watch-Dog Timer output** - Normally a HIGH level output, going LOW if the Watchdog timer times out or if the external reset ($\overline{\text{RST}}$) is held LOW. The $\overline{\text{WD}}$ output remains LOW as long as $\overline{\text{RST}}$ is held LOW.
6	$\overline{\text{IRQ}}$	**Interrupt Request Output (Open Drain) -** This active LOW output notifies the controlling microprocessor of an interrupt request. It goes LOW only when the bits in the Interrupt Enable Register are programmed to acknowledge the source of the interrupt as defined in the Interrupt Flag Register.
7-10	A0-A3	**Address Bus Inputs** - These bits address the various registers in the Protocol Controller. They select the internal registers in conjunction with $\overline{\text{CS}}$, R/$\overline{\text{W}}$ inputs and E Clock. (Refer to Table 1.)

Pin Description (continued)

Pin No.	Name	Description
11	$\overline{CS}$	**Chip Select Input** - This is an active LOW input enabling the Read or Write operation to various registers in the Protocol Controller.
12	E	**Enable Clock Input** - This input activates the Address Bus and R/$\overline{W}$ input and enables data transfers on the Data Bus.
13	R/$\overline{W}$	**Read/Write Control -** This input controls the direction of data flow on the data bus. When HIGH, the I/O buffer acts as an output driver and as an input buffer when LOW.
14	V_{SS}	Ground (0 Volt).
15-22	D0-D7	**Bidirectional Data Bus -** These Data Bus I/O ports allow the data transfer between the HDLC Protocol Controller and the microprocessor.
23	REOP	**Receive End Of Packet (Output) -** This is a HIGH going pulse that occurs for one bit duration when a closing flag is detected on the incoming packets, or the incoming packet is aborted, or when an invalid packet of 24 or more bits is received.
24	TEOP	**Transmit End Of Packet (Output) -** This is a HIGH going pulse that occurs for one bit duration when a packet is transmitted correctly or aborted.
25	CKi	**Clock Input (Bit rate clock or 2 x bit rate clock in ST-BUS format while in the Internal Timing Mode and bit rate Clock in the External Timing Mode)** - This is the clock input used for shifting in/out the formatted packets. It can be at bit rate (C2i) or twice the bit rate ($\overline{C4i}$) in ST-BUS format while the Protocol Controller is in the Internal Timing Mode. Whether the clock should be C2i (typically 2.048 MHz) or $\overline{C4i}$ (typically 4.096 MHz) is decided by the BRCK bit in the Timing Control Register. If the Protocol Controller is in the External Timing Mode, it is at the bit rate.
26	$\overline{F0i}$	**Frame Pulse Input -** This is the frame pulse input in ST-BUS format to establish the beginning of the frame in the Internal Timing Mode. This is also the signal clocking the watchdog timer.
27	$\overline{RST}$	**RESET Input -** This is an active LOW Schmitt Trigger input, resetting all the registers including the transmit and receive FIFOs and the watchdog timer.
28	V_{DD}	**Supply (5 Volts).**

Address Bits				Registers	
A3	**A2**	**A1**	**A0**	**Read**	**Write**
0	0	0	0	FIFO Status	-
0	0	0	1	Receive Data	Transmit Data
0	0	1	0	Control	Control
0	0	1	1	Receive Address	Receive Address
0	1	0	0	C-Channel Control (Transmit)	C-Channel Control (Transmit)
0	1	0	1	Timing Control	Timing Control
0	1	1	0	Interrupt Flag	Watchdog Timer
0	1	1	1	Interrupt Enable	Interrupt Enable
1	0	0	0	General Status	-
1	0	0	1	C-Channel Status (Receive)	-

Table 1. Register Addresses

Introduction

The MT8952B HDLC Protocol Controller handles bit oriented protocol structure and formats the data as per the packet switching protocol defined in the X.25 (Level 2) recommendations of the CCITT. It transmits and receives the packeted data (information or control) serially in a format shown in Figure 3 , while providing the data transparency by zero insertion and deletion. It generates and detects the flags, various link channel states and the abort sequence. Further, it provides a cyclic redundancy check on the data packets using the CCITT defined polynomial. In addition, it can generate and detect a Go Ahead sequence and recognize a single byte address in the received frame. There is also a provision to disable the protocol functions and provide transparent access to the serial bus through the parallel port.

Frame Format

All frames start with an opening flag and end with a closing flag as shown in Figure 3. Between these two flags, a frame contains the data and the frame check sequence (FCS).

FLAG	DATA FIELD	FCS	FLAG
One Byte	n Bytes ($n \geq 2$)	Two Bytes	One Byte

Figure 3. Frame Format

Flag:

The flag is a unique pattern of 8 bits (01111110) defining the frame boundary. The transmit section generates the flags and appends them automatically to the frame to be transmitted. The receive section searches the incoming packets for flags on a bit-by-bit basis and establishes frame synchronization. The flags are used only to identify and synchronize the received frame and are not transferred to the FIFO.

Data:

The data field refers to the Address, Control and Information fields defined in the CCITT recommendations. A valid frame should have a data field of at least 16 bits. The first byte in the data field is the address of the frame. If RxAD bit in the Control Register is HIGH, the incoming packet is recognized only if the address byte matches the byte stored in the Receive Address Register or the address byte is the All-Call Address (all ONEs). The LSB of the Receive Address Register is set LOW permanently and the comparison is done only on upper seven bits of the received address byte. The address detection can be limited only to the upper six bits by setting HIGH both RA6/7 and RxAD bits in the Control Register.

Frame Check Sequence (FCS):

The 16 bits following the data field are the frame check sequence bits. The generator polynomial is:

$$G(x)=x^{16}+x^{12}+x^5+1$$

The transmitter calculates the FCS on all bits of the data field and transmits after the data field and before the end flag. The receiver performs a similar computation on all bits of the received data and FCS fields and the result is compared with $FOB8_{Hex}$. If it matches, the received data is assumed error free. The error status of the received packet is indicated by D7 and D6 bits in the FIFO Status Register.

Zero Insertion and Deletion:

The Protocol Controller, while sending either data from the FIFO or the 16 bits FCS, checks the transmission on a bit-by-bit basis and inserts a ZERO after every sequence of five contiguous ONEs (including the last five bits of FCS) to ensure that the flag sequence is not simulated. Similarly the receiver examines the incoming frame content and discards any ZERO directly following the five contiguous ONEs.

Abort:

The transmitter aborts a frame by sending eight consecutive ONEs. The FA bit in the Control Register along with a write operation to the Transmit Data Register enables the transmission of abort sequence instead of the byte written to the register. On the receive side, the ABRT bit in the General Status Register is set whenever an abort sequence (7 or more continuous 1's) is received. The abort sequence causes the receiver to abandon whatever it was doing and start searching for a start flag. The FA bit in the Interrupt Status Register is set when an abort sequence is received following a start flag and at least four data bytes (minimum for a valid frame).

Interframe Time Fill and Link Channel States

When the HDLC Protocol Controller is not sending packets, the transmitter can be in any of three states mentioned below depending on the status of the IFTF0 and IFTF1 bits in the Control Register. These bits are also used to disable the protocol function to provide the transparent parallel access to the serial bus through the microprocessor port.

Idle state:

The Idle state is defined as 15 or more contiguous ONEs. When the HDLC Protocol Controller is observing this condition on the receiving channel, the Idle bit in the General Status Register is set HIGH. On the transmit side, the Protocol Controller ends the Idle state when data is loaded into the transmit FIFO.

Interframe time fill state:

The Protocol Controller transmits continuous flags ($7E_{Hex}$) in Interframe time fill state and ends this state when data is loaded into the transmit FIFO.

Go Ahead state:

Go Ahead is defined by the 9 bit sequence 011111110 ($7F_{Hex}$ followed by a ZERO), and hence contiguous 7F's appear as Go Aheads. Once the transmitter is in 'Go Ahead' state, it will continue to remain so even after the data is loaded into the FIFO. This state can only be changed by setting the IFTF bits in the Control Register to something other than 'GO Ahead'. The reception of this sequence is indicated by GA bit in the General Status Register and the Protocol Controller can generate an interrupt if enabled to do so by the GA bit in the Interrupt Enable Register.

Transparent Data Transfer State:

The Protocol Controller, in this state, disables the protocol functions defined earlier and provides bi-directional access to the serial bit streams through the parallel port. Like other states, the transparent data transfer can be selected in both timing modes.

Invalid Frames

Any frame shorter than 32 bits between the opening and closing flags (corresponding to 16 bits of data and 16 bits FCS) is considered invalid. The Protocol Controller ignores the frame only if the frame length is less than 24 bits between the flags. For frames of length 24 to 32 bits, it transfers the data field to FIFO and tags it as having bad FCS in the FIFO Status Register.

Functional Description

The functional block diagram of the HDLC Protocol Controller is shown in Figure 1. It has two ports. The serial port transmits and receives formatted data packets and the parallel port provides a microprocessor interface for access to various registers in the Protocol Controller.

The serial port can be configured to operate in two modes depending on the IC bit in the Timing Control Register. It can transmit/receive the packets on selected timeslots in ST- BUS format or it can, using the enable signals ($\overline{TxCEN}$ and $\overline{RxCEN}$), transmit/receive the packets at a bit rate equal to CKi clock input.

The microprocessor port allows parallel data transfers between the Protocol Controller and a 6800/6809 system bus. This interface consists of Data Bus (D0-D7), Address Bus (A0-A3), E Clock, Chip Select ($\overline{CS}$) and R/$\overline{W}$ control. The micro-processor can read and write to the various registers in the Protocol Controller. The addresses of these registers are given in Table 2. The $\overline{IRQ}$ is an open drain, active LOW output indicating an interrupt request to CPU. Control and monitoring of many different interrupts that may originate from the protocol controller is implemented by the Interrupt Flag Register (IFR) and the Interrupt Enable Register (IER). Specific events have been described that set a bit HIGH in the Interrupt Flag Register. Such an event does not necessarily interrupt the CPU. To assert an interrupt (pull $\overline{IRQ}$ output LOW) the bit in IER that coincides with the Interrupt Flag Register must be set HIGH. The IRQ bit in the General Status Register is the complement of $\overline{IRQ}$ pin status. If an interrupt is asserted, this bit will be set HIGH otherwise it will be LOW.

TEOP and REOP Outputs:

The HDLC Protocol Controller provides two separate signals TEOP & REOP indicating the end of packet transmitted and received respectively. TEOP is a HIGH going pulse for one bit duration asserted during the last bit of the closing flag or Abort sequence of the transmit packet. REOP is also a HIGH going pulse occurring for one bit period when a closing flag is received or an incoming packet is aborted or an invalid packet of 24 or more bits is detected. However, REOP is not generated for invalid packets of length less than 24 bits. These 'end of packet' signals are useful in multiplexing several data links on to a single HDLC Protocol Controller.

Timing Modes

There are two timing modes the Protocol Controller can be run in. These timing modes refer only to the configuration of the serial port and are not related to the microprocessor port.

Internal Timing Mode

The Internal Timing Mode is intended for an easy interface to various products using ST-BUS

architecture, particularly Zarlink's Digital Network Interface Circuit (DNIC - MT8972). The data/packets are shifted in/out serially in ST-BUS format using the timing signals $\overline{F0i}$ and C2i/$\overline{C4i}$. In addition to framing the data, the Protocol Controller reserves one channel (channel-1) on the ST-BUS for carrying control information (C-channel) and this timeslot can not be used for the packetized data. While the Protocol Controller is in the Internal Timing Mode, the clock input CKi can be either at the bit rate or at 2∞bit rate depending on the BRCK bit in the Timing Control Register as shown in Table 2.

BRCK Bit	CKi Input	Output Data Rate
0	4.096 MHz/$\overline{C4i}$	2.048 Mbps
1	2.048 MHz/C2i	2.048 Mbps

Table 2. Output Bit Rate In Internal Timing Mode

The Protocol Controller uses the ST-BUS timing signals $\overline{F0i}$ and C2i/$\overline{C4i}$, and enables the transmitter and receiver sections in the appropriate timeslots as determined by TC0-TC3 bits in the Timing Control Register.

The $\overline{TxCEN}$ and $\overline{RxCEN}$ inputs are ignored in this mode.

C-Channel Interface

This is a separate control channel (C-channel) interface relevant only in the Internal Timing Mode. The data stored in the C-Channel Control Register is shifted out during the channel-1 timeslot of the outgoing ST-BUS (CDSTo) and the C1EN bit in the Timing Control Register enables the transmission. The transmission of C-Channel is independent of packet/data transmission. The data received on channel-1 of the incoming ST-BUS (CDSTi) is shifted into the C-Channel Status Register independently and it is updated continuously.

Both the C-channel registers are accessible by the accompanying CPU through the parallel port.

External Timing Mode

In the External Timing Mode, the transmit and receive sections are enabled independently by $\overline{TxCEN}$ and $\overline{RxCEN}$ control inputs and the formatted data packets are shifted in/out serially at a rate equal to the clock frequency on CKi. The output is transmitted on the rising edge and the receiver samples the input on the falling edge of the clock. The $\overline{TxCEN}$ and $\overline{RxCEN}$ controls are independent and asynchronous and have effect only after the current bit in the packet is transmitted/received.

Although the protocol controller provides the packetized data on a limited number of channels on the ST-BUS while operating in the Internal Timing Mode, it can packetize the data on any or all the channels of the ST-BUS if it is operated in the External Timing Mode with appropriate enable signals on $\overline{TxCEN}$ and $\overline{RxCEN}$.

Transparent Data Transfer

By setting the IFTF bits in the Control Register appropriately, the protocol functions can be disabled. This provides a bidirectional access to the serial port through the microprocessor interface, with 19 byte deep FIFO in each direction. The transparent data transfer facility functions in bytewide format and is available in both timing modes except when the timing control bits are set for one bit/frame during the Internal Timing Mode.

The transmit data is shifted out serially on CDSTo and the operation being bytewide, only the least significant bits of each byte loaded are transmitted, if the timing control bits are set to select 2, 6 or 7 bits/ frame. When the transmit FIFO is empty, the last byte or the portion the last byte, written to the FIFO is transmitted repeatedly. Similarly the serial data on CDSTi is shifted in and converted to bytewide format. In case the timeslot selected is 2, 6 or 7 bits/frame, the reception involves only the most significant bits of each byte.

It should be noted that none of the protocol related status or interrupt bits are applicable in transparent data transfer state. However, the FIFO related status and interrupt bits are pertinent and carry the same meaning as they do while performing the protocol functions.

Watchdog Timer

This is a fixed eleven stage binary counter with $\overline{F0i}$ as the input and $\overline{WD}$ as the output from the last stage. This counter can be reset either by the external input ($\overline{RST}$) or by writing XXX0 1010 to the Watchdog Timer Register. The $\overline{WD}$ output is normally HIGH and if the Watchdog Timer Register is not written within 2^{10} cycles of $\overline{F0i}$ input after it is reset, the $\overline{WD}$ output will go LOW for a period of 2^{10} cycles of $\overline{F0i}$. Even though the $\overline{F0i}$ input is not required for formatting data in the External Timing Mode, it is necessary for the operation of the watchdog timer.

Order of Bit Transmission/Reception

The Least Significant Bit (LSB) corresponding to D0 on the data bus is transmitted first on the serial output (CDSTo). On the receiving side, the first bit received on the serial input (CDSTi) is considered as the LSB and placed on D0 of the data bus.

Registers

There are several registers in the HDLC Protocol Controller accessible to the associated microprocessor via the data bus. The addresses of these registers are given in Table 1 and their functional details are given below.

FIFO Status Register (Read):

This register (Figure 4) indicates the status of transmit and receive FIFOs and the received byte as described below.

D7	D6	D5	D4	D3	D2	D1	D0
Rx Byte Status		Rx FIFO Status		Tx FIFO Status		LOW	LOW

Figure 4 - FIFO Status Register

Rx Byte Status: These two bits (D7 and D6) indicate the status of the received byte ready to be read from the receive FIFO. The status is encoded as shown in Table 3.

Rx Byte Status Bits		Status
D7	D6	
0	0	Packet Byte
0	1	First Byte
1	0	Last Byte (Good FCS)
1	1	Last Byte (Bad FCS)

Table 3. Received Byte Status

Rx FIFO Status: These bits (D5 and D4) indicate the status of receive FIFO as given by Table 4. The Rx FIFO status bits are not updated immediately after an access of the Rx FIFO (a read from the microprocessor port, or a write from the serial port), to avoid the existence of unrecoverable error conditions.

When in external timing mode, the MT8952B must receive two falling edges of the clock signal at the CKi input before the Rx FIFO status bits will be updated. When in internal 2.048 MHz timing mode, the MT8952B must receive two falling edges of the C2i clock before the Rx FIFO status bits will be updated. When in internal 4.096 MHz timing mode, the MT8952B must receive four falling edges of the C4i clock before the Rx FIFO status bit will be updated (see the section on Receive Operation - Normal Packets).

Rx FIFO Status Bits		Status
D5	D4	
0	0	Rx FIFO Empty
0	1	Less than or equal to 14 bytes
1	0	Rx FIFO Full
1	1	Greater than or equal to 15 bytes

Table 4. Receive FIFO Status

Tx FIFO Status: These two bits (D3 and D2) indicate the status of transmit FIFO as shown in Table 5.

Tx FIFO Status Bits		Status
D3	D2	
0	0	Tx FIFO Full
0	1	Greater than or equal to 5 bytes
1	0	Tx FIFO Empty
1	1	Less than or equal to 4 bytes

Table 5. Transmit FIFO Status

The Tx FIFO status bits are updated in the same manner as the Rx FIFO bits, except that in external timing mode, and in internal 2.048 Mbps timing mode, the Tx FIFO status bits are updated after two falling edges of the CKi or the C2i signal (see the section on Transmit Operation - Normal Packets).

Receive Data Register (Read):

Reading the Receive Data Register (Figure 5) puts the first byte from the receive FIFO on the data bus. The first bit of the data received on the serial input (CDSTi) is considered to be the LSB and is available on D0 of the data bus.

D7	D6	D5	D4	D3	D2	D1	D0
RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0

Figure 5 - Receive Data Register

Transmit Data Register (Write):

Writing to Transmit Data Register (Figure 6) puts the data present on the data bus into the transmit FIFO. The LSB (D0) is transmitted first.

D7	D6	D5	D4	D3	D2	D1	D0
TD7	TD6	TD5	TD4	TD3	TD2	TD1	TD0

Figure 6 - Transmit Data Register

Control Register (Read/Write):

The Control Register (Figure 7) is used for general purpose control of the HDLC Protocol Controller. The bits contained in this register and their functions are described below.

D7	D6	D5	D4	D3	D2	D1	D0
TxEN	RxEN	RxAD	RA6/7	IFTF1	IFTF0	FA	EOP

Figure 7 - Control Register

TxEN -Transmit Enable: When set HIGH, this bit enables the transmitter and when LOW, disables it setting the serial output (CDSTo) to high impedance state. If the transmitter is disabled during the transmission of a packet using this bit, the Protocol Controller will wait until the completion of the packet and closing flag is transmitted or the packet is aborted before setting the output (CDSTo) to high impedance state. Thus TxEN bit controls the transmission packet by packet unlike $\overline{\text{TxCEN}}$ input (pin 1) which controls it bit-by-bit. However, if the Protocol Controller is in transparent data transfer state, the transmission will be stopped within two bit periods (maximum) and set the output to high impedance state.

RxEN - Receive Enable: This bit enables the receiver when set HIGH and disables it when LOW. If this bit goes LOW during the reception of the packet, the receiver can only be disabled after the current packet and its closing flag are received or an abort is detected. Thus RxEN bit controls the receiver section packet by packet unlike $\overline{\text{RxCEN}}$ input (pin 2) which controls it bit-by-bit. However, if the Protocol Controller is in transparent data transfer state, the receiver will be disabled immediately.

RxAD - Receive Address Detect: This bit when set HIGH, enables the address detection for the received packets. This causes the receiver to recognize only those packets having a unique address as programmed in the Receive Address Register or if the address byte is the All-Call address (all ONEs). The address comparison is done only on seven bits (compatible to the first byte of the address field defined in LAPD-CCITT) and an All-Call is defined as all ONEs in upper seven bits of the received address field. If RxAD is LOW, the address detection is disabled and every valid packet is recognized.

RA6/7 - Receive Address Six/Seven bits: This bit, when set HIGH, limits the address detection only to the upper six bits of the received address byte (last 6 bits of received address field) and when LOW, allows the address comparison on seven bits. An "all call", in this case is defined as all ONEs in the upper six bits only. RA6/7 is ignored if the address detection is disabled (RxAD=0).

IFTF0 and IFTF1 - Interframe Time Fill: Setting these bits according to the table below (Table 6) causes the transmitter to be in one of the active or idle states or allows the Protocol Controller to be in the transparent data transfer state.

IFTF Bits		Result
IFTF1	IFTF0	
0	0	Idle State (All ONEs)
0	1	Interframe Time Fill state (Continuous Flags)
1	0	Transparent Data Transfer
1	1	Go Ahead state (Continuous $7F_{HEX}$)

Table 6. Interframe Time Fill Bits

FA - Frame Abort: When set HIGH, this bit'tags' the next byte written to the transmit FIFO and causes an abort sequence (eight ONEs) to be transmitted when it reaches the bottom of the FIFO. The abort sequence will be transmitted instead of the byte that was tagged. The FA bit is cleared to ZERO upon writing the data to the transmit FIFO. As a result, a 'read' of this register bit will not reflect the last data written to it.

EOP - End Of Packet: Writing a ONE to this bit 'tags' the next byte written to the transmit FIFO to indicate that it is the last data byte of the packet. This bit is cleared to ZERO upon writing the data to the transmit FIFO. As a result, a read of this register bit will not indicate the last data written to it.

Receive Address Register (Read/Write):

D7	D6	D5	D4	D3	D2	D1	D0
RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0

Figure 8 - Receive Address Register

The data in this register (Figure 8) defines the unique address for the HDLC Protocol Controller. If address recognition is enabled using the RxAD and RA6/7 bits in the Control Register, an incoming packet is recognized only if its address byte (seven or six most significant bits) matches the corresponding bits in this register or if the address is an "all-call". The LSB

of the Receiver Address Register is set LOW permanently and the address comparison is done only on remaining bits of the register.

C-Channel Control Register (Read/Write):

D7	D6	D5	D4	D3	D2	D1	D0
CT7	CT6	CT5	CT4	CT3	CT2	CT1	CT0

Figure 9 - C-Channel Control Register

The data written to this register (Figure 9) is transmitted on channel-1 slot of the outgoing ST-BUS (CDSTo), when enabled by C1EN bit in the Timing Control Register. This feature can only be used when the HDLC Protocol Controller is in the Internal Timing Mode.

Timing Control Register (Read/Write):

The Timing Control Register (Figure 10) controls the timing mode and other related operations and provides a software reset to the Protocol Controller. The various bits in this register are described below:

D7	D6	D5	D4	D3	D2	D1	D0
RST	IC	C1EN	BRCK	TC3	TC2	TC1	TC0

Figure 10. Timing Control Register

RST - Reset: When this bit is set HIGH, all the registers in the HDLC Protocol Controller are reset and the data in the FIFOs is lost. This is equivalent to the external reset with the exception that the RST bit does not affect itself or the Watchdog Timer Register and $\overline{WD}$ output. The RST bit must be "cleared" (written as a logic "0") twice before the MT8952B will be removed from its reset state (see section on RESET operation).

IC - Internal Control: When this bit is cleared to ZERO, the Protocol Controller is in the External Timing Mode. The transmit and receive sections are enabled by the inputs $\overline{TxCEN}$ and $\overline{RxCEN}$ respectively, and $\overline{F0i}$ is used only for the watchdog timer operation. When this bit is a ONE, the Protocol Controller is in the Internal Timing Mode. The transmit and receive sections are enabled by the internally generated timings derived from the inputs CKi and $\overline{F0i}$. The $\overline{F0i}$ input defines the beginning of a frame (Figure 24) and the transmitter and receiver sections are enabled in the timeslots as determined by the bits TCO-TC3. The inputs $\overline{TxCEN}$ and $\overline{RxCEN}$ are ignored in this mode.

C1EN - Channel-1 Enable: When HIGH, it enables the transmission of C-channel information on channel-1 time-slot of the outgoing ST-BUS (CDSTo) and when LOW, puts CDSTo into high impedance state during that period. However, the C-channel information is received independently and the C-channel Status Register is updated continuously. Note that C1EN has relevance only during the Internal Timing Mode.

BRCK- Bit Rate Clock: This bit is used during the Internal Timing Mode to select the clock rate and ignored if the Protocol Controller is in the External Timing Mode. It should be set HIGH if the input clock (CKi) is at the bit rate (C2i) and should be LOW for the clock input at 2 x bit rate ($\overline{C4i}$). In both cases, the clock should be properly phase related to $\overline{F0i}$ as shown in Figure 25.

TC0-TC3 - Timing Control Bits: In the Internal Timing Mode the transmitter and the receiver sections are enabled during the times defined by the Timing Control Bits TC0-TC3 (Table 7). This applies only to the ST-BUS channels 0, 2, 3 and 4 carrying the packets or transparent data (channel-1 pertains to C-channel information). The output CDSTo is put during the remaining time intervals not enabled by these bits.

Timing Control Bits				ST-BUS Channel Number	Bits /Frame
TC3	TC2	TC1	TC0		
X	0	0	0	0	1
X	0	0	1	0	2
0	0	1	0	0	6
1	0	1	0	0	7
X	0	1	1	2	8
X	1	0	0	3	8
X	1	0	1	4	8
X	1	1	0	2 and 3	16
X	1	1	1	2, 3 and 4	24

X : Don't Care **Table 7. Timing Control Bits**

Interrupt Flag Register (Read):

Reading the Interrupt Flag Register puts the interrupt status bits on the data bus. This register is reset when it is read and a particular bit will not be set until its particular condition occurs again. The functional details of each bit are provided in Figure 11.

D7	D6	D5	D4	D3	D2	D1	D0
GA	EOPD	Tx DONE	FA	Tx 4/19 FULL	Tx URUN	Rx 15/19 FULL	Rx OFLW

Figure 11. Interrupt Flag Register

GA - Go Ahead: This bit when set HIGH, indicates the detection of 'go ahead' sequence on the incoming data stream (CDSTi).

EOPD - End of Packet Detect: A HIGH on this bit confirms the reception of an 'end of packet' flag, an abort sequence or an invalid packet of 24 or more bits on the incoming data stream (CDSTi).

Tx DONE - Transmitter Done: This bit, when HIGH, indicates that the packet transmission is complete and the Transmit FIFO is empty. The falling edge of TEOP output causes this interrupt status bit to be set HIGH if the FIFO is empty.

FA - Frame Abort: This bit is set HIGH to indicate that a frame abort has been detected on the incoming data stream.

Tx 4/19 FULL - Transmit FIFO 4/19 full: This bit if set HIGH, indicates that the transmit FIFO has only 4 bytes remaining in it and another 15 bytes could be loaded. This bit has significance only when the transmit FIFO is being depleted and not when it is getting loaded.

Tx URUN - Transmit FIFO underrun: This bit when HIGH, identifies that the transmit FIFO is empty without the Protocol Controller being given the 'end of packet' indication. This indicates that the transmit FIFO has underrun and the Protocol Controller will transmit an abort sequence automatically. Tx DONE will be set 8 bit times after Tx URUN is set.

Rx15/19 FULL - Receive FIFO 15/19 full: This bit when HIGH, confirms that the receive FIFO has 15 bytes in it and it can receive four more bytes.

Rx OFLW - Receive FIFO overflow: This bit when set HIGH, indicates that the receive FIFO is full and a 'write' occurred indicating an overflow. The byte causing this and all the subsequent bytes written while the FIFO is in this state are lost. The receiver begins to search for a new start flag.

Watchdog Timer Register (Write):

The Watchdog Timer Register operates in conjunction with the Watchdog Timer and the $\overline{WD}$ output. Writing the code of XXX0 1010 in the register resets the WD timer. If the register is not re-written within 2^{10} cycles of $\overline{F0i}$ after resetting the timer, the $\overline{WD}$ output goes LOW. This register serves the sole purpose of resetting the timer and hence relevant only if it is written with the above data.

Interrupt Enable Register (Read/Write):

This register enables/disables the interrupts as specified in the Interrupt Flag Register (IFR). Setting HIGH the appropriate bits in this register (IER) enables the associated interrupt source. However, the masked bits in the IFR are still valid but they do not cause the $\overline{IRQ}$ output to go LOW. The description of the bits enabling the various interrupts is identical to those of the Interrupt Flag Register.

General Status Register (Read):

This register (Figure 12) contains the general status information on the Protocol Controller.

D7	D6	D5	D4	D3	D2	D1	D0
Rx OFLW	Tx URUN	GA	ABRT	IRQ	IDLE	LOW	HIGH

Figure 12 - General Status Register

Rx OFLW - Receive FIFO overflow: This bit, if set HIGH, indicates that the receive FIFO has overflowed. The byte causing this and all the subsequent bytes written while the FIFO is in this state are lost. Note that this bit is the same as the Rx OFLW bit in Interrupt Flag Register (IFR) and can only be cleared by reading the IFR.

Tx URUN - Transmit FIFO Underrun: When HIGH, this bit indicates that the transmit FIFO has underrun. Under this condition the packet being transmitted is aborted. This bit is the same as the Tx URUN bit in the Interrupt Flag Register (IFR) and can only be cleared when the IFR is read.

GA - Go Ahead: This bit is set HIGH if a 'go ahead' is received on the incoming data stream and is cleared when the Interrupt Flag Register is read. This bit is the same as the GA bit in the IFR.

ABRT - Abort: The reception of contiguous seven ONEs on incoming data, sets this bit HIGH and reading the General Status Register, clears it.

IRQ - Interrupt Request: This bit refers to the status of the interrupt request output from the Protocol Controller. If HIGH, it indicates that the $\overline{IRQ}$ (pin 6) output is LOW and vice versa.

IDLE - Idle Channel: This bit, if set HIGH, identifies that the receiver is detecting an idle channel at its input (minimum 15 ONEs).

C-Channel Status Register (Read):

D7	D6	D5	D4	D3	D2	D1	D0
CR7	CR6	CR5	CR4	CR3	CR2	CR1	CR0

Figure 13. C-Channel Status Register

The C-Channel Register (Figure 13) continuously stores the data received during the channel-1

timeslot of the incoming ST-BUS (CDSTi) during the Internal Timing Mode of the Protocol Controller.

RESET

When the MT8952B is reset by a low going pulse on the $\overline{RST}$ pin or by setting (logic high) the RST bit in the Timing Control Register, the device is put into the following state:

a) All bits in the Timing Control Register are cleared (logic 0) by an external reset. An internal reset clears all bits except the RST bit.

b) All bits in the Interrupt Enable Register are cleared (logic 0).

c) All bits in the Control Register are cleared (logic 0).

d) All bits in the Interrupt Register are cleared (logic 0).

e) All bits in the General Status Register are cleared (logic 0) except for the two least significant bits.

f) Receive and Transmit Registers are cleared and the FIFO Status Register reflects their state accordingly.

g) The $\overline{WD}$ output is reset low by an external reset but is not affected by an internal reset.

h) The Transmitter and the Receiver are disabled.

Transmit Operation

After a reset, which the external circuitry should provide upon power up, the transmit section is disabled. Before enabling this section, the timing should be set up. On reset, the serial port is set to External Timing Mode. In case this is not desired, the Timing Control Register should be written to with the appropriate data. Once in the correct timing mode, the Transmit Enable (TxEN) bit in the Control Register can be set. Now that the transmitter is enabled it will be in the Idle channel state. If any other channel state or the transparent data transfer facility is required, the IFTF bits in the Control Register should be set accordingly.

Normal Packets:

To start a packet, the data is written into the transmit FIFO starting with the address field. All the data must be written to the FIFO in a bytewide manner. When the data is detected in the transmit FIFO, the protocol controller will proceed in one of the following ways:

If the transmitter is in idle state, the present byte of eight ONEs being transmitted is completed and then followed by a start flag and subsequently the data in the transmit FIFO is transmitted.

If the transmitter is in the interframe time fill state, the flag presently being transmitted is finished and then another start flag is transmitted before transmitting the data from the transmit FIFO.

If the transmitter is in go ahead state, it continues to be in that state even after the data is loaded into the FIFO. Only when the IFTF bits are set to choose something other than go ahead will the data be transmitted.

If the transmitter is in transparent data transfer state, the protocol functions are disabled and the data in the transmit FIFO is transmitted on CDSTo.

To indicate that the particular byte is the last byte of the packet, the EOP bit in the Control Register must be set before the last byte is written into the transmit FIFO. The EOP bit is cleared automatically when the data byte is written to the FIFO. After the transmission of the last byte in the packet, the frame check sequence (16 bits) is sent followed by a closing flag. If there is any more data in the transmit FIFO, another flag is transmitted followed by the new data. In case of no data in the FIFO, the transmitter assumes the selected link channel state. During the transmission of either the data or the frame check sequence, the Protocol Controller checks the transmitted information on a bit by bit basis and inserts a ZERO after every sequence of five consecutive ONEs.

Transmit FIFO Full:

When the Transmit FIFO is full, this state is indicated by the Transmit FIFO status bits in the FIFO Status Register. These bits do not change state for two bit periods after an access of the FIFO from either the serial port or the microprocessor port. The bit period is determined by the CKi signal frequency. If the bus cycle of the controlling microprocessor is much shorter than the bit period, the Transmit FIFO status bits may not be updated in time for the next microprocessor read of the FIFO Status Register.

To make sure that the microprocessor does not overwrite the Tx FIFO, if over four bytes of information have been written to the Tx FIFO, the

microprocessor should wait for a 4/19 FULL interrupt before writing to the Tx FIFO again. When a 4/19 FULL interrupt has been received, a maximum of 15 bytes should be written to the Tx FIFO, then transfer of information to the Tx FIFO should stop and the 4/19 FULL interrupt should be waited for once more. The FIFO may be allowed to empty if no more information is to be sent at the moment. This procedure should keep software independent of the frequency of the CKi signal.

Transmit Underrun:

A transmit underrun occurs when the last byte loaded into the transmit FIFO was not 'flagged' with the 'end of packet' (EOP) bit and there are no more bytes in the FIFO. In such a situation, the Protocol Controller transmits the abort sequence (eight ONEs) and moves to the selected link channel state.

Abort Transmission:

If it is desired to abort the packet currently being loaded into the transmit FIFO, the next byte written to the FIFO should be 'flagged' to cause this to happen. The FA bit of the Control Register must be set HIGH, before writing the next byte into the FIFO. This bit is cleared automatically once the byte is written to the FIFO. When the 'flagged' byte reaches the bottom of the FIFO, a frame abort sequence is sent instead of the byte and the transmitter operation returns to normal.

Go Ahead Transmission:

By setting the IFTF bits in the Control Register appropriately the transmitter can be made to send the Go Ahead sequences when the Protocol Controller is not sending the packets. Since the go ahead is defined as 011111110, contiguous $7F_{Hex}$' s appear as go aheads. As long as the IFTF bits are set to choose go aheads, the transmitter will send them even if data is subsequently loaded into the FIFO. Only when the IFTF bits are set to select something other than go aheads, will the data be transmitted.

C-Channel Transmission:

By setting the C1EN bit in the Timing Control Register HIGH, the information loaded in the C-Channel Control Register can be transmitted over channel-1 timeslot of the outgoing ST-BUS (CDSTo). This is available only during the Internal Timing Mode of the Protocol Controller.

Transparent Data Transfer:

The IFTF bits in the Control Register can be set to provide transparent data transfer disabling the protocol functions. The transmitter no longer generates the Flag, GA, Abort and Idle sequences nor does it insert the zeros and calculate the FCS . It operates in both timing modes in bytewide manner and transmits data serially on CDSTo. If the Protocol Controller is in the Internal Timing Mode and the Timing Control bits are set to select 2, 6 or 7 bits/frame, the corresponding least significant bits of every byte loaded into the transmit FIFO are only transmitted. The transparent data transfer facility is not available when the Timing Control bits are set for 1 bit/frame. In case the FIFO is empty, the last byte or the portion of the last byte, written to the FIFO is transmitted repeatedly. Note that the transparent data transfer can be disabled immediately in software (unlike during the transmission of packets) using TxEN bit in the Control Register.

The operation of the transmitter is similar in the External Timing Mode.

Receive Operation

After a reset on power up, the receive section is disabled. Timing set up considerations are similar to that of the transmit section. Address detection is also disabled when a reset occurs. If address detection is required, the Receiver Address Register is loaded with the desired address and the RxAD bit in the Control Register is set HIGH. The receive section can then be enabled by RxEN bit in the Control Register.

Normal Packets:

After initialization as explained above, the serial data starts to be clocked in and the receiver checks for the idle channel and flags. If an idle channel is detected, the 'Idle' bit in the General Status Register is set HIGH. Once a flag is detected, the receiver synchronizes itself in a bytewide manner to the incoming data stream. The receiver keeps resynchronizing to the flags until an incoming packet appears. The incoming packet is examined on a bit-by-bit basis, inserted zeros are deleted, the FCS is calculated and the data bytes are written into the receive FIFO. However, the FCS and other control characters like the flag, abort etc., never appear in the FIFO. If the address detection is enabled, the first byte following the flag is compared to the byte in the Receive Address Register and to All-Call address. If a match is not found, the entire packet is ignored and nothing is written to the FIFO. If the incoming address byte is valid, the packet is received in normal fashion. All the bytes written to the receive

FIFO are flagged with two status bits. The status bits are found in the FIFO status register and indicate whether the byte to be read from the FIFO is the first byte of the packet, the middle of the packet, the last byte of the packet with good FCS or the last byte of the packet with bad FCS. This status indication is valid for the byte to be read from the receive FIFO.

The incoming data is always written to the FIFO in a bytewide manner. However, in the event of data sent not being a multiple of eight bits, the software associated with the receiver should be able to pick the data bits from the MSB positions of the last byte in the received data written to the FIFO. The Protocol Controller does not provide any indication as to how many bits this might be.

Receive FIFO Empty:

When the Receive FIFO is empty, this state is indicated by the Receive FIFO status bits in the FIFO Status Register. As with the Tx FIFO status bits (see Transmit FIFO Full Section), these bits are not updated for two bit periods after any access of the Receive FIFO. If the controlling microprocessor's bus cycle is much shorter than a bit period on the serial port, then the status bits may not be updated to indicate there is no information left in the Rx FIFO before the microprocessor has returned to read the Rx FIFO again. The result is an underflow condition that is only evident by redundant bytes in the received message.

To avoid a Rx FIFO underflow, reading information from the Rx FIFO should be approached in two ways. The first approach is to be used when the MT8952B indicates (via interrupt) that the Rx FIFO is 15/19 FULL. The controlling microprocessor should then immediately read 14 bytes from the Rx FIFO. This will avoid emptying the FIFO. The second approach is to be used when an End of Packet interrupt is signalled by the MT8952B. The controlling microprocessor should then empty the Rx FIFO until the Rx Byte Status bits in the FIFO Status Register indicate that the byte about to be read is the last byte. These bits are "tag" bits whose state was determined before the End of Packet condition was indicated, therefore their state is valid.

Invalid Packets:

If there are less than 24 data bits between the opening and closing flags, the packet is considered invalid and the data never enters the receive FIFO. This is true even with data and the abort sequence, the total of which is less than 24 bits. The data packets that are at least 24 bits but less than 32 bits long are also invalid, but not ignored. They are clocked into the receive FIFO and tagged as having bad FCS.

Frame Abort:

When a frame abort is received the appropriate bits in the Interrupt Flag and Status Registers are set. The last byte of the packet that was aborted is written to the FIFO with a status of 'packet byte' tagged to it. The CPU determines which packet in the FIFO was aborted, if there is more than one packet in the FIFO, by the absence of 'last byte' status on any of the bytes.

Idle Channel:

While receiving the idle channel, the idle bit in the general status register remains set.

Go Ahead:

The occurrence of this sequence can be used to generate an interrupt as described earlier. The receive circuitry will not recognize a frame abort followed by a flag as go ahead.

C-Channel Reception:

The information contained in channel-1 of the incoming ST-BUS (CDSTi) is shifted into the C-Channel Status Register during the Internal Timing Mode.

Transparent Data Transfer:

By setting the IFTF bits in the Control Register to select the transparent data transfer, the receive section can be made to disable the protocol functions like Flag/Abort/GA/Idle detection, zero deletion, CRC calculation and address comparison. The received data is shifted in from CDSTi and written to receive FIFO in bytewide format. If the Protocol Controller is in the Internal Timing Mode and the Timing Control bits are set to 2, 6 or 7 bits/frame, the respective MSBs of each byte are only to be read from the data bus. The transparent data transfer facility is not available when the Timing Control bits are set to one bit/frame. The receive section can be disabled in software immediately using the RxEN bit in the Control Register.

The operation of the receiver is similar in the External Timing Mode.

Receive Overflow:

Receive overflow occurs when the receive section attempts to load a byte to an already full receive FIFO. This status can be used to generate the interrupt as described earlier.

Typical Connection

A typical connection to the HDLC Protocol Controller is shown in Figure 14. The parallel port interfaces with 6800/6809 type processors. The bits A0-A3 are the addresses of various registers in the Protocol Controller. The microprocessor can read and write to these registers treating them as memory locations.

The serial port transmits/receives the packetized data. It can be connected to a digital transmission medium or to a digital network interface circuit. The TEOP and REOP are the 'end of packet' signals on transmit and receive direction respectively. $\overline{F0i}$ and CKi are the timing signals with CKi accepting either the bit rate clock or 2 x bit rate clock in the internal timing mode. $\overline{TxCEN}$ and $\overline{RxCEN}$ are the enable inputs in the External Timing Mode.

$\overline{WD}$ is the output of the watchdog timer. It goes LOW when the timer times out or if the $\overline{RST}$ input is held LOW. This output can be used to reset the associated microprocessor. The $\overline{RST}$ is an active LOW input which resets the entire circuitry.

Applications

The MT8952B has a number of applications for transferring data or control information over a digital channel while providing built-in error detection capability. In combination with the MT8972 (the Digital Network Interface Circuit), it can be used to transmit digital data over a twisted wire pair.

The block schematic of one such application is shown in Figures 15 and 16. They refer to the primary and secondary ends of a voice/data communication link using the Digital Network Interface Circuits (DNIC). Each end is associated with one DNIC which interfaces twisted wire pair to the digital data rate up to 160kbps (2B+D, framing signal and housekeeping information).

Primary End of the Link:

The MT8952B is operating in the internal timing mode with the C-channel transceiver action enabled. The processor loads the data or control information (D Channel) in the transmit FIFO which is packetized in HDLC format and shifted out serially during the selected channels of the outgoing ST-BUS (CDSTo). The channels and the number of bits per frame (frame period=125µsec) can be selected by TC0-TC3 bits in the Timing Control Register. Since channel 1 is reserved for the C-channel information and channels 2 and 3 carry B-channels (64 kbps each), the D-channel information can only be sent on channel-0. Similarly the incoming packets on CDSTi are loaded into receive FIFO after the removal of all overhead bits and checked for any errors. The microprocessor will then read the data from the receive FIFO.

The DNIC (MT8972) is selected to operate in single port, master mode with the digital network (DN) option enabled. The B-channels, B1 and B2, are shown connected directly to the DNIC. Hence, these should be in ST-BUS format enabled at the appropriate timeslot (channels 2 and 3). It can be the outputs of voice codecs (MT896X) providing voice communication or data codecs (MT8950) for

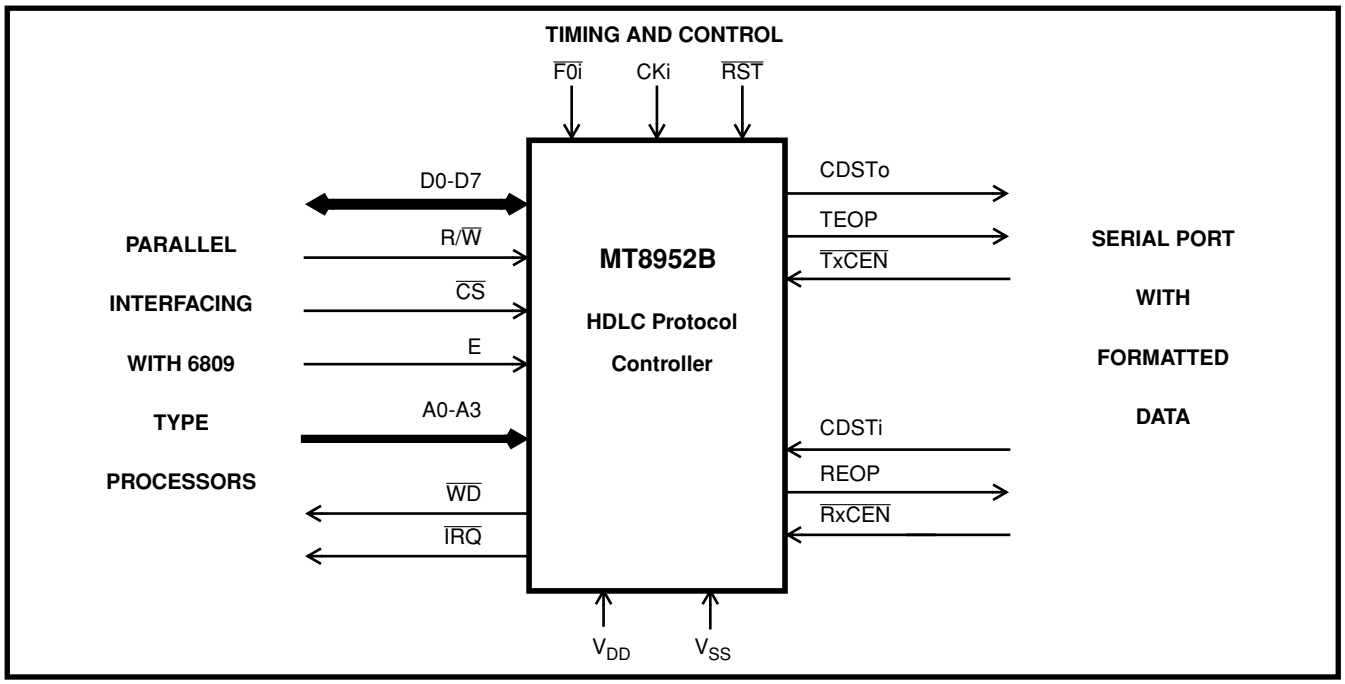


Figure 14 - Typical Connection Diagram

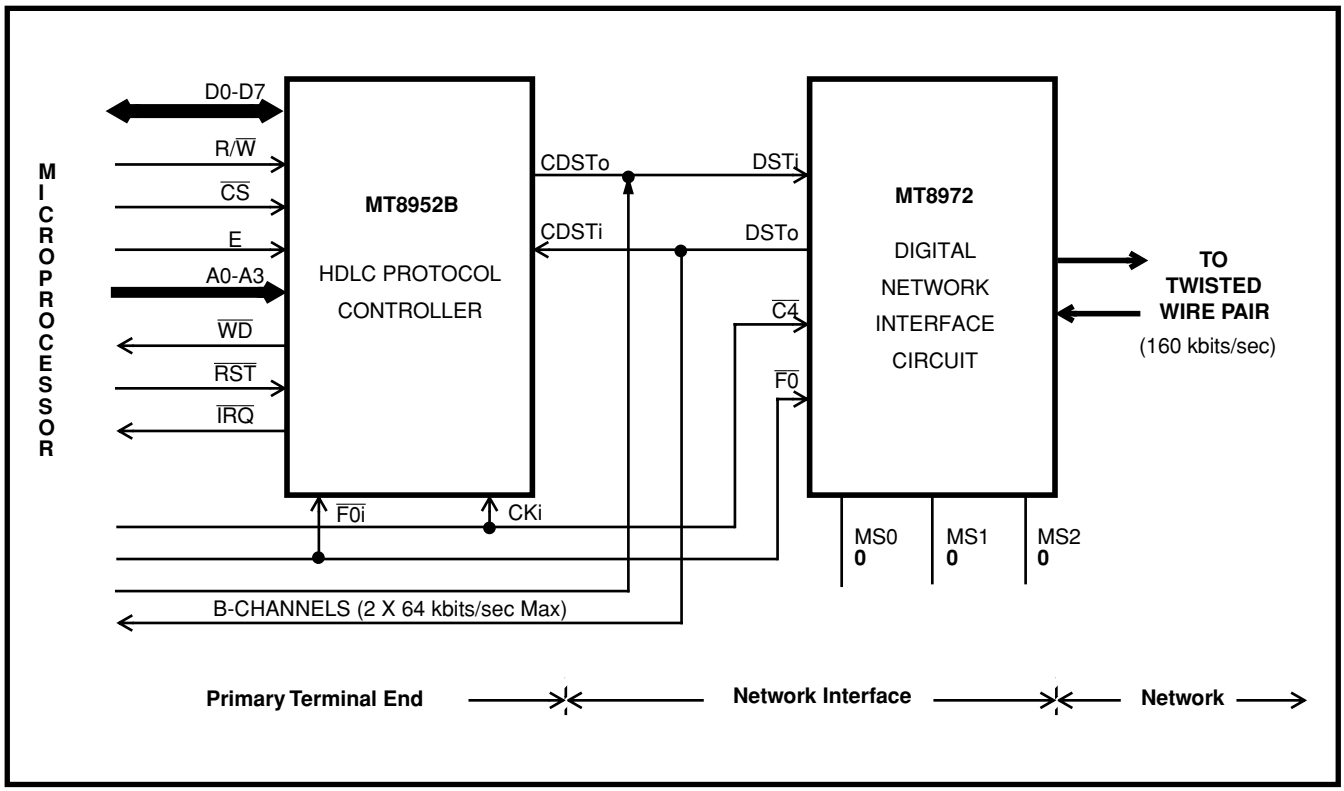


Figure 15 - HDLC Protocol Controller at the Primary End of the Link

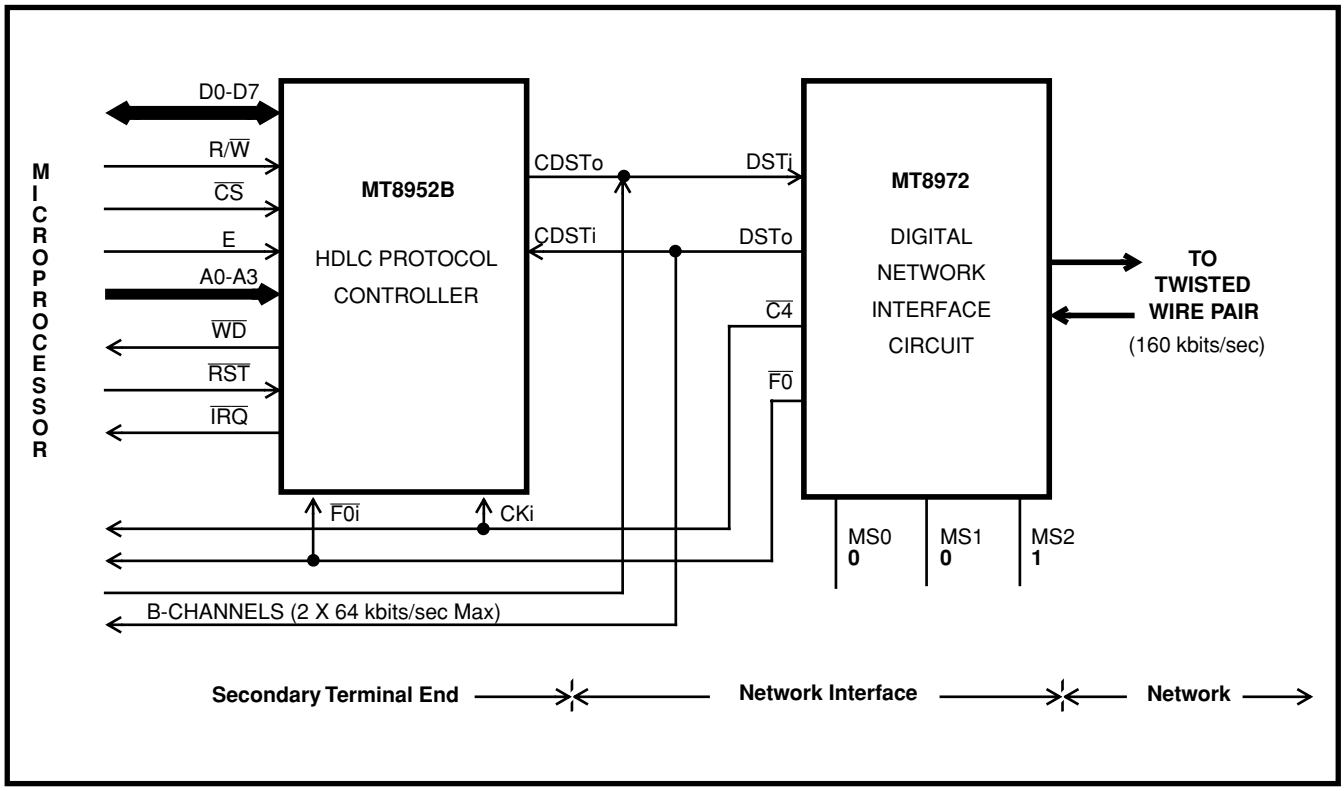


Figure 16 - HDLC Protocol Controller at the Secondary End of the Link

communication between RS232-C type terminals. It is possible to use the HDLC protocol on B1 and B2 channels to provide the error detection.

This can be done by using a separate MT8952B enabled appropriately to shift out the formatted data during channels 2 and 3 or by multiplexing the same MT8952B between B- and D- channels.

Secondary End of the Link:

At the secondary end of the communication link, a similar procedure is adopted to transmit/receive the data and control information.

The MT8952B operates in the Internal Timing Mode as at the primary end, but the DNIC (MT8972) is selected to operate in single port, slave mode with the digital network capability enabled.

The other functions and procedures are similar to those at the primary end.

The timing signals like CKi (C2i or $\overline{C4i}$) and $\overline{F0i}$ are provided externally at the primary end and at the secondary end, they are derived from the received data.

Although this application describes the communication between two stations over a dedicated link, it can be modified to serve a switched communication path by additional control functions and a call set-up procedure many of which can be achieved in software.

Absolute Maximum Ratings*

	Parameter	Symbol	Min	Max	Units
1	Supply voltage	V_{DD}	-0.3	7.0	V
2	Voltage on any pin (other than supply pins)	V_I	V_{SS}-0.3	V_{DD}+0.3	V
3	Current on any pin (other than supply pins)	I_I / I_O		±25	mA
4	DC Supply or ground current	I_{DD} / I_{SS}		±50	mA
5	Storage temperature	T_{ST}	-65	150	°C
6	Package power dissipation Plastic	P_D		0.6	W

* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Supply Voltage	V_{DD}	4.75	5.0	5.25	V	
2	Input HIGH voltage	V_{IH}	2.4		V_{DD}	V	For a Noise Margin of 400 mV
3	Input LOW voltage	V_{IL}	V_{SS}		0.4	V	For a Noise Margin of 400 mV
4	Frequency of operation	f_{CL}			5.0	MHz	When clock input is at twice the bit rate.
5	Operating temperature	T_A	-40	25	85	°C	

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

DC Electrical Characteristics - Voltages are with respect to ground (VSS) unless otherwise stated.

V_{DD}=5V±5%, V_{SS}=0V, T_A=-40 to 85°C.

		Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1		Supply Current (Quiescent)	I_{DD}		1	10	µA	Outputs unloaded and clock input (CKi) grounded
2		Supply current (Operational)	I_{DD}		0.4	1.0	mA	*See below
3	INPUT	Input HIGH voltage	V_{IH}	2.0			V	
4		Input LOW voltage	V_{IL}			0.8	V	
5		Input leakage current	I_{IZ}			10	µA	
6		Input capacitance	C_{in}		10		pF	
7		HIGH switching point for Schmitt Trigger ($\overline{RST}$) input	V_{T+}		4.0		V	
8		LOW switching point for Schmitt Trigger ($\overline{RST}$) input	V_{T-}		1.0		V	
9		Hysteresis on Schmitt Trigger ($\overline{RST}$) input	V_H		0.5		V	
10	OUTPUT	Output HIGH current (on all the outputs except $\overline{IRQ}$)	I_{OH}	-5	-16		mA	V_{OH}=2.4 V
11		Output LOW current (on all the outputs including $\overline{IRQ}$)	I_{OL}	5	10		mA	V_{OL}=0.4 V
12		Output capacitance	C_o		15		pF	

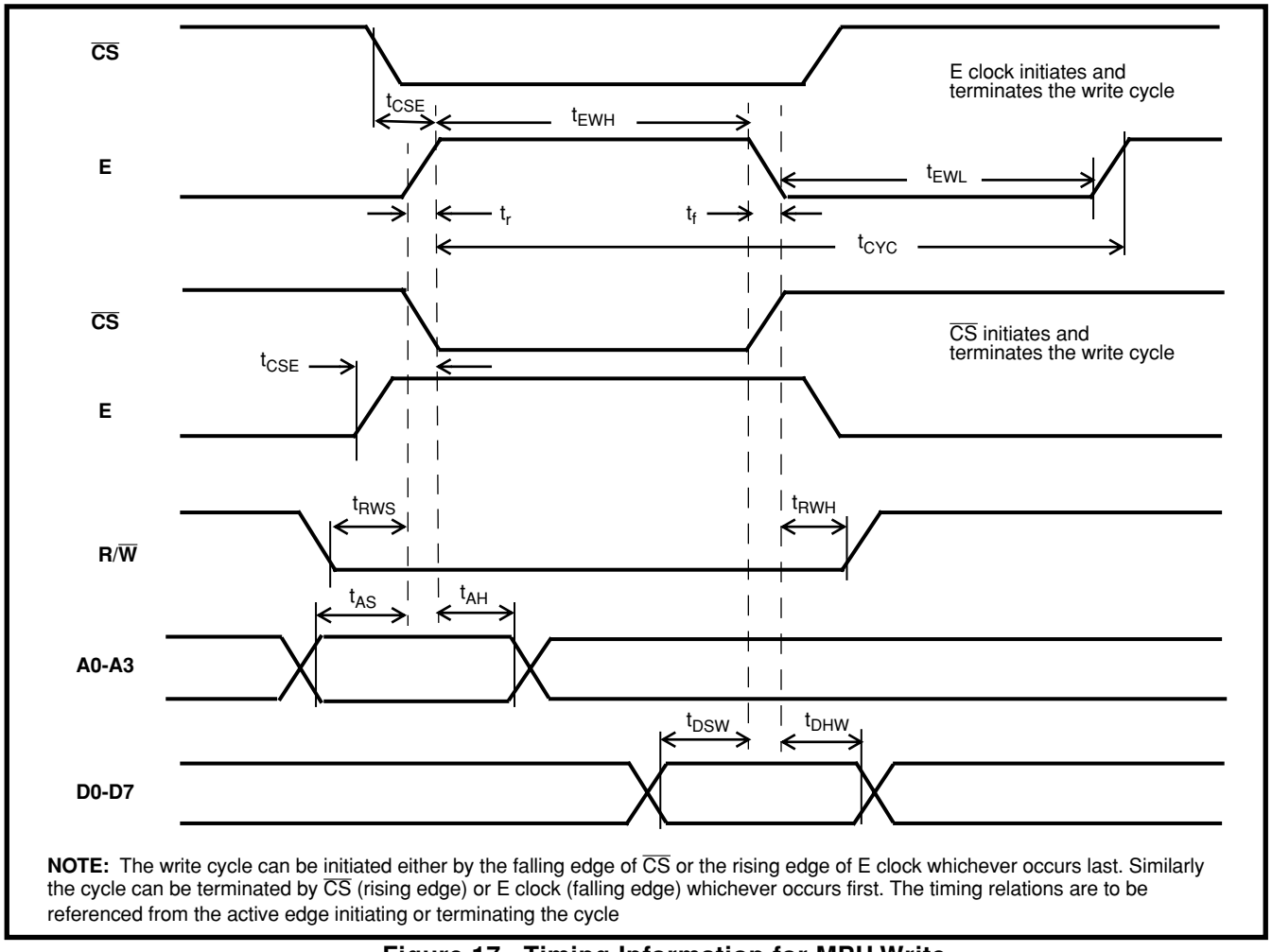
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.
* Outputs unloaded. Input pins 12 and 25 clocked at 2048 kHz. All other inputs at V_{SS}.

AC Electrical Characteristics† - Microprocessor Interface - (Figures 17 and 18)

Voltages are with respect to ground (V_{SS}) unless otherwise stated.

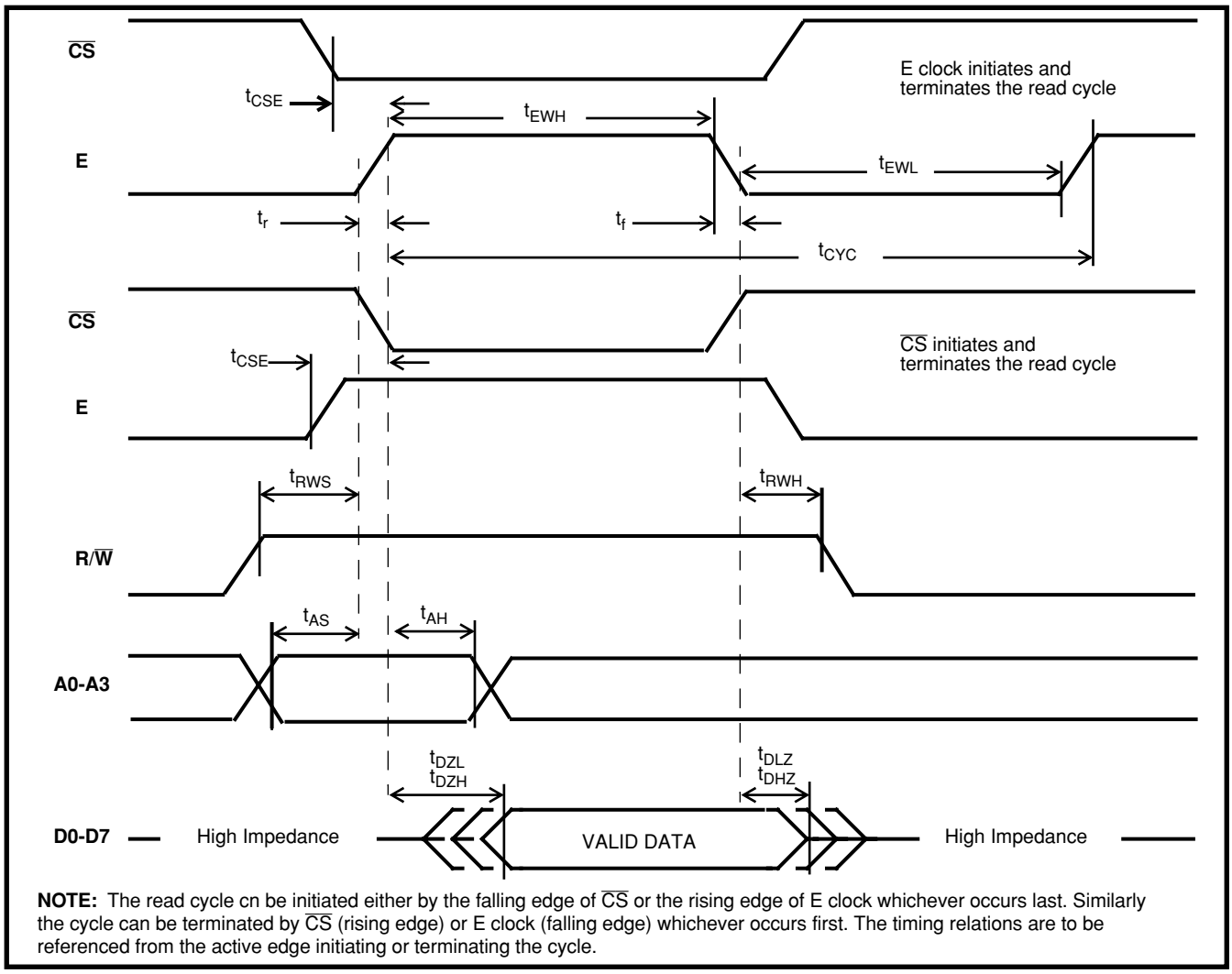
	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Delay between $\overline{CS}$ and E clock	t_{CSE}	0			ns	
2	Cycle time	t_{CYC}	205			ns	
3	E Clock pulse width HIGH	t_{EWH}	145			ns	
4	E Clock pulse width LOW	t_{EWL}	60			ns	
5	Read/Write setup time	t_{RWS}	20			ns	
6	Read/Write hold time	t_{RWH}	10			ns	
7	Address setup time	t_{AS}	20			ns	
8	Address hold time	t_{AH}	60			ns	
9	Data setup time (write)	t_{DSW}	35			ns	
10	Data hold time (write)	t_{DHW}	10			ns	
11	E clock to valid data delay	t_{DZL} t_{DZH}			145	ns	Test load circuit 1 (Fig. 26) C_L=200pF
12	Data hold time (read)	t_{DLZ} t_{DHZ}	10		60	ns	Test load circuit 3 (Fig. 26)

† Timing is over recommended temperature & power supply voltages (V_{DD}=5V±5%, V_{SS}=0V, T_A=–40 to 85°C).
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.



NOTE: The write cycle can be initiated either by the falling edge of $\overline{CS}$ or the rising edge of E clock whichever occurs last. Similarly the cycle can be terminated by $\overline{CS}$ (rising edge) or E clock (falling edge) whichever occurs first. The timing relations are to be referenced from the active edge initiating or terminating the cycle

Figure 17 - Timing Information for MPU Write



NOTE: The read cycle cn be initiated either by the falling edge of $\overline{CS}$ or the rising edge of E clock whichever occurs last. Similarly the cycle can be terminated by $\overline{CS}$ (rising edge) or E clock (falling edge) whichever occurs first. The timing relations are to be referenced from the active edge initiating or terminating the cycle.

Figure 18 - Timing Information for MPU Read

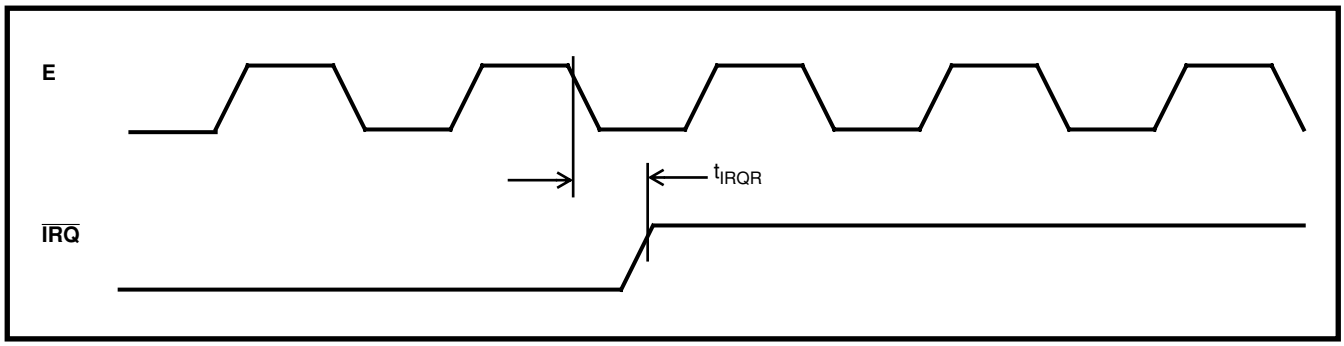


Figure 19 - Interrupt Request Release Time

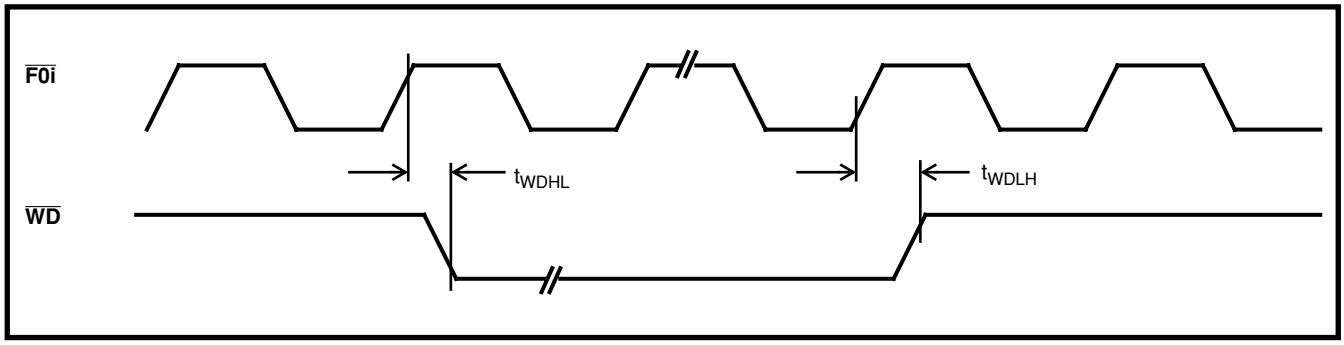


Figure 20 - Watchdog Timer Input and Output

AC Electrical Characteristics† - Serial Port, RESET, WD Timer and IRQ Release Time

(Figures 19, 20, 21 and 22). Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Interrupt request release time	t_{IRQR}			120	ns	Test load circuit 2 (Fig.26)
2	$\overline{WD}$ output delay HIGH to LOW	t_{WDHL}			135	ns	Test load circuit 1 (Fig.26)
3	$\overline{WD}$ output delay LOW to HIGH	t_{WDLH}			135	ns	Test load circuit 1 (Fig.26)
4	TEOP/REOP output delay	t_{EOPD}			110	ns	Test load circuit 1 (Fig.26)
5	TEOP/REOP output hold time	t_{EOPH}			110	ns	Test load circuit 1 (Fig.26)
6	CDSTo delay from CKi	t_{STOD}			125	ns	Test load circuit 1 (Fig.26)
7	CDSTi setup time	t_{STiS}	20			ns	
8	CDSTi hold time	t_{STiH}	65			ns	
9	RESET pulse width	t_{RST}		100		ns	

† Timing is over recommended temperature & power supply voltages (V_{DD}=5V±5%, V_{SS}=0V, T_A=–40 to 85°C).
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

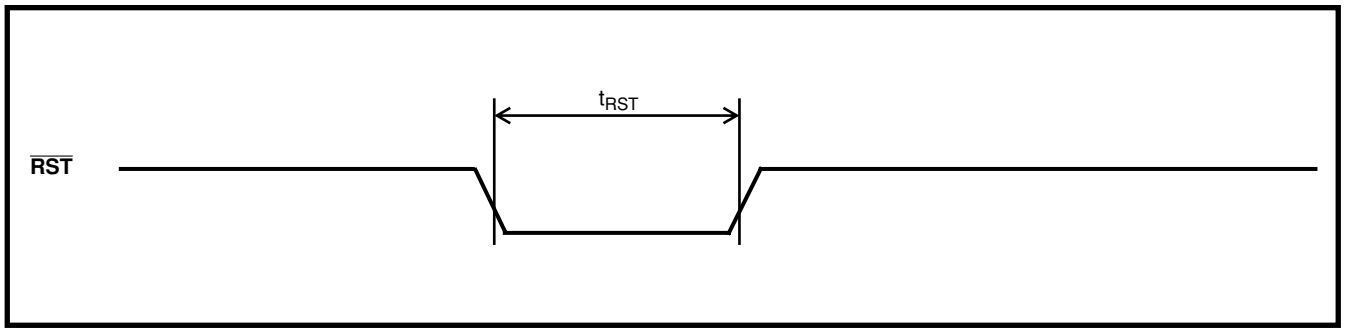


Figure 21 - RESET Timing

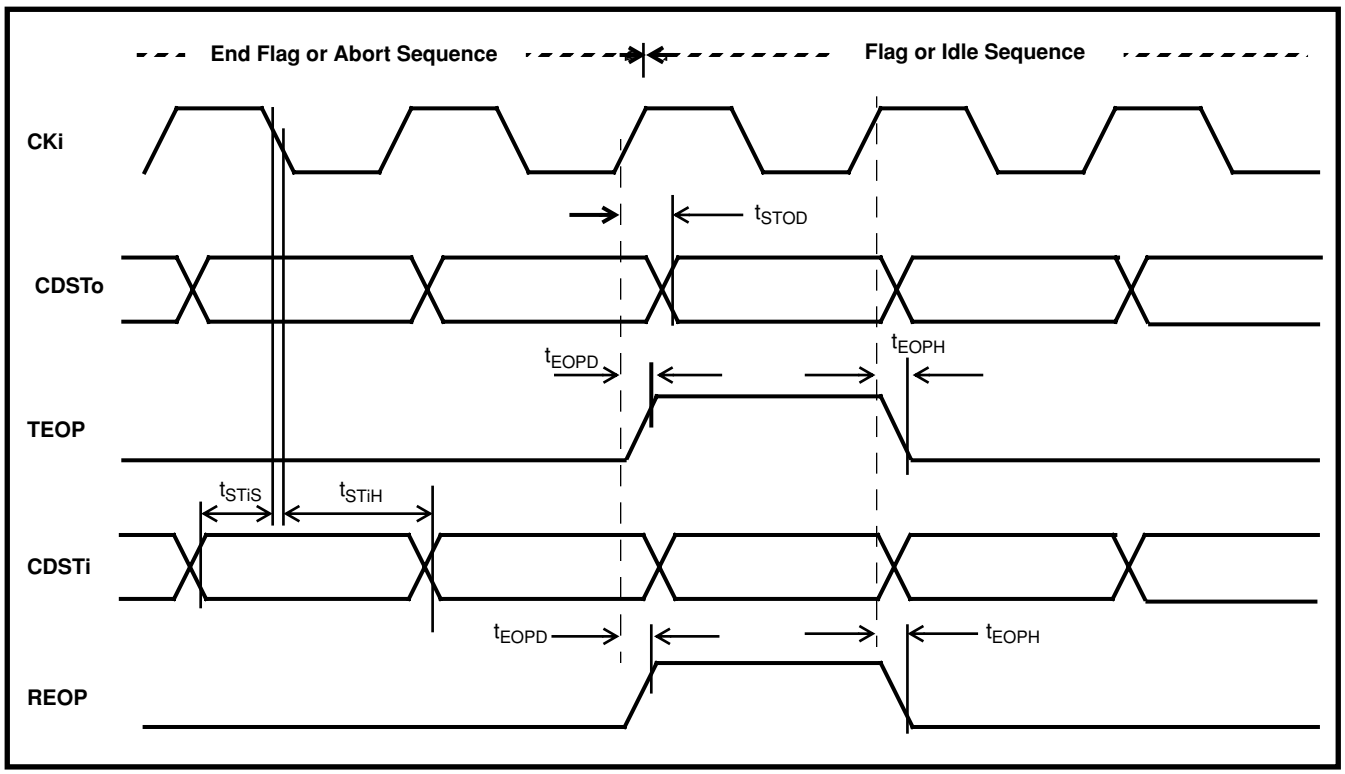


Figure 22 - Serial Port Input and REOP, Output and TEOP

Note: The frequency of the clock input CKi is assumed to be at the output bit rate. However, it can be at twice the bit rate in the Internal Timing Mode.

AC Electrical Characteristics† - Serial Port in External Timing Mode - (Figure 23)

Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Clock period on CKi pin	t_{CEX}	400			ns	
2	CKi transition time	t_T		20		ns	
3	$\overline{TxCEN}/\overline{RxCEN}$ setup time	t_{CENS}	60			ns	
4	$\overline{TxCEN}/\overline{RxCEN}$ hold time	t_{CENH}	40			ns	
5	CDSTi setup time	t_{STiS}	20			ns	
6	CDSTi hold time	t_{STiH}	65			ns	
7	CDSTo delay	t_{SToZL} t_{SToZH}			125	ns	Test load circuit 1 (Fig. 26) C_L=150pF
8	CDSTo disable time	t_{SToLZ} t_{SToHZ}			85	ns	Test load circuit 3 (Fig. 26)

† Timing is over recommended temperature & power supply voltages (V_{DD}=5V±5%, V_{SS}=0V, T_A=–40 to 85°C).
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

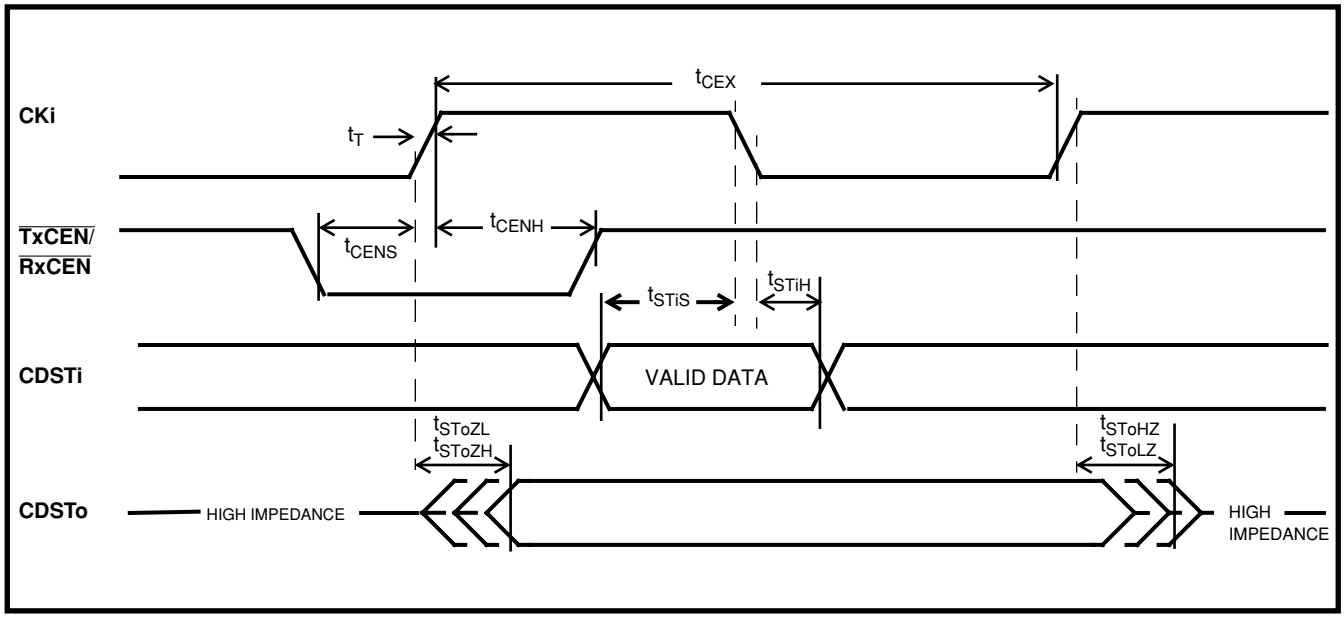


Figure 23 - Serial Port Inputs and Outputs in External Timing Mode

Note: The frequency of the clock input (CKi) should be at the output bit rate in the External Timing Mode.

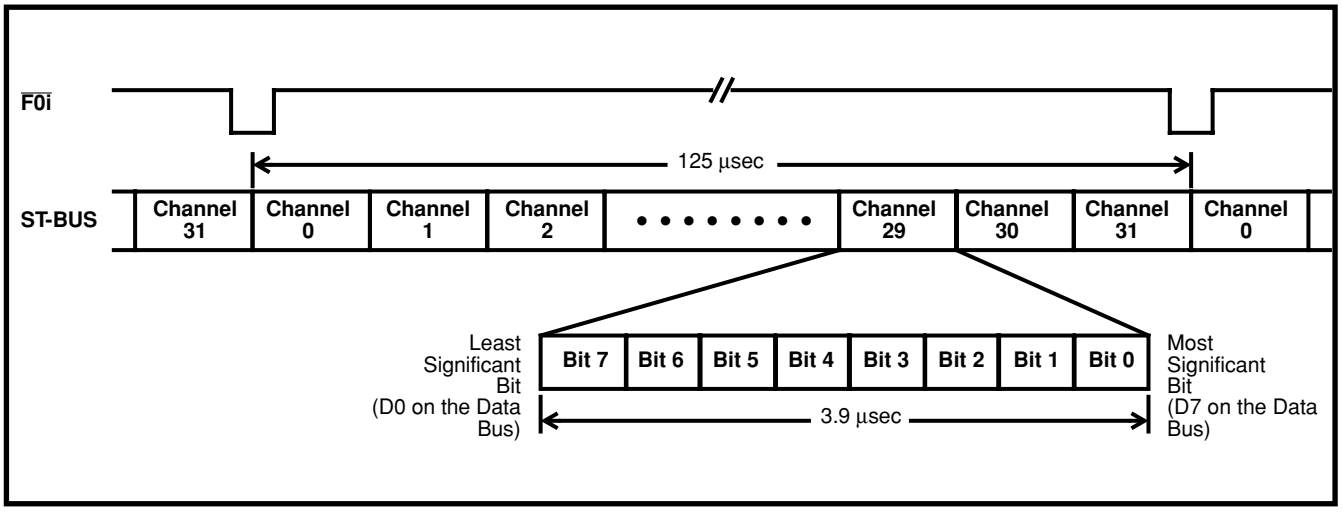


Figure 24 - ST-BUS Format

AC Electrical Characteristics† - Serial Port in Internal Timing Mode - (Figure 25)

Voltages are with respect to ground (V_{SS}) unless otherwise stated .

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Frame Pulse ($\overline{F0i}$) width	t_{F0iW}	50			ns	
2	Frame Pulse ($\overline{F0i}$) setup time	t_{F0iS}	30			ns	See note 3.
3	Frame Pulse ($\overline{F0i}$) hold time	t_{F0iH}	20			ns	See note 3.
4	CDSTo delay from clock input	t_{SToZL} t_{SToZH}			125	ns	Test load circuit 1 (Fig. 26)
5	CDSTi setup time	t_{STiS}	20			ns	
6	CDSTi hold time	t_{STiH}	65			ns	
7	C2i clock period	t_{C2i}	400			ns	
8	$\overline{C4i}$ clock period	t_{C4i}	200			ns	

† Timing is over recommended temperature & power supply voltages (V_{DD}=5V±5%, V_{SS}=0V, T_A=–40 to 85°C).
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

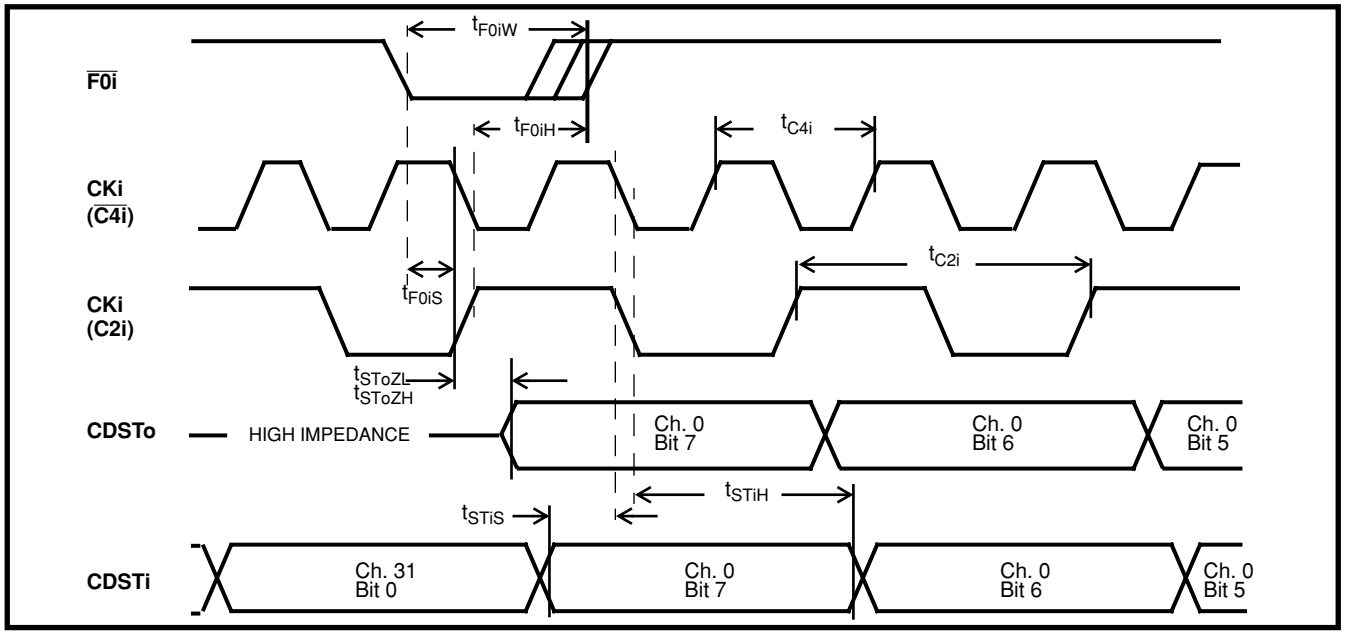


Figure 25 - Serial Port Input and Output in ST-BUS Format (Internal Timing Mode)

Note: 1. Channels 0 to 4 can only be active on CDSTi and CDSTo in the Internal Timing Mode.
2. Clock input CKi can be either of the ST-BUS clocks C2i (2.048MHz) or $\overline{C4i}$ (4.096 MHz) in the Internal Timing Mode.
3. The Frame Pulse set up and hold time measurements are to be referenced from the falling edge of $\overline{C4i}$ or the rising edge of C2i depending on the clock selected.

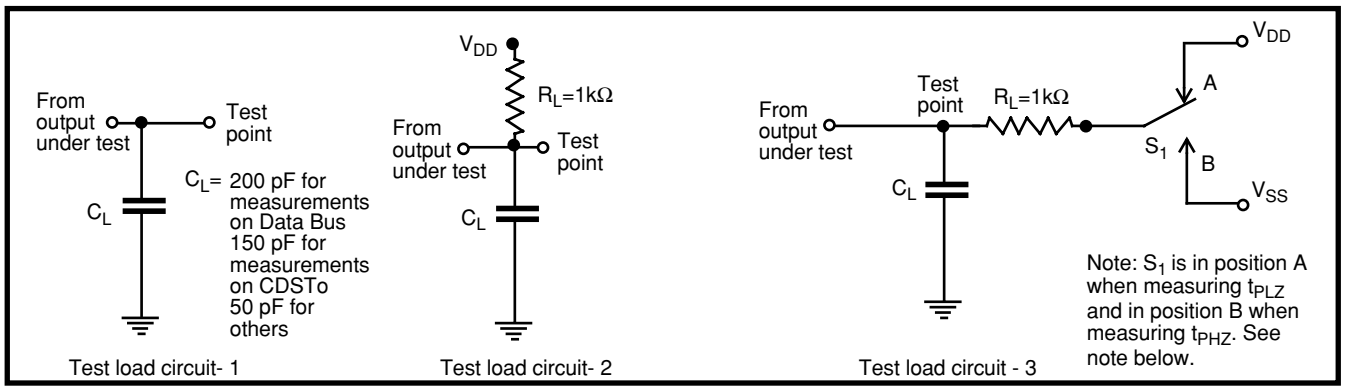
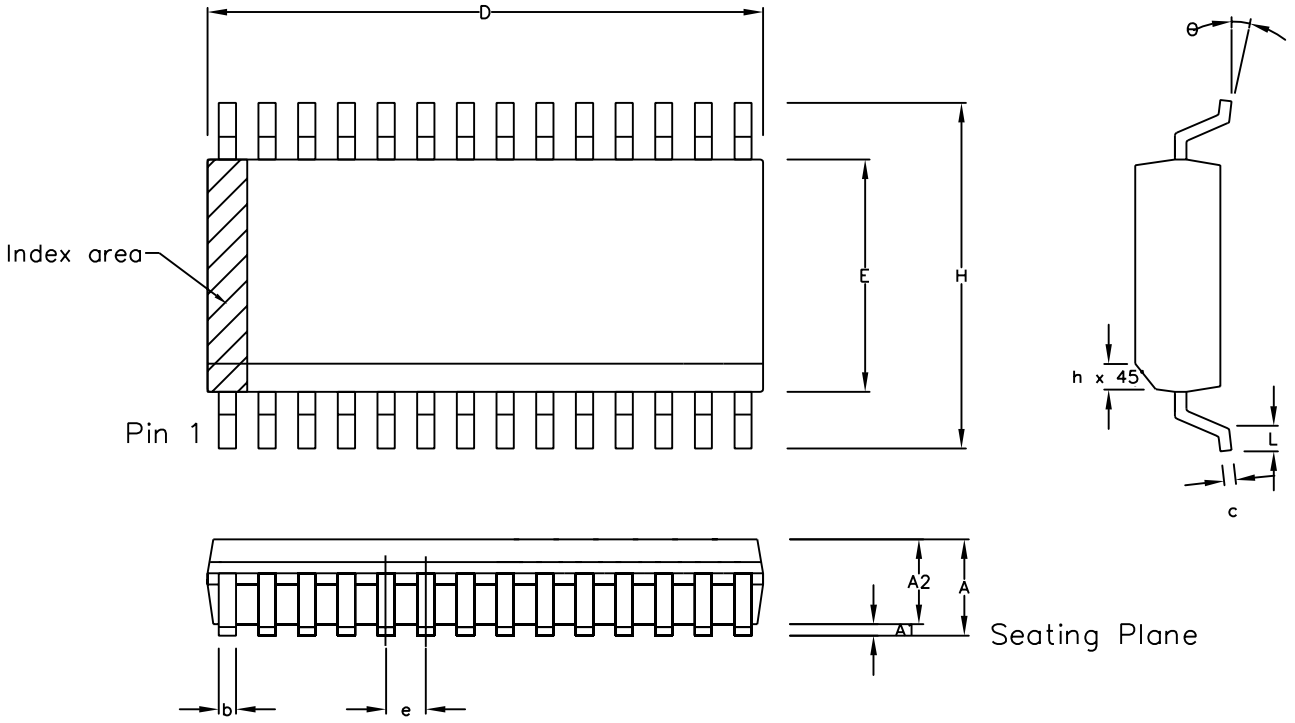


Figure 26 - Test Load Circuits

Note: Active Low to High impedance times are measured from the disabling signal edge to the time when V_{out} has increased by 0.5 volts. Active High to High impedance times are measured from the disabling signal edge to the time when V_{out} has decreased by 0.5 volts.



Symbol	Control Dimensions in millimetres				Altern. Dimensions in inches		
	MIN	Nominal	MAX		MIN	Nominal	MAX
A	2.35		2.65		0.093		0.104
A1	0.10		0.30		0.004		0.012
A2	2.25		2.35		0.089		0.092
D	17.70		18.10		0.697		0.713
H	10.00		10.65		0.394		0.419
E	7.40		7.60		0.291		0.299
L	0.40		1.27		0.016		0.050
e	1.27 BSC.				0.050 BSC.		
b	0.33		0.51		0.013		0.020
c	0.23		0.32		0.009		0.013
θ	0°		8°		0°		8°
h	0.25		0.75		0.010		0.029
	Pin features						
N	28						
Conforms to JEDEC MS-013AE Iss. C							

Notes:
1. The chamfer on the body is optional. If it not present, a visual index feature, e.g. a dot, must be located within the cross-hatched area.
2. Controlling dimension are in millimeters.
3. Dimension D do not include mould flash, protrusion or gate burrs. These shall not exceed 0.006" per side.
4. Dimension E1 do not include inter-lead flash or protrusion. These shall not exceed 0.010" per side.
5. Dimension b does not include dambar protrusion/intrusion. Allowable dambar protrusion shall be 0.004" total in excess of b dimension.

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ZARLINK SEMICONDUCTOR

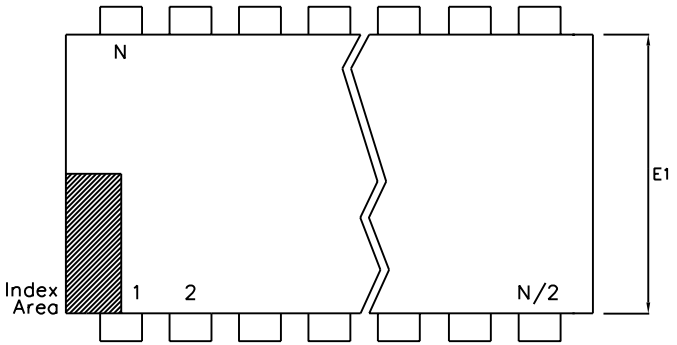
Previous package codes

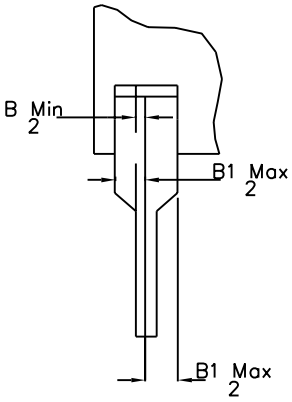
MP / S

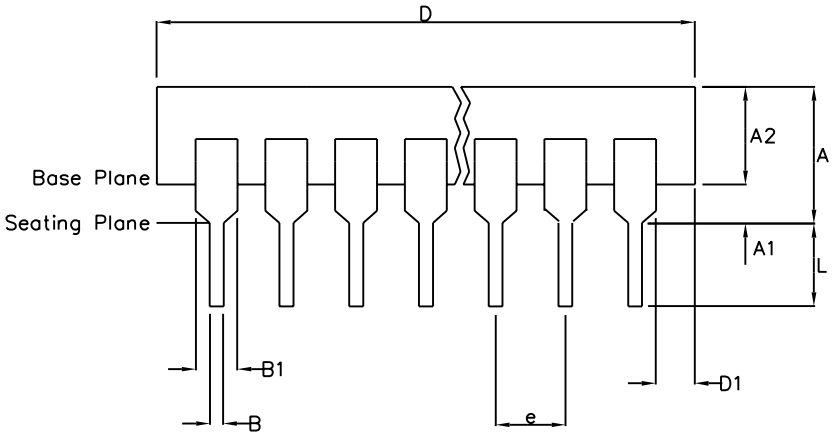
Package Code DC

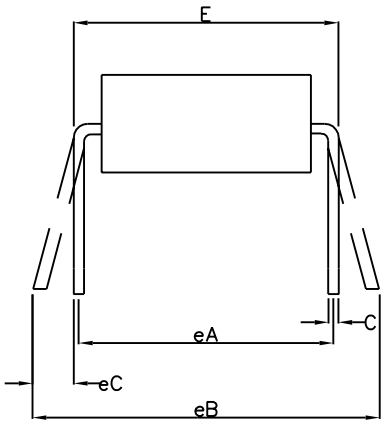
Package Outline for
28 lead SOIC
(0.300" Body Width)

GPD00017









	Min mm	Max mm	Min Inches	Max Inches
A		6.35		0.250
A1	0.38		0.015	
A2	3.18	4.95	0.125	0.195
B	0.36	0.56	0.014	0.022
B1	0.76	1.78	0.030	0.070
C	0.20	0.38	0.008	0.015
D	35.05	39.75	1.380	1.565
D1	0.13		0.005	
E	15.24	15.88	0.600	0.625
E1	12.32	14.73	0.485	0.580
e	2.54 BSC		0.100 BSC	
eA	15.24 BSC		0.600 BSC	
eB		17.78		0.700
L	2.92	5.08	0.115	0.200
N	28		28	
Conforms to Jedec MS-011AB ISS.B				

Notes:
1. Controlling Dimensions are in inches
2. Dimension A, A1 and L are measured with the package seated in the Seating Plane
3. Dimensions D & E1 do not include mould flash or protrusions. Mould flash or protrusion shall not exceed 0.010 inch.
4. Dimensions E & eA are measured with leads constrained to be perpendicular to plane T.
5. Dimensions eB & eC are measured at the lead tips with the leads unconstrained; eC must be zero or greater.

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ZARLINK SEMICONDUCTOR

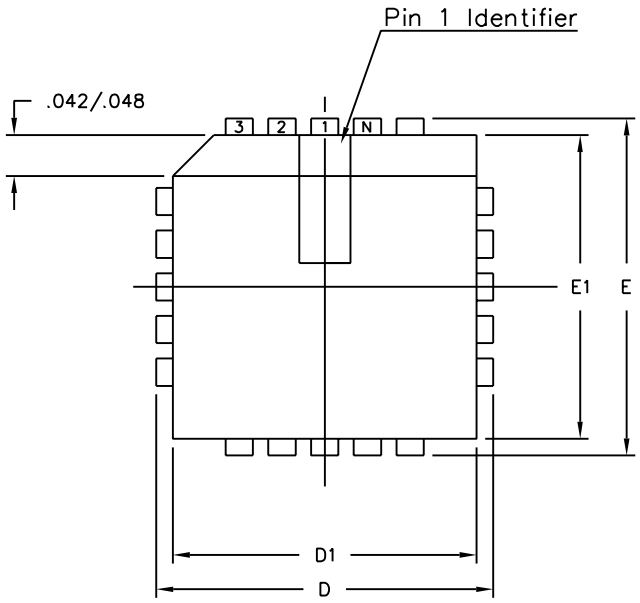
Previous package codes

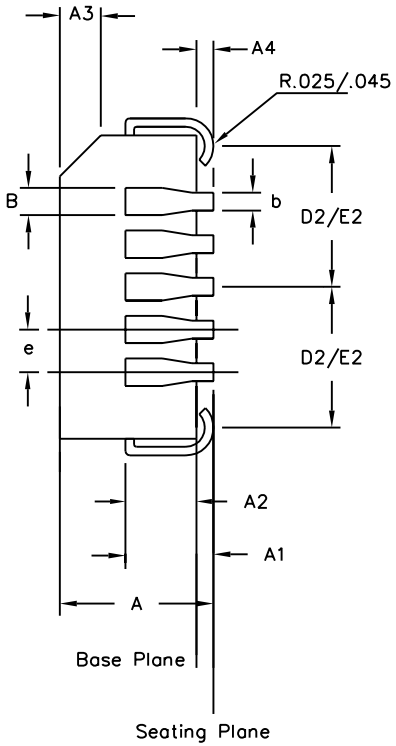
DP / E

Package Code DA

Package Outline for
28 lead PDIP

GPD00072





Symbol	Control Dimensions in inches		Altern. Dimensions in millimetres	
	MIN	MAX	MIN	MAX
A	0.165	0.180	4.19	4.57
A1	0.090	0.120	2.29	3.05
A2	0.062	0.083	1.57	2.11
A3	0.042	0.056	1.07	1.42
A4	0.020	–	0.51	–
D	0.485	0.495	12.32	12.57
D1	0.450	0.456	11.43	11.58
D2	0.191	0.219	4.85	5.56
E	0.485	0.495	12.32	12.57
E1	0.450	0.456	11.43	11.58
E2	0.191	0.219	4.85	5.56
B	0.026	0.032	0.66	0.81
b	0.013	0.021	0.33	0.53
e	0.050 BSC		1.27 BSC	
	Pin features			
ND	7			
NE	7			
N	28			
Note	Square			
Conforms to JEDEC MS-018AB Iss. A				

Notes:
1. All dimensions and tolerances conform to ANSI Y14.5M–1982
2. Dimensions D1 and E1 do not include mould protrusions. Allowable mould protrusion is 0.010" per side. Dimensions D1 and E1 include mould protrusion mismatch and are determined at the parting line, that is D1 and E1 are measured at the extreme material condition at the upper or lower parting line.
3. Controlling dimensions in Inches.
4. "N" is the number of terminals.
5. Not To Scale
6. Dimension R required for 120° minimum bend.

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ZARLINK SEMICONDUCTOR

Previous package codes

HP / P

Package Code QA

Package Outline for 28 lead PLCC

GPD00002

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