TDF8551J

I²C-bus controlled 4 × 45 W power amplifier with six voltage regulators

Rev. 02 — 18 August 2009 Product data sheet

1. General description

1.1 Amplifiers

The TDF8551J has a complementary quad audio power amplifier that uses BCDMOS technology. It contains four amplifiers configured in Bridge-Tied Load (BTL) to drive four speakers: two front and two rear channels. The I²C-bus enables diagnostic information of each amplifier and its speaker to be read separately. Both front and both rear channel amplifiers can be configured independently in line driver mode with a gain of 20 dB (differential output) or amplifier mode with a gain of 26 dB (BTL output).

1.2 Voltage regulators and switches

The TDF8551J has six output voltage regulators and two power switches:

- Four switchable regulators and two standby regulators
- Two power switches with loss-of-ground protection and surge protection
- Second supply pin to reduce dissipation by means of an external DC-to-DC converter
- Backup functionality for regulator 2

2. Features

- Amplifiers
  - I²C-bus control
  - Can drive a 2 Ω load with a battery voltage of up to 16 V and a 4 Ω load with a battery voltage of up to 18 V
  - DC load detection: open, short and present
  - AC load (tweeter) detection
  - Programmable clip detect; 1 % or 3 %
  - Programmable thermal protection pre-warning
  - Independent short-circuit protection for each channel
  - Selectable line driver (20 dB) and amplifier mode (26 dB)
  - Loss-of-ground and open V_P safe
  - All outputs protected from short-circuit to ground, to V_P or across the load
  - All pins protected from short-circuit to ground
  - Soft thermal-clipping to prevent audio holes
  - Low battery detection
- Voltage regulators and switches
  - I²C-bus control

- Good stability for any regulator with almost any output capacitor value
- Six voltage regulators (microcontroller, display, audio processor, tuner, bus, mechanical digital and drive)
- Selectable output voltages for regulators 1, 4 and 5
- Low dropout voltage PNP output stages
- High supply voltage ripple rejection
- Low noise for all regulators
- Two power switches (antenna switch and amplifier switch)
- Standby regulators 2 and 6 (microcontroller and bus supply) operational during load dump and thermal shutdown
- Low standby quiescent current (regulators 2 and 6 operational only)
- Second supply pin for connecting optional external DC-to-DC converter to reduce internal dissipation
- Backup functionality for regulator 2

■ Protection

- If connection to the battery voltage is reversed, all regulator voltages will be zero
- Withstands output voltages up to 18 V (supply line may be short-circuited)
- Thermal protection to avoid thermal breakdown
- Load dump protection
- Regulator outputs protected from DC short-circuit to ground or to supply voltage
- All regulators protected by foldback current limiting
- Power switches protected from loss-of-ground and surge conditions

3. Applications

■ Boost amplifier and voltage regulator for car radios and CD/MD players

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Amplifiers							
$V_{P(oper)}$	operating supply voltage	R_L = 4 Ω	[1]	8	14.4	18	V
$I_{q(tot)}$	total quiescent current	no load		-	280	400	mA
$P_{o(max)}$	maximum output power	R_L = 4 Ω; V_P = 14.4 V; V_{IN} = 2 V RMS square wave		39	41	-	W
		R_L = 4 Ω; V_P = 15.2 V; V_{IN} = 2 V RMS square wave		44	46	-	W
		R_L = 2 Ω; V_P = 14.4 V; V_{IN} = 2 V RMS square wave		64	69	-	W
THD	total harmonic distortion	P_o = 1 W to 12 W; f = 1 kHz; R_L = 4 Ω		-	0.01	0.1	%
$V_{n(o)}$	output noise voltage	filter 20 Hz to 22 kHz; R_s = 600 Ω					
		line driver mode		-	25	35	μV
		amplifier mode		-	50	70	μV

Table 1. Quick reference data *…continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Voltage regulators						
V_P	supply voltage	regulators 1, 3, 4 and 5 on; switches 1 and 2 on	10	14.4	18	V
		jump starts for t ≤ 10 minutes	-	-	30	V
		load dump protection for t ≤ 50 ms and t_r ≥ 2.5 ms	-	-	50	V
$V_{th(dis)}$	disable threshold voltage	regulator 1, 3, 4 and 5 on; switches 1 and 2 on	18.1	22	-	V
V_{DCDC}	DC-to-DC converter voltage		4.75	5.0	V_P	V
$I_{q(tot)}$	total quiescent current	Standby mode; V_P = 14.4 V	-	180	250	µA
$V_{O(reg)}$	regulator output voltage	regulator 1; 0.5 mA ≤ I_O ≤ 400 mA; 10 V ≤ V_P ≤ 18 V				
		IB2[D3:D2] = 01	7.9	8.3	8.7	V
		IB2[D3:D2] = 10	8.1	8.6	9.1	V
		IB2[D3:D2] = 11	4.75	5.0	5.25	V
		regulator 2; 0.5 mA ≤ I_O ≤ 350 mA; 10 V ≤ V_P ≤ 18 V	3.1	3.3	3.5	V
		regulator 3; 0.5 mA ≤ I_O ≤ 525 mA; 5 V ≤ V_{DCDC} ≤ 18 V	3.1	3.3	3.5	V
		regulator 4; 0.5 mA ≤ I_O ≤ 800 mA; 10 V ≤ V_P ≤ 18 V				
		IB2[D7:D5] = 001	4.75	5.0	5.25	V
		IB2[D7:D5] = 010	5.7	6.0	6.3	V
		IB2[D7:D5] = 011	6.6	7.0	7.4	V
		IB2[D7:D5] = 100	8.1	8.6	9.1	V
		IB2[D7:D5] = 101	7.6	8.0	8.4	V
		regulator 5; 0.5 mA ≤ I_O ≤ 400 mA				
		10 V ≤ V_P ≤ 18 V; IB1[D7:D4] = 0001	5.7	6.0	6.3	V
		10 V ≤ V_P ≤ 18 V; IB1[D7:D4] = 0010	6.65	7.0	7.37	V
		10 V ≤ V_P ≤ 18 V; IB1[D7:D4] = 0011	7.8	8.2	8.6	V
		10.5 V ≤ V_P ≤ 18 V; IB1[D7:D4] = 0100	8.55	9.0	9.45	V
		11 V ≤ V_P ≤ 18 V; IB1[D7:D4] = 0101	9.0	9.5	10.0	V
		11.5 V ≤ V_P ≤ 18 V; IB1[D7:D4] = 0110	9.5	10.0	10.5	V
		13 V ≤ V_P ≤ 18 V; IB1[D7:D4] = 0111	9.9	10.4	10.9	V
		14.2 V ≤ V_P ≤ 18 V; IB1[D7:D4] = 1000	11.8	12.5	13.2	V
		12.5 V ≤ V_P ≤ 18 V; IB1[D7:D4] = 1001	V_P – 1	V_P – 0.5	-	V
		10 V ≤ V_P ≤ 18 V; IB1[D7:D4] = 1010	4.75	5.0	5.25	V
		10 V ≤ V_P ≤ 18 V; IB1[D7:D4] = 1011	3.1	3.3	3.5	V
		regulator 6; 0.5 mA ≤ I_O ≤ 100 mA; 10 V ≤ V_P ≤ 18 V	4.75	5.0	5.25	V
Power switches						
V_{do}	dropout voltage	switch 1; I_O = 400 mA	-	0.6	1.1	V
		switch 2; I_O = 400 mA	-	0.6	1.1	V

[1] voltage on pin V_{p1} and/or pin V_{p2}

5. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
TDF8551J	DBS37P	plastic DIL-bent-SIL power package; 37 leads (lead length 6.8 mm)	SOT725-1

6. Block diagram

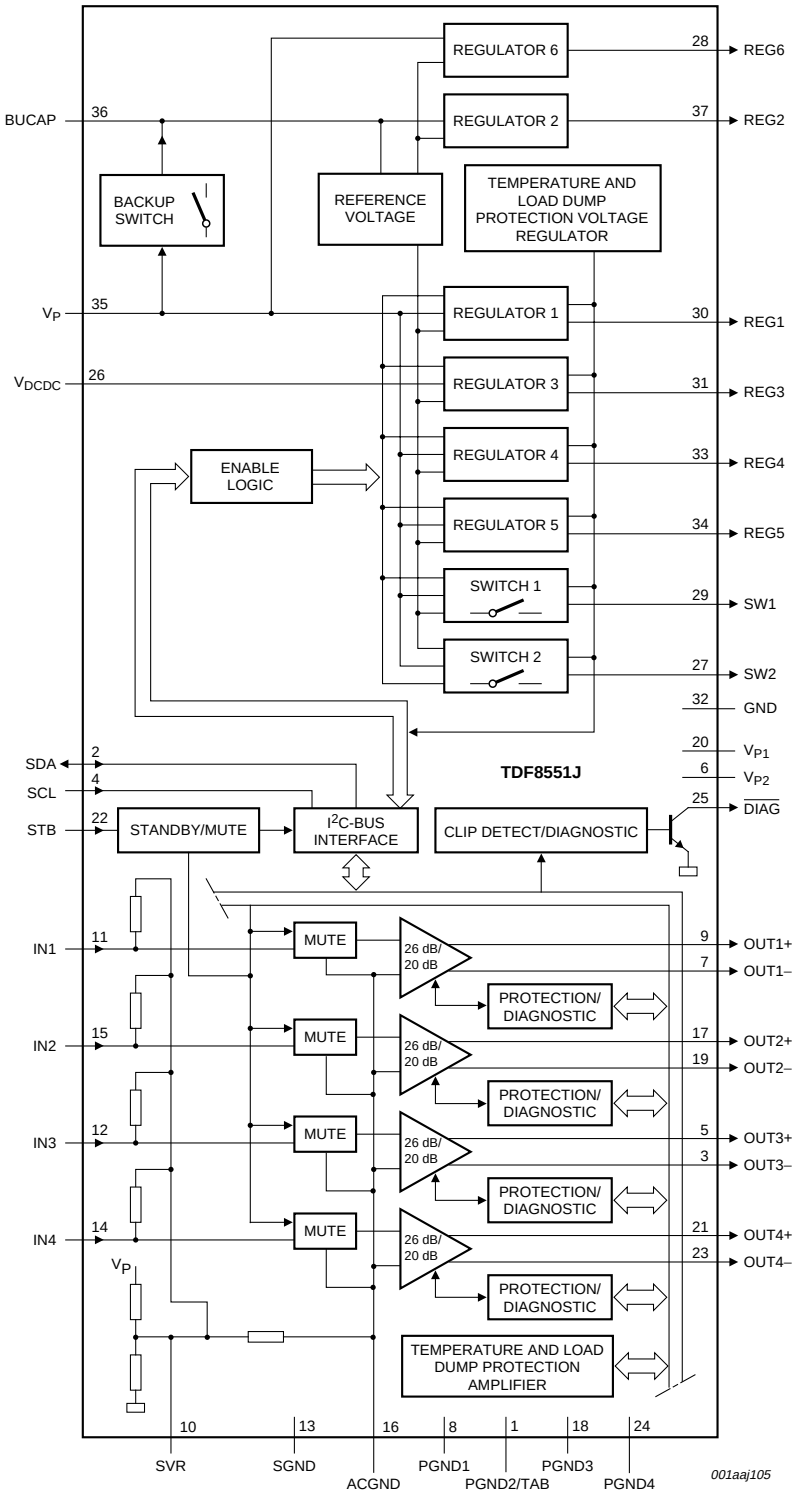


Fig 1. Block diagram

7. Pinning information

7.1 Pinning

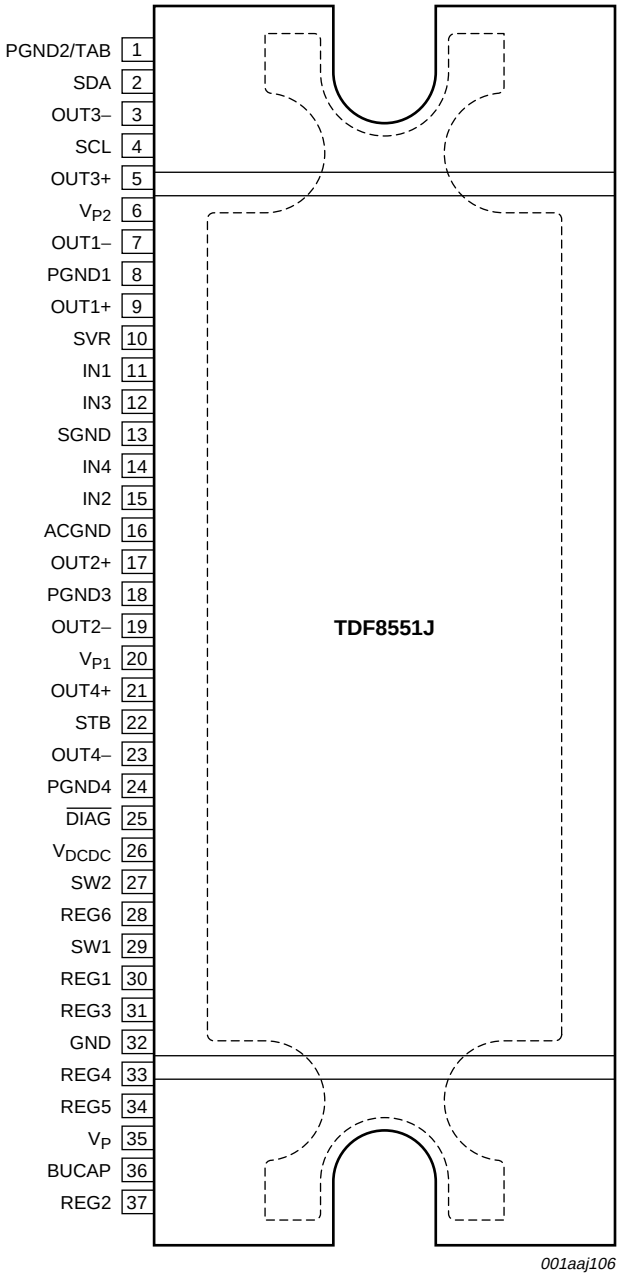


Fig 2. Pin configuration

7.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
PGND2/TAB	1	power ground 2 and connection for heatsink
SDA	2	I^2C-bus data input and output
OUT3–	3	channel 3 negative output
SCL	4	I^2C-bus clock input
OUT3+	5	channel 3 positive output
V_{P2}	6	power supply voltage 2 to amplifiers
OUT1–	7	channel 1 negative output
PGND1	8	power ground 1
OUT1+	9	channel 1 positive output
SVR	10	half supply voltage filter capacitor
IN1	11	channel 1 input
IN3	12	channel 3 input
SGND	13	signal ground
IN4	14	channel 4 input
IN2	15	channel 2 input
ACGND	16	AC ground
OUT2+	17	channel 2 positive output
PGND3	18	power ground 3
OUT2–	19	channel 2 negative output
V_{P1}	20	power supply voltage 1 to amplifiers
OUT4+	21	channel 4 positive output
STB	22	standby, operating or mute mode select input
OUT4–	23	channel 4 negative output
PGND4	24	power ground 4
$\overline{DIAG}$	25	diagnostic and clip detection output, active-LOW
V_{DCDC}	26	power supply voltage from optional DC-to-DC converter
SW2	27	antenna switch; supplies unregulated power to car aerial motor
REG6	28	regulator 6 output; supply for bus controller
SW1	29	amplifier switch; supplies unregulated power to amplifiers
REG1	30	regulator 1 output; supply for audio part of radio and CD player
REG3	31	regulator 3 output; supply for signal processor part (mechanical digital) of CD player
GND	32	combined voltage regulator, power and signal ground
REG4	33	regulator 4 output; supply for mechanical part (mechanical drive) of CD player
REG5	34	regulator 5 output; supply for display part of radio and CD player
V_P	35	power supply to voltage regulators
BUCAP	36	connection for backup capacitor
REG2	37	regulator 2 output; supply voltage to microcontroller

8. Functional description

The TDF8551J is an IC which provides six voltage regulators in combination with four independent, BTL configured, power amplifiers and diagnostic capabilities. All regulator output voltages except regulators 2 and 6 can be controlled via the I²C-bus.

The amplifier diagnostic functions give information about output offset, load, or short-circuit. The diagnostic functions are controlled using the I²C-bus. The TDF8551J is protected against short-circuit, overtemperature, open ground and open V_P connections. If a short-circuit occurs at the output of a single amplifier, that channel shuts down and the other channels continue to operate normally. The short-circuited channel can be switched off by the microcontroller using the appropriate enable bit of the I²C-bus to prevent any noise generated by the fault condition from being heard.

8.1 Start-up

At power on, regulators 2 and 6 reach their final voltage when the backup capacitor voltage exceeds 5.5 V, independently of the voltage on pin STB. When pin STB is LOW, the total quiescent current is low and the I²C-bus lines are high-impedance.

When pin STB is HIGH, the I²C-bus is biased on and the TDF8551J performs a power-on reset. When bit IB1[D0] is set, the amplifier is activated, DB2[D7] (power-on reset occurred) is reset and pin $\overline{\text{DIAG}}$ is no longer held LOW.

8.2 Start-up and shutdown timing

See Figure 12.

A capacitor connected to pin SVR enables smooth start-up and shutdown, preventing the amplifier from producing audible clicks at switch-on or switch-off. The start-up and shutdown times can be extended by increasing the capacitor value.

If the amplifier is shutdown using pin STB, it is muted, the regulators and switches are switched off, and the capacitor connected to pin SVR discharges. The low-current Standby mode is activated 2 seconds after pin STB goes LOW.

8.3 Power-on reset and supply voltage spikes

See Figure 13 and Figure 14.

If the supply voltage drops too low to guarantee the integrity of the data in the I²C-bus latches, the power-on reset cycle will start. All latches will be set to a predefined state, pin $\overline{\text{DIAG}}$ will be pulled LOW to indicate that a power-on reset has occurred, and bit DB2[D7] is also set for the same reason. When IB1[D0] is set, the power-on flag resets, pin $\overline{\text{DIAG}}$ is released and the amplifier enters its start-up cycle.

8.4 Diagnostic output

Pin $\overline{\text{DIAG}}$ indicates clipping, thermal protection pre-warning of amplifier and voltage regulator parts, short-circuit protection and low and high battery voltage. Pin $\overline{\text{DIAG}}$ is an active-LOW, open-drain output which must be connected to an external voltage using an external pull-up resistor. If a failure occurs, pin $\overline{\text{DIAG}}$ remains LOW during the failure and no clipping information is available. The microcontroller can read the failure information using the I²C-bus.

8.5 Amplifiers

8.5.1 Muting

Both a hard mute and a soft mute can be performed using the I²C-bus. A hard mute mutes the amplifier within 0.5 ms. A soft mute mutes the amplifier within 20 ms and is less audible. A hard mute is also activated if a voltage of 8 V is applied to pin STB.

8.5.2 Temperature protection

If the average junction temperature rises to the temperature trigger value that has been set using the I²C-bus, a thermal protection pre-warning is activated making pin $\overline{\text{DIAG}}$ LOW. If the temperature continues to rise, all four channels are muted to reduce the output power (soft thermal clipping). However, the value at which the temperature mute control activates is fixed; only the temperature at which the thermal protection pre-warning signal occurs can be specified by bit IB3[D4].

If applying the temperature mute control does not reduce the average junction temperature, all the power stages will be switched off (muted) at the absolute maximum temperature $T_{j(max)}$.

8.5.3 Offset detection

Offset detection can only be performed when there is no input signal to the amplifiers, for instance when the external digital signal processor is muted after a start-up. The output voltage of each channel is measured and compared with a reference voltage. If the output voltage of a channel is greater than the reference voltage, bit D2 of the associated data byte is set and read by the microcontroller during a read instruction. Note that the value of this bit is only meaningful when there is no input signal and the amplifier is not muted. Offset detection is always enabled.

8.5.4 Speaker protection

If one side of a speaker is connected to ground, the missing current protection is triggered to prevent damage to the speaker. A fault condition is detected in a channel when there is a mismatch between the power current in the high-side and the power current in the low-side; during a fault condition the channel will be switched off.

The load status of each channel can be read using the I²C-bus: short to ground (one side of the speaker connected to ground), short to V_P (one side of the speaker connected to V_P) and shorted load.

8.5.5 Line driver mode

An amplifier can be used as a line-driver by switching it to low-gain mode. In normal mode, the gain between single-ended input and differential output (across the load) is 26 dB. In low-gain mode the gain between single-ended input and differential output is 20 dB.

8.5.6 Input and AC ground capacitor values

The negative inputs to all four amplifier channels are combined at pin ACGND. To obtain the best performance of supply voltage ripple rejection and unwanted audible noise, the value of the capacitor connected to pin ACGND must be as close as possible to 4 times the value of the input capacitor connected to the positive input of each channel.

8.5.7 Load detection

8.5.7.1 DC load detection

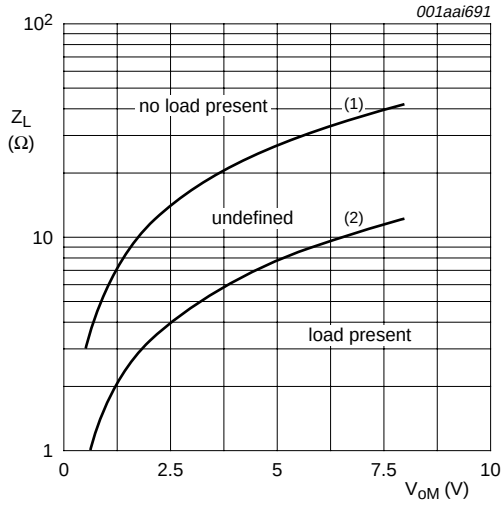
When DC load detection is enabled, during the start-up cycle, a DC-offset is applied slowly to the amplifier outputs and the output currents are measured. If the output current of an amplifier rises above a certain level, it is assumed that there is a load of less than 6 Ω and bit D5 is reset in the associated data byte register to indicate that a load is detected.

The offset is measured during the amplifier start-up cycle which means detection is inaudible and can be performed every time the amplifier is switched on.

8.5.7.2 AC load detection

AC load detection can be used to detect that AC-coupled speakers are connected correctly during assembly. This requires at least 3 periods of a 19 kHz sine wave to be applied to the amplifier inputs. The amplifier produces a peak output voltage which also generates a peak output current through the AC-coupled speaker. The 19 kHz sine wave is also audible during the test. If the amplifier detects three current peaks that are greater than 550 mA, the AC load detection bit is set. Three current peaks are counted to avoid false AC load detection which can occur if the input signal is switched on and off. The peak current counter can be reset by setting bit IB1[D1] to logic 0. To guarantee AC load detection, an amplifier current of more than 550 mA is required. AC load detection never occurs with a current of less than 150 mA.

Figure 3 shows which AC loads are detected at different output voltages. For example, if a load is detected at an output voltage of 2.5 V peak, the load is less than 4 Ω. If no load is detected, the output impedance is more than 14 Ω.



(1) I_{oM} = < 150 mA.

(2) I_{oM} = > 550 mA.

Fig 3. Tolerance of AC load detection as a function of output voltage

8.5.7.3 Load detection procedure

1. At start-up, enable the AC or DC load detection by setting bit IB1[D1] to logic 1.
2. After 250 ms the DC load is detected and the mute is released. This is inaudible and can be implemented each time the IC is powered on.
3. When the amplifier start-up cycle is completed (after 1.5 s), apply an AC signal to the input, and DC load bits D5 of each data byte should be read and stored by the microcontroller.
4. After at least 3 periods of the input signal, the load status can be checked by reading AC detect bits D4 of each data byte.

   The AC load peak current counter can be reset by setting bit IB1[D1] to logic 0 and then to logic 1. Note that this will also reset the DC load detection bits D5 in each data byte.

8.5.8 Low headroom protection

The normal DC output voltage of the amplifier is set to half the supply voltage and is related to the voltage on pin SVR. An external capacitor is connected to pin SVR to suppress power supply ripple. If the supply voltage drops (at vehicle engine start), the DC output voltage will follow slowly due to the affect of the SVR capacitor.

The headroom voltage is the voltage required for correct operation of the amplifier and is defined as the voltage difference between the level of the DC output voltage before the V_P voltage drop and the level of V_P after the voltage drop (see Figure 4).

At a certain supply voltage drop, the headroom voltage will be insufficient for correct operation of the amplifier. To prevent unwanted audible noises at the output, the headroom protection mode will be activated (see Figure 4). This protection discharges the capacitors connected to pins SVR and ACGND to increase the headroom voltage.

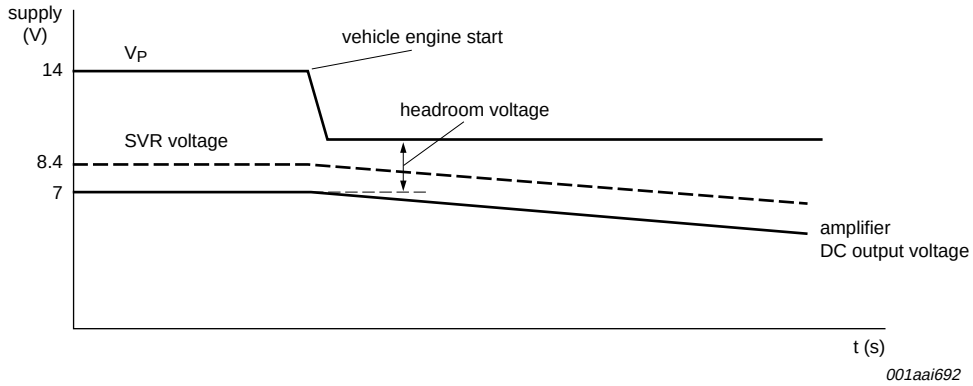


Fig 4. Amplifier output during supply voltage drop

8.6 Voltage regulators and switches

The TDF8551J has six output voltage regulators and two power switches:

- Four switchable regulators and two standby regulators
- Two power switches with loss-of-ground protection and surge protection

- Second supply pin to reduce dissipation by means of an external DC-to-DC converter
- Backup functionality for regulator 2

The TDF8551J uses low dropout voltage regulators for use in low voltage applications. All of the voltage regulators except for the standby regulators can be controlled using the I^2C-bus.

The TDF8551J also has two power switches which can deliver unregulated continuous current and several fail-safe protection modes.

It conforms to peak transient tests and protects against continuous high voltage (24 V), short-circuits and thermal stress. Standby regulators 2 and 6 will try to maintain output for as long as possible even if a thermal shutdown or any other fault condition occurs. During overvoltage stress conditions, all outputs except regulators 2 and 6 will switch-off and the device will be able to supply a minimum current for an indefinite amount of time sufficient for powering the memory of a microcontroller and bus controller functionality. Provision is made for an external reserve supply capacitor to be connected to pin BUCAP which can store enough energy to allow regulator 2 to supply a microcontroller for a period long enough for it to prepare for a loss-of-voltage.

8.6.1 Standby regulator outputs

Standby outputs (regulators 2 and 6) are used for the microcontroller and bus controller supply. These regulators will not shutdown with the switched regulators and cannot be controlled by the I^2C-bus. The standby regulators will not shutdown during load dump transients or by high temperature protection.

8.6.2 Backup capacitor

A backup capacitor (C_{backup}) is used as a backup supply for the regulator 2 output when the battery supply voltage (V_P) cannot support the regulator 2 voltage.

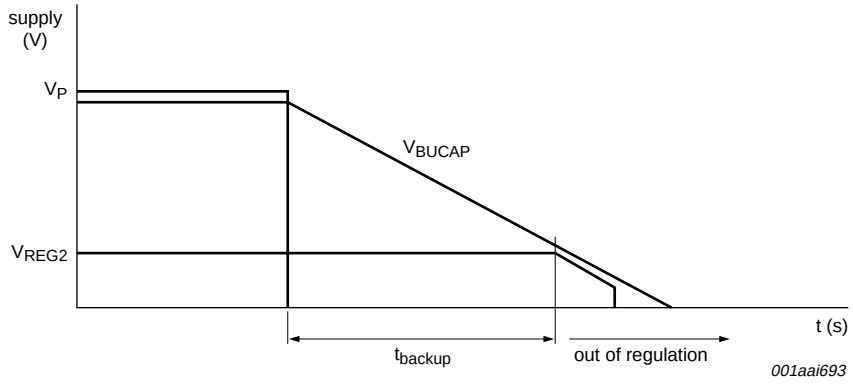
8.6.3 Backup function

The backup function is implemented by a switch function, which behaves like an ideal diode between pins V_P and BUCAP; the forward voltage of this ideal diode depends on the current flowing through it. The backup function supplies regulator 2 during brief periods when no supply voltage is present on pin V_P. It requires an external capacitor to be connected to pin BUCAP and ground. When the supply voltage is present on pin V_P this capacitor will be charged to a level of V_P – 0.3 V. When the supply voltage is absent from pin V_P, this charge can then be used to supply regulator 2 for a brief period (t_{backup}) calculated using the formula:

$$t_{backup} = C_{backup} \times R_L \times \left(\frac{V_P - (V_{REG2} - 0.5)}{V_{REG2}} \right) \quad (1)$$

Example: V_P = 14.4 V, V_{REG2} (voltage on pin REG2) = 3.3 V, R_L = 1 kΩ and C_{backup} = 100 µF provides a t_{backup} of 321 ms.

When an overvoltage condition occurs, the voltage on pin BUCAP is limited to approximately 24 V; see Figure 5.



$$t_{backup} = C_{backup} \times \left(\frac{V_P - (V_{REG2} - 0.5)}{I_{load}} \right)$$

Fig 5. Backup capacitor function

8.6.4 Power switches

There are two power switches that provide an unregulated DC voltage output for amplifiers and an aerial motor respectively. The switches have internal protection for overtemperature conditions and are activated by setting bits IB1[D2] and IB1[D3] to logic 1.

In the ON state, the switches have a low impedance to the battery voltage. When the battery voltage is higher than 22 V, the switches are switched off. When the battery voltage is below 22 V the switches are set to their original condition.

The power switches have built-in surge protection to be able to absorb energy from switching inductive or capacitive external loads. This surge protection is implemented in such a way that in case no supply (V_P) is present the supply line will not be charged from a possible external source connected to a power switch output.

8.6.5 External DC-to-DC converter

The V_{DCDC} supply pin can be connected to an external DC-to-DC down converter ($V_O \geq 5$ V) to reduce the dissipation in regulator 3. If no external DC-to-DC converter is used, the V_{DCDC} pin must be connected to V_P.

8.6.6 Protection

All regulator and switch outputs are fully protected by foldback current limiting against load dumps and short-circuits; see Figure 6. During a load dump all regulator outputs, except the output of regulators 2 and 6, will go low.

The power switches can withstand ‘loss-of-ground’. This means that if pin GND becomes disconnected, the switch is protected by automatically connecting its outputs to ground.

8.6.7 Temperature protection

If the junction temperature of a regulator becomes too high, the amplifier(s) are switched off to prevent unwanted noise signals being audible. A regulator junction temperature that is too high is indicated by pin $\overline{DIAG}$ going LOW and is also indicated by setting bit DB2[D6].

If the junction temperature of the regulator continues to rise and reaches the maximum temperature protection level, all regulators and switches will be disabled except regulators 2 and 6.

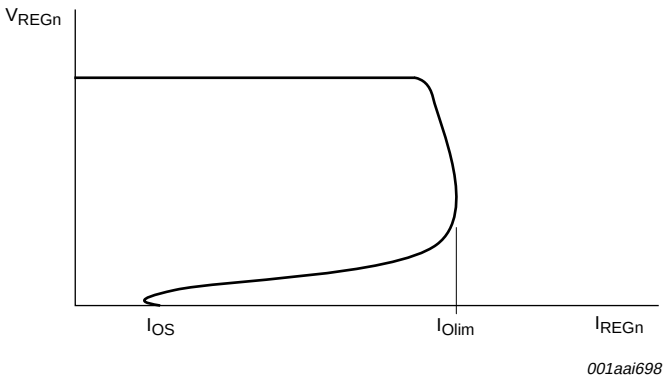


Fig 6. Foldback current protection

8.7 I²C-bus specification

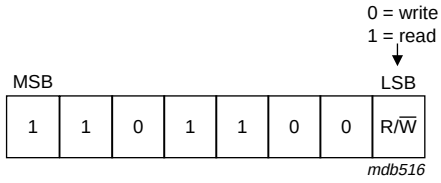


Fig 7. Address byte

If address byte bit R/$\overline{W}$ = 0, the TDF8551J expects three instruction bytes: IB1, IB2 and IB3; see Table 1 to Table 6.

After a power-on, all instruction bits are set to zero.

If address byte bit R/$\overline{W}$ = 1, the TDF8551J will send four data bytes to the microcontroller: DB1, DB2, DB3 and DB4; see Table 7 to Table 10.

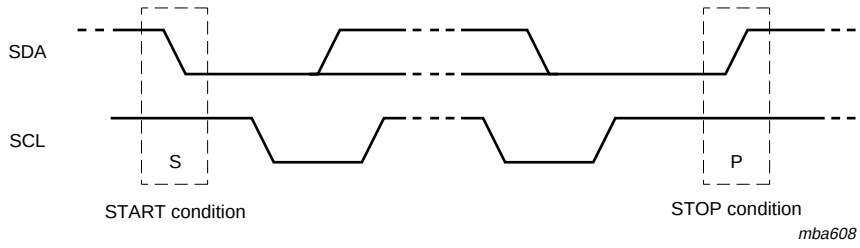


Fig 8. Definition of start and stop conditions

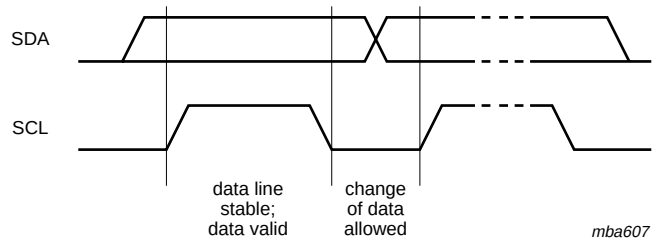


Fig 9. Bit transfer

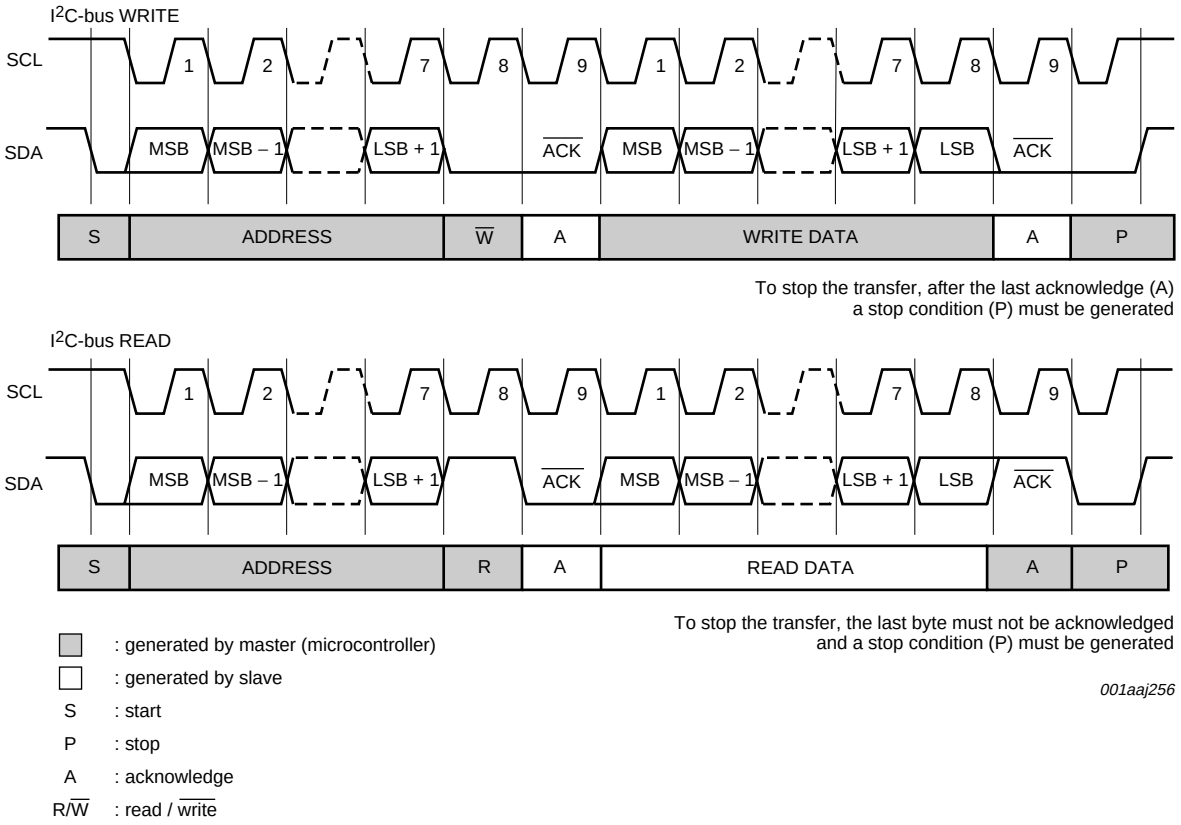


Fig 10. I²C-bus read and write modes

Table 4. Instruction byte IB1 bit description

Bit	Symbol	Description
7	D7	regulator 5 output voltage control; see Table 5
6	D6	
5	D5	
4	D4	
3	D3	SW2 control
		0 = SW2 off
		1 = SW2 on

Table 4. Instruction byte IB1 bit description *...continued*

Bit	Symbol	Description
2	D2	SW1 control
		0 = SW1 off
		1 = SW1 on
1	D1	AC load or DC load detection switch
		0 = AC load or DC load detection off; resets DC load detection bits and AC load detection peak current counter
		1 = AC load or DC load detection on
0	D0	amplifier start enable (clear power-on reset flag DB2[D7])
		0 = amplifier off; pin $\overline{DIAG}$ remains LOW
		1 = amplifier on; when power-on occurs, bit DB2[D7] is reset and pin $\overline{DIAG}$ is released

Table 5. Regulator 5 (display) output voltage control

Bit				Output (V)
D7	D6	D5	D4	
0	0	0	0	0 (off)
0	0	0	1	6.0
0	0	1	0	7.0
0	0	1	1	8.2
0	1	0	0	9.0
0	1	0	1	9.5
0	1	1	0	10.0
0	1	1	1	10.4
1	0	0	0	12.5
1	0	0	1	$\leq V_P - 1$ (switch)
1	0	1	0	5.0
1	0	1	1	3.3

Table 6. Instruction byte IB2 bit description

Bit	Symbol	Description
7	D7	regulator 4 output voltage control; see Table 7
6	D6	
5	D5	
4	D4	regulator 3 (mechanical digital) control
		0 = regulator 3 off
		1 = regulator 3 on
3	D3	regulator 1 output voltage control; see Table 8
2	D2	
1	D1	soft mute all amplifier channels (mute delay 20 ms)
		0 = mute off
		1 = mute on

Table 6. Instruction byte IB2 bit description *...continued*

Bit	Symbol	Description
0	D0	hard mute all amplifier channels (mute delay 0.4 ms)
		0 = mute off
		1 = mute on

Table 7. Regulator 4 (mechanical drive) output voltage control

Bit			Output (V)
D7	D6	D5	
0	0	0	0 (off)
0	0	1	5
0	1	0	6
0	1	1	7
1	0	0	8.6
1	0	1	8.0

Table 8. Regulator 1 (audio) output voltage control

Bit		Output (V)
D3	D2	
0	0	0 (off)
0	1	8.3
1	0	8.6
1	1	5.0

Table 9. Instruction byte IB3 bit description

Bit	Symbol	Description
7	D7	clip detection level
		0 = 3 % detection level
		1 = 1 % detection level
6	D6	amplifier channels 1 and 2 gain select
		0 = 26 dB gain (normal mode)
		1 = 20 dB gain (line-driver mode)
5	D5	amplifier channels 3 and 4 gain select
		0 = 26 dB gain (normal mode)
		1 = 20 dB gain (line-driver mode)
4	D4	amplifier thermal protection pre-warning
		0 = warning at 145 °C
		1 = warning at 122 °C
3	D3	disable channel 1
		0 = enable channel 1
		1 = disable channel 1

Table 9. Instruction byte IB3 bit description *...continued*

Bit	Symbol	Description
2	D2	disable channel 2
		0 = enable channel 2
		1 = disable channel 2
1	D1	disable channel 3
		0 = enable channel 3
		1 = disable channel 3
0	D0	disable channel 4
		0 = enable channel 4
		1 = disable channel 4

Table 10. Instruction byte DB1 bit description

Bit	Symbol	Description
7	D7	amplifier thermal protection pre-warning
		0 = no warning
		1 = junction temperature above pre-warning level
6	D6	amplifier maximum thermal protection
		0 = junction temperature below 175 °C
		1 = junction temperature above 175 °C
5	D5	channel 4 DC load detection
		0 = DC load detected
		1 = no DC load detected
4	D4	channel 4 AC load detection
		0 = no AC load detected
		1 = AC load detected
3	D3	channel 4 load short-circuit
		0 = normal load
		1 = short-circuit load
2	D2	channel 4 output offset
		0 = no output offset
		1 = output offset
1	D1	channel 4 V_P short-circuit
		0 = no short-circuit to V_P
		1 = short-circuit to V_P
0	D0	channel 4 short-circuit to ground
		0 = no short-circuit to ground
		1 = short-circuit to ground

Table 11. Data byte DB2 bit description

Bit	Symbol	Description
7	D7	Power-on reset occurred or amplifier status
		0 = amplifier on
		1 = POR has occurred; amplifier off
6	D6	regulator thermal protection pre-warning
		0 = no warning
		1 = regulator temperature too high; amplifier off
5	D5	channel 3 DC load detection
		0 = DC load detected
		1 = no DC load detected
4	D4	channel 3 AC load detection
		0 = no AC load detected
		1 = AC load detected
3	D3	channel 3 load short-circuit
		0 = normal load
		1 = short-circuit load
2	D2	channel 3 output offset
		0 = no output offset
		1 = output offset
1	D1	channel 3 V_P short-circuit
		0 = no short-circuit to V_P
		1 = short-circuit to V_P
0	D0	channel 3 short-circuit to ground
		0 = no short-circuit to ground
		1 = short-circuit to ground

Table 12. Data byte DB3 bit description

Bit	Symbol	Description
7	D7	-
6	D6	-
5	D5	channel 2 DC load detection
		0 = DC load detected
		1 = no DC load detected
4	D4	channel 2 AC load detection
		0 = no AC load detected
		1 = AC load detected
3	D3	channel 2 load short-circuit
		0 = normal load
		1 = short-circuit load
2	D2	channel 2 output offset
		0 = no output offset
		1 = output offset

Table 12. Data byte DB3 bit description *...continued*

Bit	Symbol	Description
1	D1	channel 2 V_P short-circuit
		0 = no short-circuit to V_P
		1 = short-circuit to V_P
0	D0	channel 2 short-circuit to ground
		0 = no short-circuit to ground
		1 = short-circuit to ground

Table 13. Data byte DB4 bit description

Bit	Symbol	Description
7	D7	-
6	D6	-
5	D5	channel 1 DC load detection
		0 = DC load detected
		1 = no DC load detected
4	D4	channel 1 AC load detected
		0 = no AC load detected
		1 = AC load detected
3	D3	channel 1 load short-circuit
		0 = normal load
		1 = short-circuit load
2	D2	channel 1 output offset
		0 = no output offset
		1 = output offset
1	D1	channel 1 short-circuit to V_P
		0 = no short-circuit to V_P
		1 = short-circuit to V_P
0	D0	channel 1 short-circuit to ground
		0 = no short-circuit to ground
		1 = short-circuit to ground

9. Limiting values

Table 14. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_P	supply voltage	operating	-	18	V
		not operating	–1	+50	V
		jump starts for t ≤ 10 minutes	-	30	V
		load dump protection for t ≤ 50 ms and t_r ≥ 2.5 ms	0	50	V
V_{SDA}	voltage on pin SDA	operating	0	7	V

Table 14. Limiting values *...continued*

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{SCL}	voltage on pin SCL	operating	0	7	V
V_I	input voltage	pins INn, SVR, ACGND, $\overline{DIAG}$, operating	0	13	V
V_{STB}	voltage on pin STB	operating	0	24	V
I_{OSM}	non-repetitive peak output current		-	10	A
I_{ORM}	repetitive peak output current		-	6	A
$V_{P(sc)}$	short-circuit supply voltage	across output pin loads and to ground or supply (AC and DC)	-	18	V
$V_{P(r)}$	reverse supply voltage	voltage regulator only	-	–18	V
P_{tot}	total power dissipation	T_{case} = 70 °C	-	80	W
T_j	junction temperature		-	150	°C
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	ambient temperature		–40	+85	°C
V_{ESD}	electrostatic discharge voltage	[1]	-	2000	V
		[2]	-	200	V

[1] Human body model: R_s = 1.5 kΩ; C = 100 pF; all pins have passed all tests to 2500 V to guarantee 2000 V, according to class II.

[2] Machine model: R_s = 10 Ω; C = 200 pF; L = 0.75 mH; all pins have passed all tests to 250 V to guarantee 200 V, according to class II.

10. Thermal characteristics

Table 15. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	40	K/W
$R_{th(j-c)}$	thermal resistance from junction to case	see Figure 11	0.75	K/W

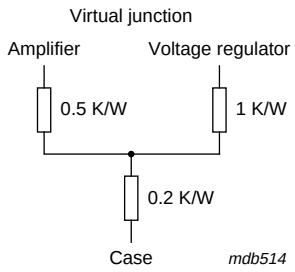


Fig 11. Equivalent thermal resistance network

10.1 Quality specification

In accordance with *"General Quality Specification for Integrated Circuits SNW-FQ-611D"*.

11. Characteristics

Table 16. Characteristics

T_{amb} = 25 °C; V_{DCDC}; V_P = 14.4 V; R_L = 4 Ω; measured in the test circuit Figure 26; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Amplifier						
Supply voltage behavior						
$V_{P(oper)}$	operating supply voltage	R_L = 4 Ω	8	14.4	18	V
		R_L = 2 Ω	8	14.4	16	V
$I_{q(tot)}$	total quiescent current	no load	-	280	400	mA
I_{stb}	standby current		-	10	50	µA
V_O	output voltage	DC	-	7.2	-	V
$V_{P(low)(mute)}$	low supply voltage mute		6.5	7	8	V
V_{hr}	headroom voltage	when headroom protection is activated; see Figure 4	-	1.4	-	V
V_{POR}	power-on reset voltage	see Figure 13	-	5.5	-	V
$V_{O(offset)}$	output offset voltage	mute mode and power on	–100	0	+100	mV
Mode select (pin STB)						
V_{STB}	voltage on pin STB	Standby mode	-	-	1.3	V
		operating mode	2.5	-	5.5	V
		mute mode	8	-	V_P	V
I_I	input current	V_{STB} = 5 V	-	4	25	µA
Start-up, shutdown and mute timing						
t_{wake}	wake-up time	from standby before first I²C-bus transmission is recognized; via pin STB; see Figure 12	-	300	500	µs
$t_{d(mute\_off)}$	mute off delay time	via I²C-bus IB1[D0]; C_{SVR} = 22 µF; see Figure 12	-	250	-	ms
$t_{d(mute-on)}$	delay time from mute to on	soft mute; via I²C-bus IB2[D1] = 1 to 0	10	25	40	ms
		hard mute; via I²C-bus IB2[D0] = 1 to 0	10	25	40	ms
		via pin STB; V_{STB} = 8 V to 4 V	10	25	40	ms
$t_{d(on-mute)}$	delay time from on to mute	soft mute; via I²C-bus IB2[D1] = 0 to 1	10	25	40	ms
		hard mute; via I²C-bus IB2[D0] = 0 to 1	-	0.4	1	ms
		via pin STB; V_{STB} = 4 V to 8 V	-	0.4	1	ms
I²C-bus interface						
V_{IL}	LOW-level input voltage	on pins SCL and SDA	-	-	1.5	V
V_{IH}	HIGH-level input voltage	on pins SCL and SDA	2.3	-	5.5	V
V_{OL}	LOW-level output voltage	on pin SDA; I_{load} = 3 mA	-	-	0.4	V
f_{SCL}	SCL clock frequency		-	-	400	kHz

Table 16. Characteristics *...continued*

T_{amb} = 25 °C; V_{DCDC}; V_P = 14.4 V; R_L = 4 Ω; measured in the test circuit Figure 26; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Amplifier diagnostics						
$V_{OL(DIAG\_N)}$	LOW-level output voltage on pin $\overline{DIAG}$	fault condition (pin LOW); I_{DIAG_N} = 200 µA	-	-	0.8	V
$V_{O(offset)}$	output offset voltage		±1.5	±2	±2.5	V
THD_{clip}	total harmonic distortion clip detection level	IB3[D7] = 0	-	3	-	%
		IB3[D7] = 1	-	1	-	%
$T_{j(AV)(pwarn)}$	pre-warning average junction temperature	IB3[D4] = 0	135	145	155	°C
		IB3[D4] = 1	112	122	132	°C
$T_{j(AV)(mute)}$	mute average junction temperature	V_{IN} = 0.05 V; −3 dB muting	150	160	170	°C
$T_{j(AV)(off)}$	average junction temperature for off	all outputs switched off	165	175	185	°C
Z_L	load impedance	DC load detected	-	-	6	Ω
		no DC load detected	500	-	-	Ω
$I_{det(load)}$	load detection current	AC load detected	550	-	-	mA
		no AC load detected	-	-	150	mA
Amplifier						
P_o	output power	R_L = 4 Ω; V_P = 14.4 V; THD = 0.5 %	18	19	-	W
		R_L = 4 Ω; V_P = 14.4 V; THD = 10 %	25	26	-	W
		R_L = 2 Ω; V_P = 14.4 V; THD = 0.5 %	27	31	-	W
		R_L = 2 Ω; V_P = 14.4 V; THD = 10 %	40	44	-	W
$P_{o(max)}$	maximum output power	R_L = 4 Ω; V_P = 14.4 V; V_{IN} = 2 V RMS square wave	39	41	-	W
		R_L = 4 Ω; V_P = 15.2 V; V_{IN} = 2 V RMS square wave	44	46	-	W
		R_L = 2 Ω; V_P = 14.4 V; V_{IN} = 2 V RMS square wave	64	69	-	W
THD	total harmonic distortion	P_o = 1 W to 12 W; f = 1 kHz; R_L = 4 Ω	-	0.01	0.1	%
		P_o = 1 W to 12 W; f = 10 kHz	-	0.2	0.5	%
		P_o = 4 W; f = 1 kHz	-	0.01	0.03	%
		line driver mode; V_o = 2 V (RMS); f = 1 kHz; R_L = 600 Ω	-	0.01	0.03	%
α_{cs}	channel separation	f = 1 Hz to 10 kHz; R_s = 600 Ω	50	60	-	dB
		P_o = 4 W; f = 1 kHz	-	80	-	dB
SVRR	supply voltage rejection ratio	f = 100 Hz to 10 kHz; R_s = 600 Ω	55	70	-	dB
CMRR	common mode rejection ratio	amplifier mode; V_{cm} = 0.3 V (p-p); f = 1 kHz to 3 kHz; R_s = 0 Ω	40	70	-	dB

Table 16. Characteristics *...continued*

T_{amb} = 25 °C; V_{DCDC}; V_P = 14.4 V; R_L = 4 Ω; measured in the test circuit Figure 26; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{cm(max)(rms)}$	maximum common mode voltage (rms value)	f = 1 kHz		-	-	0.6	V
$V_{n(o)}$	output noise voltage	filter 20 Hz to 22 kHz; R_s = 600 Ω					
		line driver mode		-	25	35	μV
		amplifier mode		-	50	70	μV
$G_{v(amp)}$	voltage gain amplifier mode	single-ended in to differential out		25	26	27	dB
$G_{v(ld)}$	voltage gain line driver mode	single-ended in to differential out		19	20	21	dB
Z_i	input impedance	C_{in} = 220 nF		55	70	-	kΩ
α_{mute}	mute attenuation	$V_{O(on)}/V_{o(mute)}$		80	90	-	dB
$V_{o(mute)}$	mute output voltage	V_i = 1 V RMS		-	70	-	μV
B_p	power bandwidth	–1 dB; THD = 1 %		-	20	-	kHz
Voltage regulators							
V_P	supply voltage	regulator 1, 3, 4 and 5 on; switches 1 and 2 on		10.0	14.4	18	V
		standby regulator 2 in regulation		5.0	-	50	V
		standby regulator 6 in regulation		6.0	-	50	V
$V_{th(dis)}$	disable threshold voltage	regulator 1, 3, 4 and 5 on; switches 1 and 2 on		18.1	22	-	V
V_{DCDC}	DC-to-DC converter voltage			4.75	5.0	V_P	V
$I_{q(tot)}$	total quiescent current	Standby mode; V_P = 14.4 V	[1]	-	180	250	μA
Regulator 1 audio supply: pin REG1; I_O = 5 mA unless otherwise specified							
$V_{O(reg)}$	regulator output voltage	0.5 mA ≤ I_O ≤ 400 mA; 10 V < V_P < 18 V					
		IB2[D3:D2] = 01		7.9	8.3	8.7	V
		IB2[D3:D2] = 10		8.1	8.6	9.1	V
		IB2[D3:D2] = 11		4.75	5.0	5.25	V
SVRR	supply voltage rejection ratio	f_{ripple} = 120 Hz; V_{ripple} = 2 V (p-p)		50	60	-	dB
V_{do}	dropout voltage	V_P = 7 V; IB2[D3:D2] = 01	[3]				
		I_O = 300 mA		-	0.5	0.8	V
		I_O = 400 mA		-	0.7	1.2	V
I_O	output current	V_O ≥ 4 V	[4]	400	700	-	mA
I_{OS}	output short-circuit current	R_L ≤ 0.5 Ω	[5]	100	200	-	mA
Line regulation							
ΔV_O	output voltage variation	10 V ≤ V_P ≤ 18 V		-	-	50	mV
Load regulation							
ΔV_O	output voltage variation	5 mA ≤ I_O ≤ 400 mA		-	-	100	mV

Table 16. Characteristics *...continued*

T_{amb} = 25 °C; V_{DCDC}; V_P = 14.4 V; R_L = 4 Ω; measured in the test circuit Figure 26; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Regulator 2 microprocessor supply: pin REG2; I_O = 5 mA unless otherwise specified							
$V_{O(reg)}$	regulator output voltage	0.5 mA ≤ I_O ≤ 350 mA; 10 V ≤ V_P ≤ 18 V		3.1	3.3	3.5	V
SVRR	supply voltage rejection ratio	f_{ripple} = 120 Hz; V_{ripple} = 2 V (p-p)		40	50	-	dB
V_{do}	dropout voltage	V_{BUCAP} = 4.75 V	[6][8]				
		I_O = 350 mA		-	1.45	2.0	V
I_O	output current	V_O ≥ 2.8 V	[4]	350	1000	-	mA
I_{OS}	output short-circuit current	R_L ≤ 0.5 Ω	[5]	160	300	-	mA
Line regulation							
ΔV_O	output voltage variation	10 V ≤ V_P ≤ 18 V		-		50	mV
Load regulation							
ΔV_O	output voltage variation	0.5 mA ≤ I_O ≤ 350 mA		-	-	100	mV
Regulator 3 mechanical digital supply: pin REG3; I_O = 5 mA unless otherwise specified							
$V_{O(reg)}$	regulator output voltage	0.5 mA ≤ I_O ≤ 525 mA; 10 V ≤ V_P ≤ 18 V	[9]	3.1	3.3	3.5	V
		5 V ≤ V_{DCDC} ≤ 18 V					
SVRR	supply voltage rejection ratio	f_{ripple} = 120 Hz; V_{ripple} = 2 V (p-p)		50	65	-	dB
V_{do}	dropout voltage	V_{DCDC} = 4.75 V; I_O = 525 mA	[2][8]	-	1.45	2.0	V
I_O	output current	V_O ≥ 2.8 V	[4]	525	900	-	mA
I_{OS}	output short-circuit current	R_L ≤ 0.5 Ω	[5]	180	350	-	mA
Line regulation							
ΔV_O	output voltage variation	5 V ≤ V_{DCDC} ≤ 18 V		-	3	50	mV
Load regulation							
ΔV_O	output voltage variation	0.5 mA ≤ I_O ≤ 525 mA		-	-	100	mV
Regulator 4 mechanical drive supply: pin REG4; I_O = 5 mA unless otherwise specified							
$V_{O(reg)}$	regulator output voltage	0.5 mA ≤ I_O ≤ 800 mA; 10 V ≤ V_P ≤ 18 V					
		IB2[D7:D5] = 001		4.75	5.0	5.25	V
		IB2[D7:D5] = 010		5.7	6.0	6.3	V
		IB2[D7:D5] = 011		6.6	7.0	7.4	V
		IB2[D7:D5] = 100		8.1	8.6	9.1	V
		IB2[D7:D5] = 101		7.6	8.0	8.4	V
SVRR	supply voltage rejection ratio	f_{ripple} = 120 Hz; V_{ripple} = 2 V (p-p)		50	65	-	dB
V_{do}	dropout voltage	V_P = 7 V; IB2[D7:D5] = 011	[3]				
		I_O = 500 mA		-	0.5	0.8	V
		I_O = 800 mA		-	0.7	1.2	V
I_{OM}	peak output current	T ≤ 3 s; V_O = 4 V		1	1.5	-	A
I_O	output current	V_O ≥ 4 V; T ≤ 100 ms; V_P ≥ 11.5 V	[4]	1.5	2	-	A

Table 16. Characteristics *...continued*

T_{amb} = 25 °C; V_{DCDC}; V_P = 14.4 V; R_L = 4 Ω; measured in the test circuit Figure 26; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{OS}	output short-circuit current	$R_L \leq 0.5\ \Omega$	[5]	240	400	-	mA
Line regulation							
ΔV_O	output voltage variation	$10\ V \leq V_P \leq 18\ V$		-	3	50	mV
Load regulation							
ΔV_O	output voltage variation	$0.5\ mA \leq I_O \leq 800\ mA$		-	-	100	mV
Regulator 5 display supply: pin REG5; I_O = 5 mA unless otherwise specified							
$V_{O(reg)}$	regulator output voltage	$0.5\ mA \leq I_O \leq 400\ mA$					
		$10\ V \leq V_P \leq 18\ V$; IB1[D7:D4] = 0001		5.7	6.0	6.3	V
		$10\ V \leq V_P \leq 18\ V$; IB1[D7:D4] = 0010		6.65	7.0	7.37	V
		$10\ V \leq V_P \leq 18\ V$; IB1[D7:D4] = 0011		7.8	8.2	8.6	V
		$10.5\ V \leq V_P \leq 18\ V$; IB1[D7:D4] = 0100		8.55	9.0	9.45	V
		$11\ V \leq V_P \leq 18\ V$; IB1[D7:D4] = 0101		9.0	9.5	10.0	V
		$11.5\ V \leq V_P \leq 18\ V$; IB1[D7:D4] = 0110		9.5	10.0	10.5	V
		$13\ V \leq V_P \leq 18\ V$; IB1[D7:D4] = 0111		9.9	10.4	10.9	V
		$14.2\ V \leq V_P \leq 18\ V$; IB1[D7:D4] = 1000		11.8	12.5	13.2	V
		$12.5\ V \leq V_P \leq 18\ V$; IB1[D7:D4] = 1001		$V_P - 1$	$V_P - 0.5$	-	V
		$10\ V \leq V_P \leq 18\ V$; IB1[D7:D4] = 1010		4.75	5.0	5.25	V
		$10\ V \leq V_P \leq 18\ V$; IB1[D7:D4] = 1011		3.1	3.3	3.5	V
SVRR	supply voltage rejection ratio	f_{ripple} = 120 Hz; V_{ripple} = 2 V (p-p)		50	60	-	dB
V_{do}	dropout voltage	V_P = 7 V; IB1[D7:D4] = 0010	[3]				
		I_O = 300 mA		-	0.5	0.8	V
		I_O = 400 mA		-	0.7	1.2	V
I_O	output current	$V_O \geq 2.8\ V$	[4]	400	900	-	mA
I_{OS}	output short-circuit current	$R_L \leq 0.5\ \Omega$	[5]	150	300	-	mA
Line regulation							
ΔV_O	output voltage variation	$10\ V \leq V_P \leq 18\ V$		-	3	50	mV
Load regulation							
ΔV_O	output voltage variation	$0.5\ mA \leq I_O \leq 400\ mA$		-	-	100	mV
Regulator 6 bus control supply: pin REG6; I_O = 5 mA unless otherwise specified							
$V_{O(reg)}$	regulator output voltage	$0.5\ mA \leq I_O \leq 100\ mA$; $10\ V \leq V_P \leq 18\ V$		4.75	5.0	5.25	V

Table 16. Characteristics *...continued*

T_{amb} = 25 °C; V_{DCDC}; V_P = 14.4 V; R_L = 4 Ω; measured in the test circuit Figure 26; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
SVRR	supply voltage rejection ratio	f_{ripple} = 120 Hz; V_{ripple} = 2 V (p-p)		40	50	-	dB
V_{do}	dropout voltage	V_P = 4.75 V; I_O = 100 mA	[3]	-	0.4	0.8	V
I_O	output current	V_O > 4.0 V	[4]	150	350	-	mA
I_{OS}	output short-circuit current	R_L < 0.5 Ω	[5]	50	125	-	mA
Line regulation							
ΔV_O	output voltage variation	10 V ≤ V_P ≤ 18 V		-	3	50	mV
Load regulation							
ΔV_O	output voltage variation	0.5 mA ≤ I_O ≤ 100 mA		-	-	100	mV
Power switch 1 antenna: pin SW1							
V_{do}	dropout voltage	I_O = 300 mA		-	0.6	0.8	V
		I_O = 400 mA		-	0.6	1.1	V
I_O	output current	V_O ≥ 8.5 V	[4]	0.5	1	-	A
I_{OS}	output short-circuit current	R_L ≤ 0.5 Ω	[5]	-	250	-	mA
I_L	leakage current	V_O = 18 V; V_P = 0 V	[7]	-	25	250	µA
Power switch 2 amplifier: pin SW2							
V_{do}	dropout voltage	I_O = 300 mA		-	0.6	0.8	V
		I_O = 400 mA		-	0.6	1.1	V
I_O	output current	V_O ≥ 8.5 V	[4]	0.5	1	-	A
I_{OS}	output short-circuit current	R_L ≤ 0.5 Ω	[5]	-	250	-	mA
I_L	leakage current	V_O = 18 V; V_P = 0 V	[7]	-	25	250	µA
Backup switch							
I_{bu}	backup current (DC)	V_{BUCAP} ≥ 6 V		0.4	1.5	-	A
V_{CL}	clamping voltage	V_P = 30 V; $I_{O(reg2)}$ = 100 mA		-	24	28	V
V_{do}	dropout voltage	I_O = 500 mA; (V_P – V_{BUCAP})		-	0.8	1.2	V

[1] The quiescent current is measured in Standby mode when R_L = ∞.

[2] The dropout voltage of regulator 3 is the voltage difference between V_{DCDC} and $V_{O(reg)}$.

[3] The dropout voltage of a regulator is the voltage difference between V_P and $V_{O(reg)}$.

[4] At current limit, $V_{O(reg)}$ is held constant; see Figure 6.

[5] The foldback current protection limits the dissipation power at short-circuit; see Figure 6.

[6] The dropout voltage of regulator 2 is the voltage difference between V_{BUCAP} and $V_{O(reg)}$.

[7] Unbiased switch-supply I_L is measured in supply line V_P.

[8] Regulator output still in regulation at applied test voltage, therefore the actual dropout voltage can not be measured.

[9] The current capability of regulator 3 is sufficient to drive NXP Semiconductors' DSP devices SAF7730, SAF7740 or SAF7741.

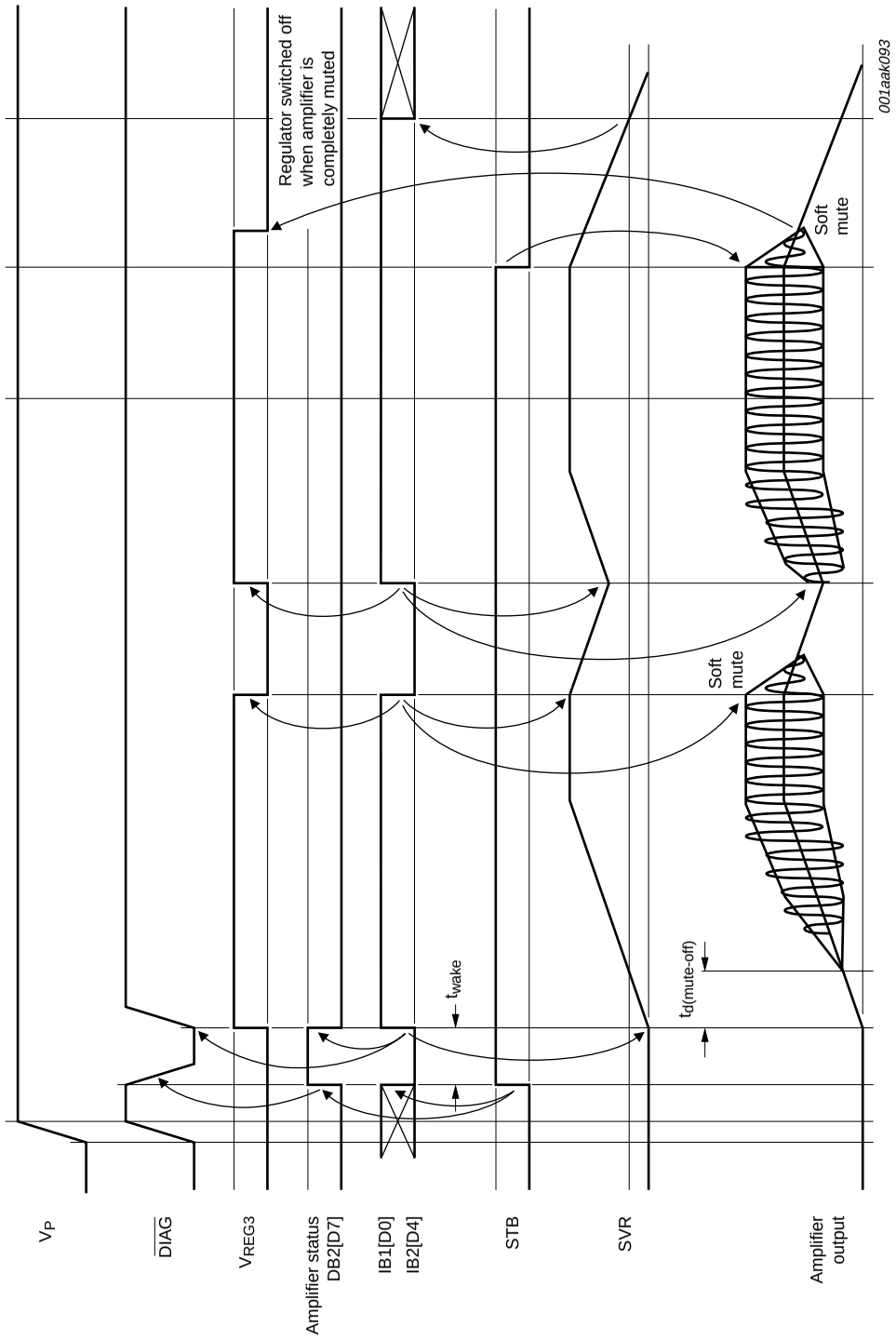


Fig 12. Start-up and shutdown timing

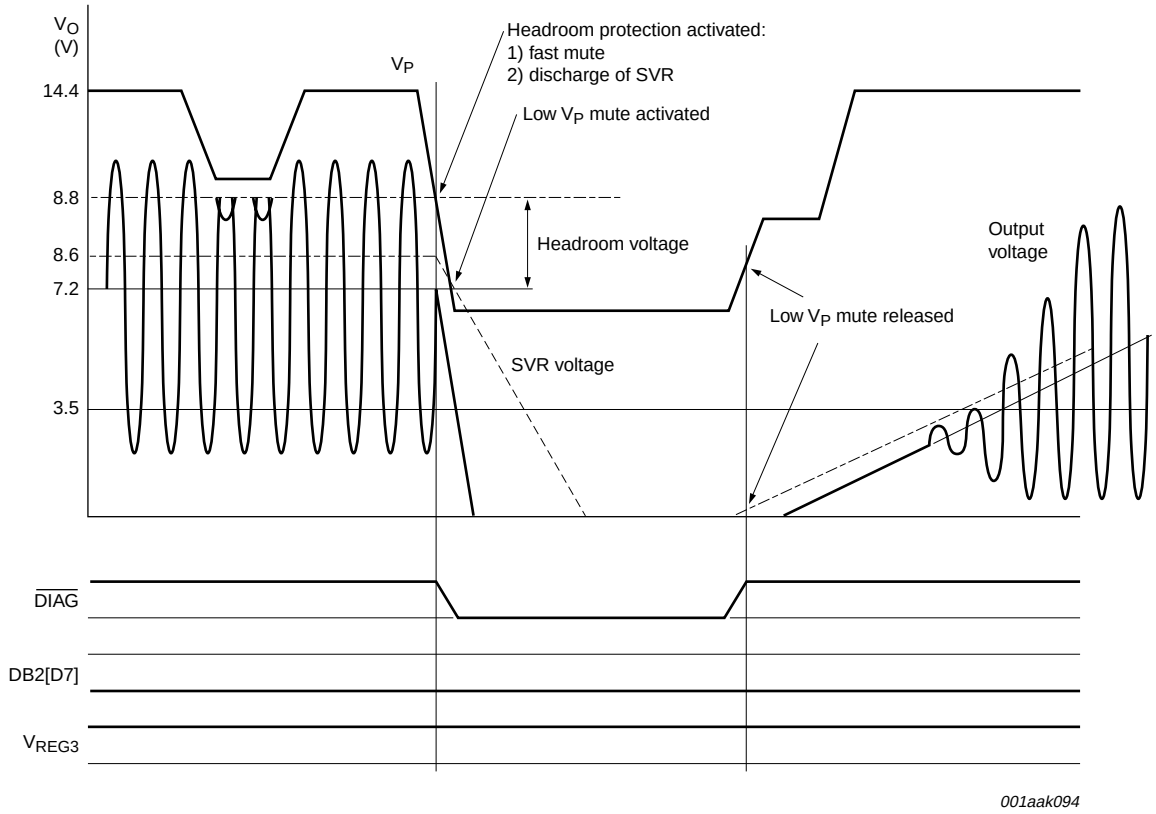


Fig 13. Low supply voltage behavior at V_P > 5.5 V

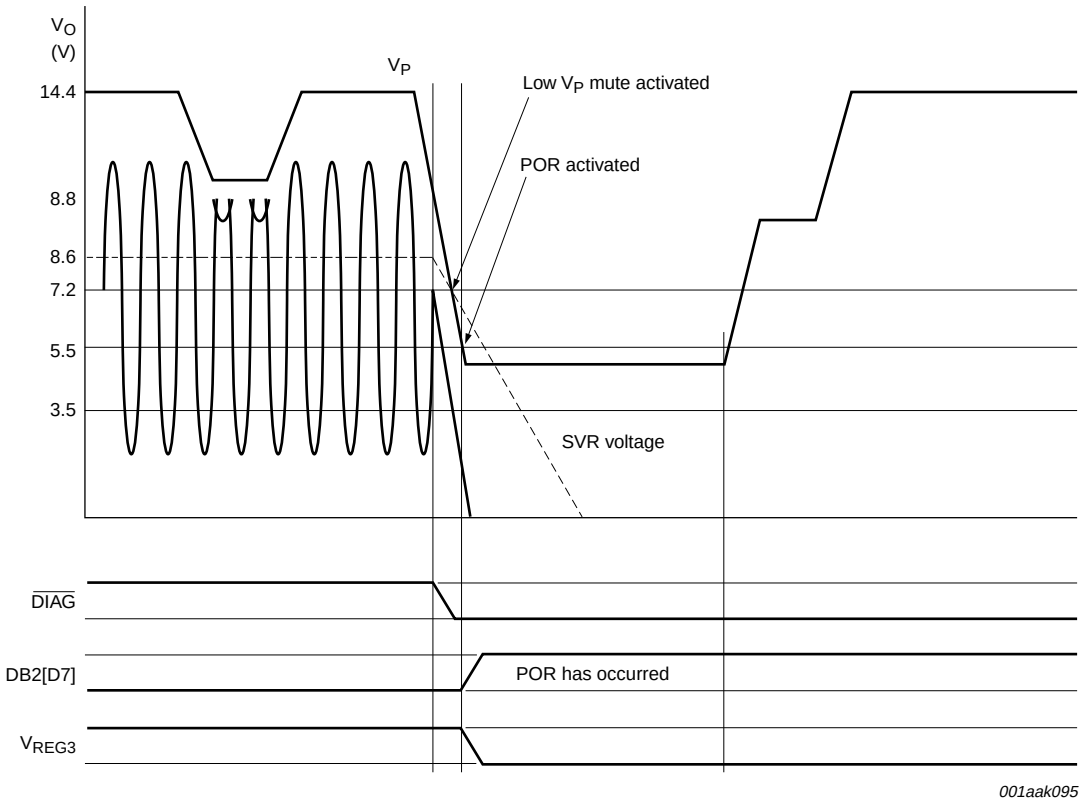
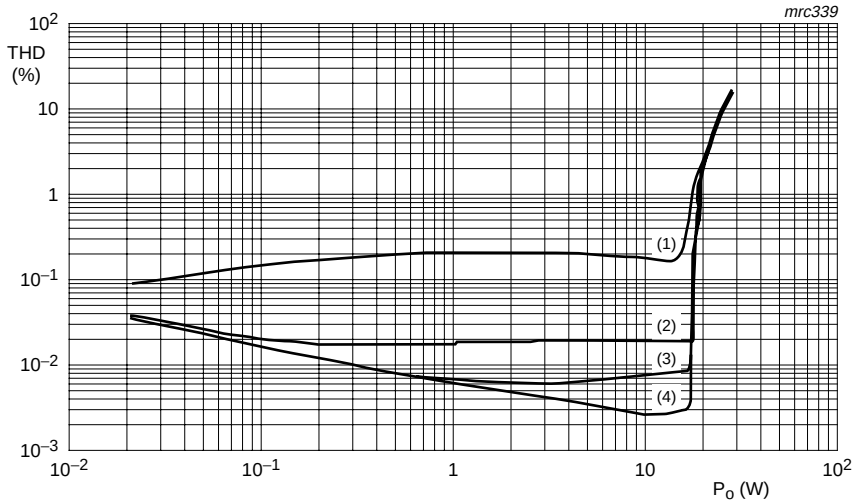


Fig 14. Low supply voltage behavior at V_P < 5.5 V



(1) f = 10 kHz (channels 1 to 4).

(2) f = 100 Hz and 1 kHz (channels 1 and 2).

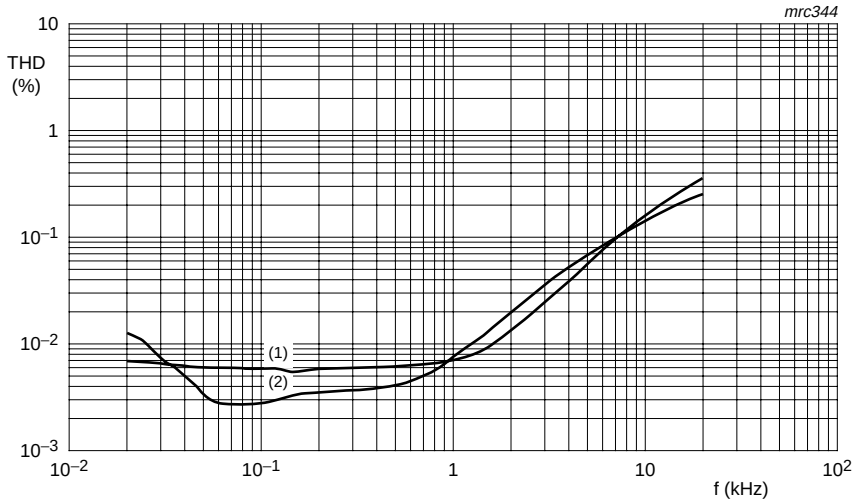
(3) f = 1 kHz (channels 3 and 4).

(4) f = 100 Hz (channels 3 and 4).

V_P = 14.4 V.

R_L = 4 Ω.

Fig 15. Total harmonic distortion as a function of output power



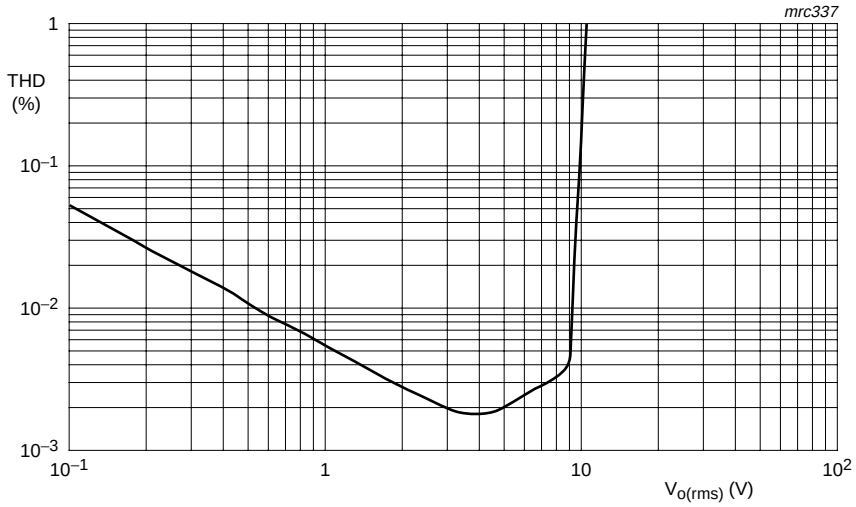
(1) P_o = 1 W.

(2) P_o = 10 W.

V_P = 14.4 V.

R_L = 4 Ω.

Fig 16. Total harmonic distortion as a function of frequency

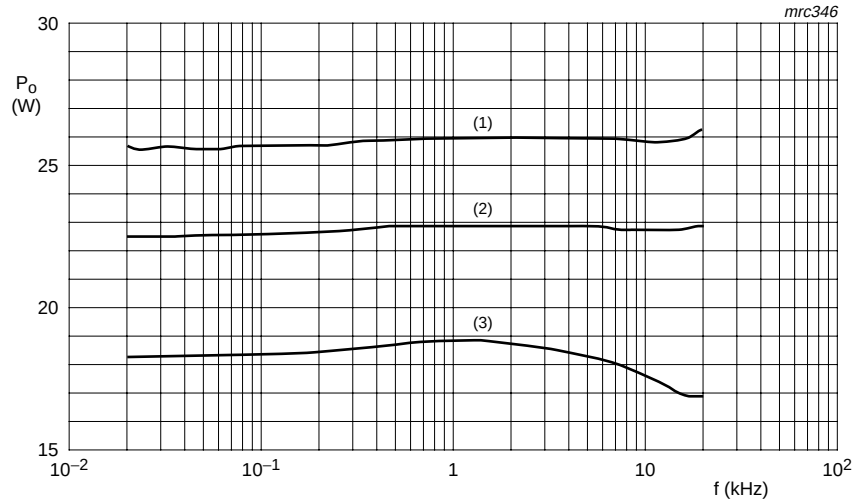


V_P = 14.4 V.

R_L = 600 Ω.

f = 1 kHz.

Fig 17. Total harmonic distortion as a function of output voltage in balanced line driver mode



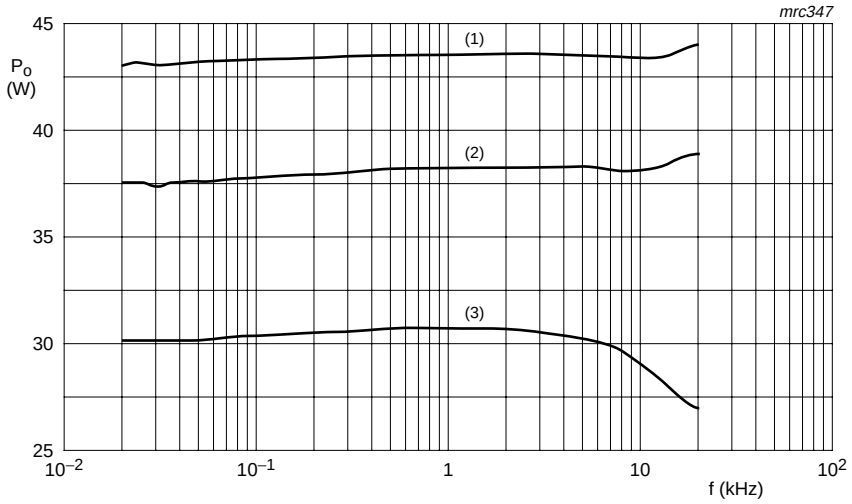
V_P = 14.4 V; R_L = 4 Ω

(1) THD = 10 %.

(2) THD = 5 %.

(3) THD = 0.5 %.

Fig 18. Output power as a function of frequency



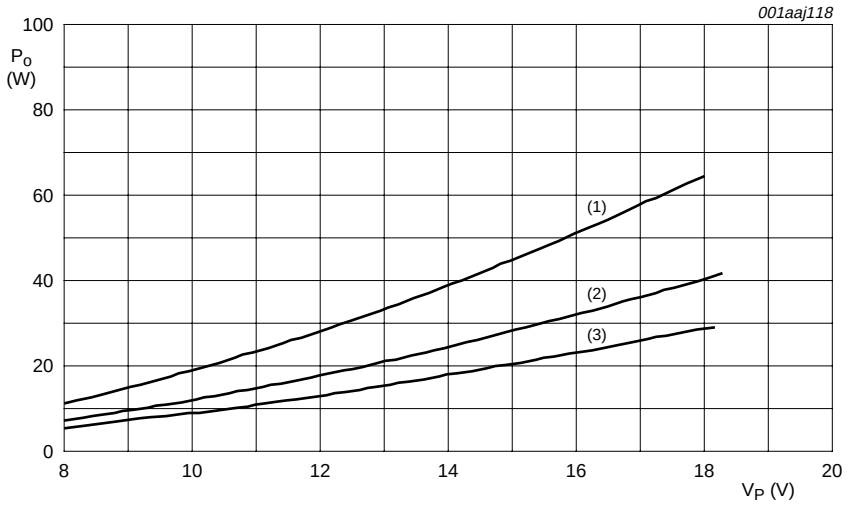
V_P = 14.4 V; R_L = 2 Ω

(1) THD = 10 %.

(2) THD = 5 %.

(3) THD = 0.5 %.

Fig 19. Output power as a function of frequency



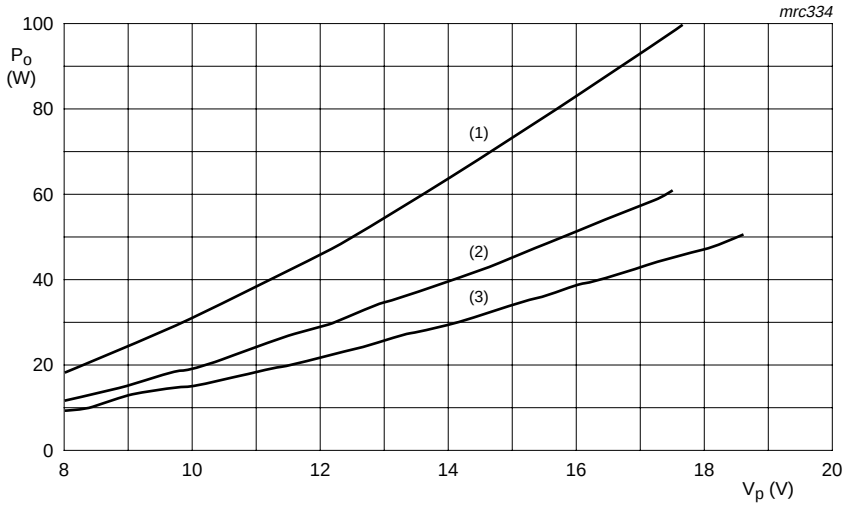
f = 1 kHz; R_L = 4 Ω

(1) Maximum power.

(2) THD = 10 %.

(3) THD = 0.5 %.

Fig 20. Output power as a function of supply voltage



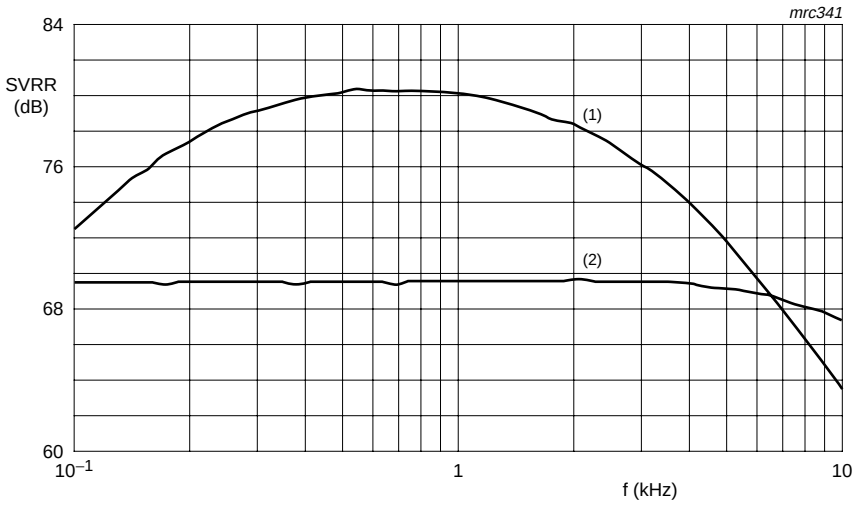
f = 1 kHz; R_L = 2 Ω

(1) Maximum power.

(2) THD = 10 %.

(3) THD = 0.5 %.

Fig 21. Output power as a function of supply voltage



(1) Operating mode.

(2) Mute mode.

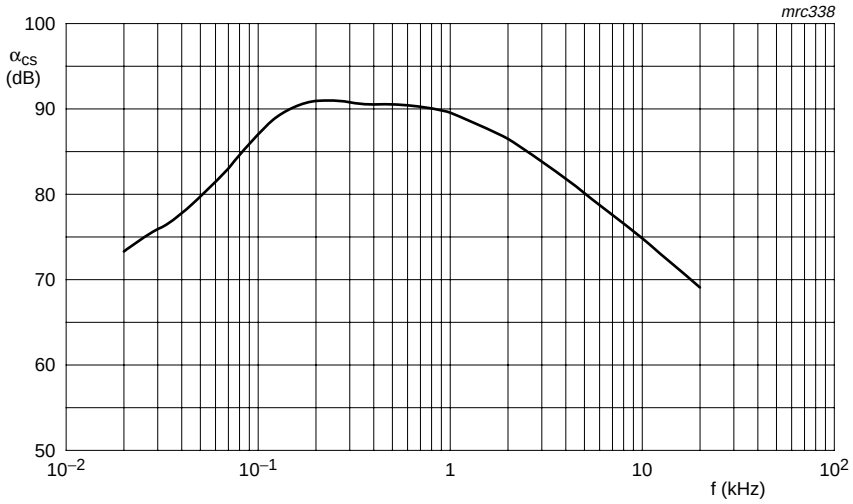
V_P = 14.4 V.

R_L = 4 Ω.

V_{ripple} = 2 V (p-p).

R_s = 600 Ω.

Fig 22. Supply voltage rejection ratio as a function of frequency



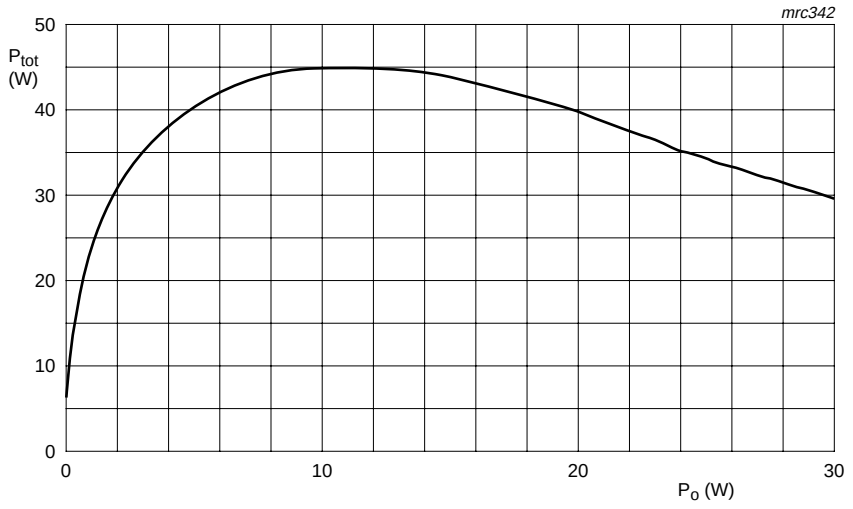
V_P = 14.4 V.

R_L = 4 Ω.

P_o = 4 W.

R_s = 600 Ω.

Fig 23. Channel separation

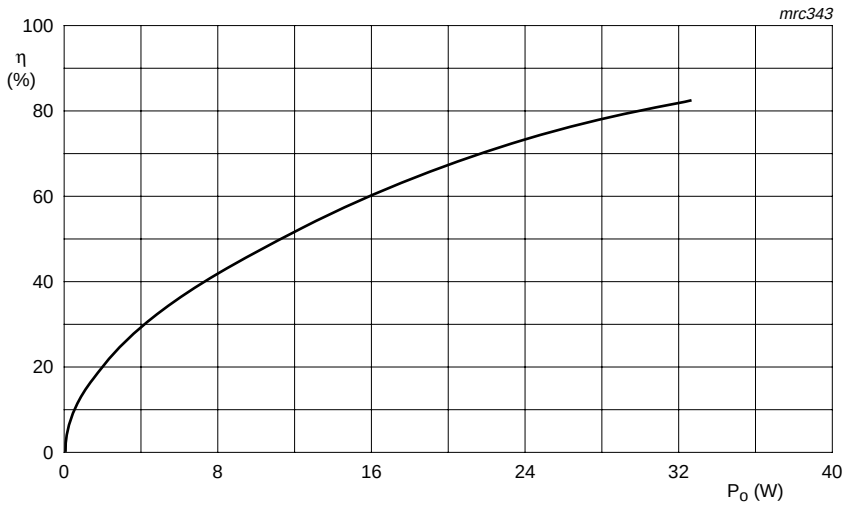


V_P = 14.4 V.

R_L = 4 Ω.

f = 1 kHz.

Fig 24. Amplifier power dissipation as a function of output power; all channels driven



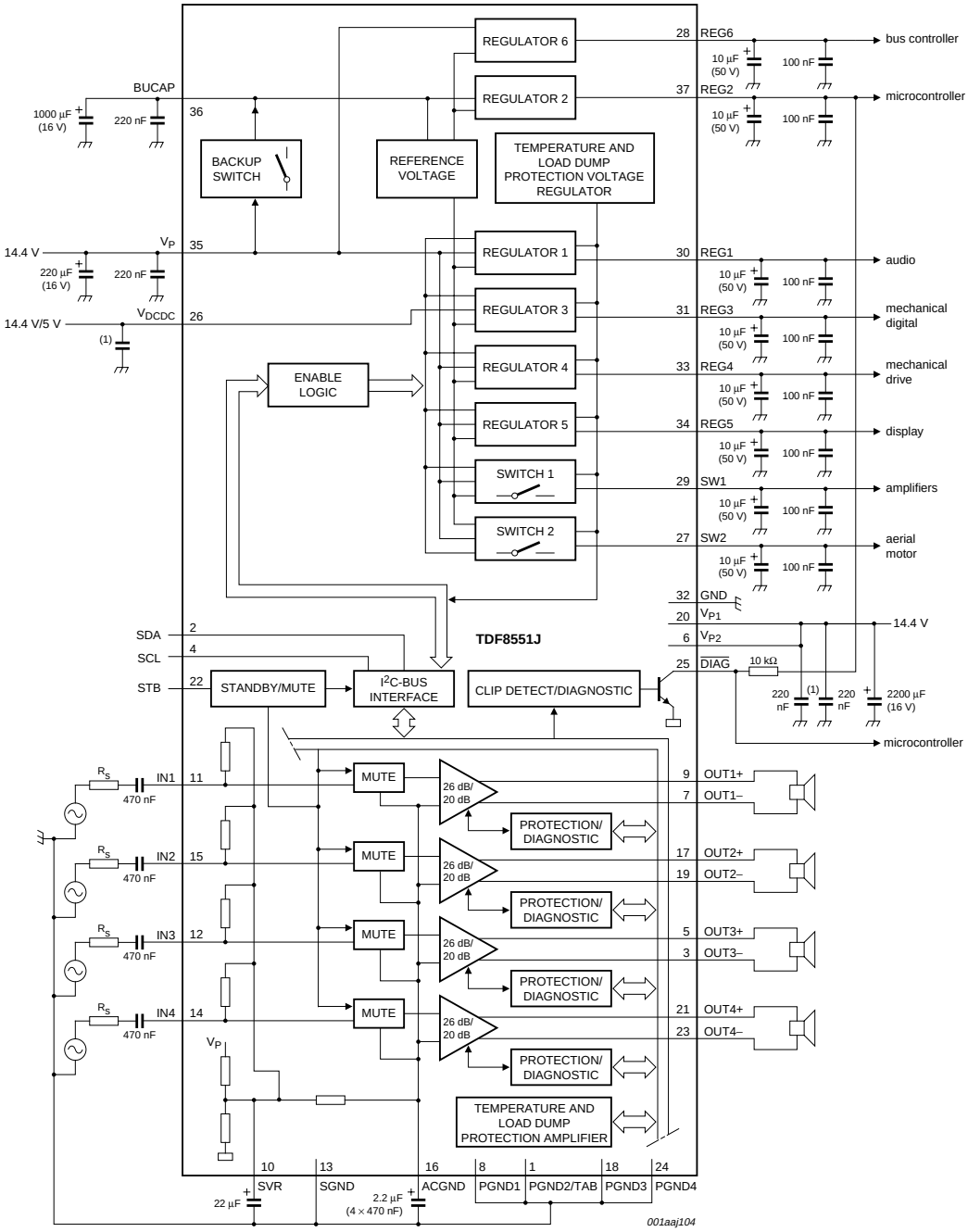
V_P = 14.4 V.

R_L = 4 Ω.

f = 1 kHz.

Fig 25. Amplifier efficiency as a function of output power; all channels driven

12. Application information



(1) See Section 12.1.

The value of ACGND capacitor must be close to 4 × the value of capacitor connected to the positive input of each channel; for EMC reasons a 10 nF capacitor can be connected between each amplifier output and ground.

Fig 26. Test and application diagram of TDF8551J

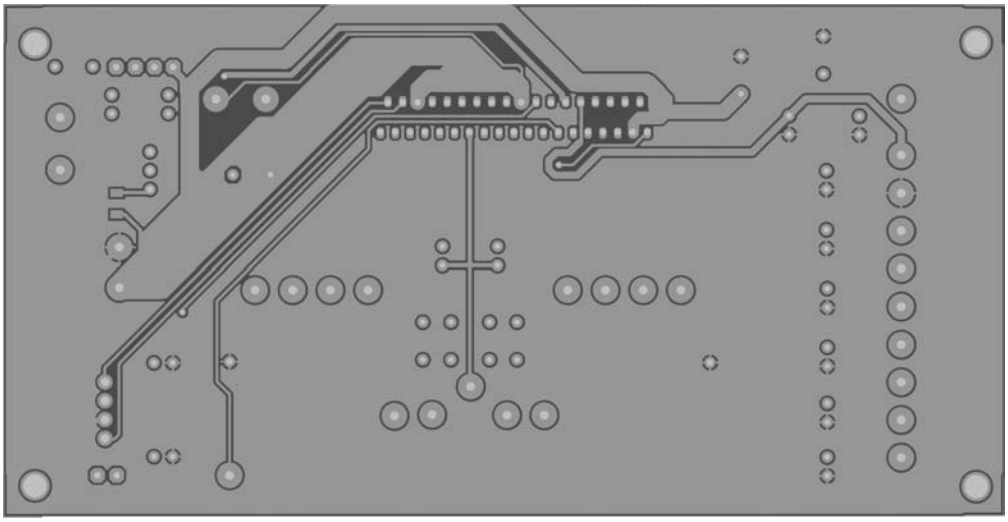
12.1 Supply decoupling

See Figure 26 to Figure 30.

The high frequency 220 nF decoupling capacitors connected to power supply voltage pins 6 and 20 should be located as close as possible to these pins.

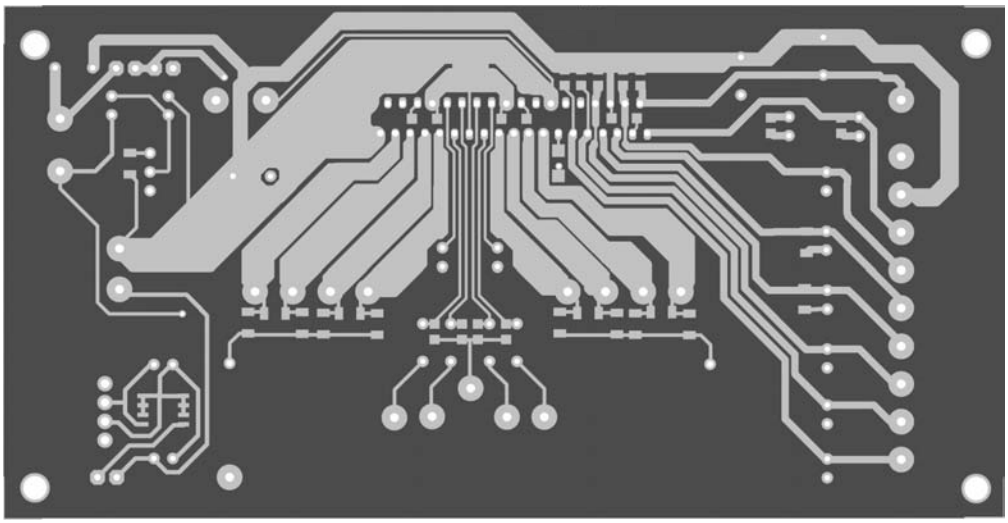
It is important to use good quality capacitors. These capacitors should be able to suppress high voltage peaks that can occur on the power supply if several audio channels are accidentally shorted to the power supply simultaneously, due to the activation of current protection. Good results have been achieved using 0805 case-size capacitors (X7R material, 220 nF) located close to power supply voltage pins 6 and 20.

If a DC-to-DC converter is used to supply regulator 3, the recommendations of the converter manufacturer relating to decoupling must be followed.



001aai763

Fig 27. Printed-circuit board layout of test and application circuit showing top copper layer viewed from top



001aai762

Fig 28. Printed-circuit board layout of test and application circuit showing bottom copper layer viewed from top

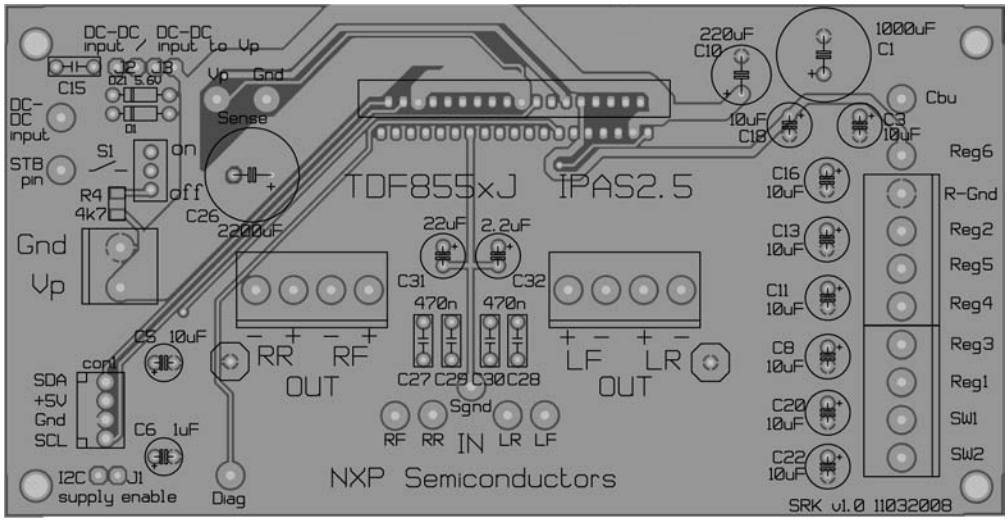


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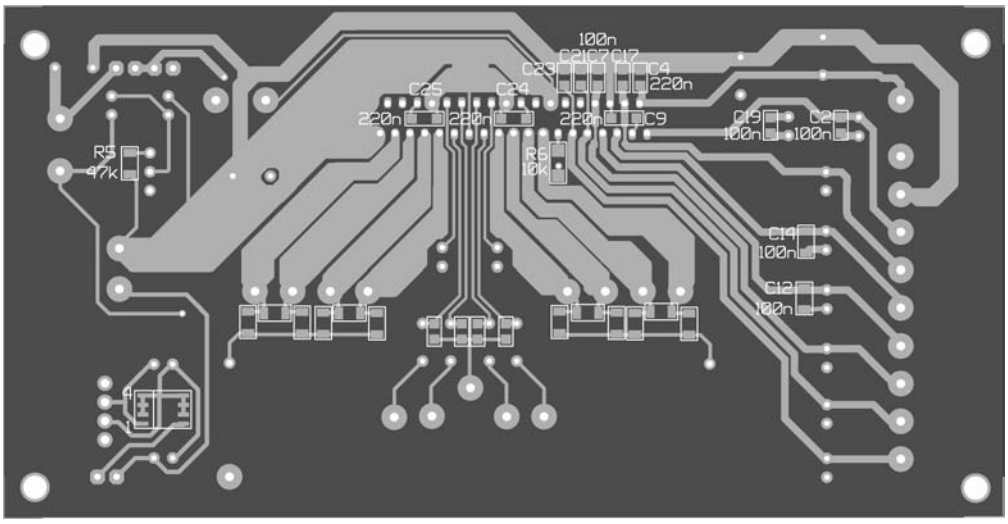
Fig 29. Printed-circuit board layout of test and application circuit showing components and top copper layout viewed from top



001aai765

Fig 30. Printed-circuit board layout of test and application circuit showing components and bottom copper layout viewed from top

12.2 Beep input circuit

Beep input circuit to amplify the beep signal from the microcontroller to all 4 amplifiers (gain = 0 dB). Note that this circuit will not affect amplifier performance.

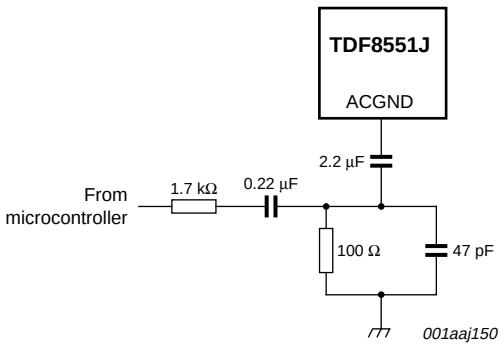


Fig 31. Application diagram for beep input

12.3 Noise

The outputs of regulators 1 to 6 are designed to give very low noise with good stability. The noise output voltage depends on output capacitor C_o. Table 17 shows the effect of the output capacitor on the noise figure.

Table 17. Regulator noise figures

Regulator	Noise figure (µV) [1]		
	C_o = 10 µF	C_o = 47 µF	C_o = 100 µF
1	225	180	145
2	700	600	390
3	100	85	65
4	235	205	175
5	315	285	225
6	710	550	340

[1] Measured in the frequency range 20 Hz to 80 kHz; at $I_{O(reg)}$ = 10 mA.

12.4 Stability

The regulators are made stable by connecting capacitors to the regulator outputs. The stability can be guaranteed with almost any output capacitor if its Equivalent Series Resistance (ESR) stays below the ESR curve shown in Figure 32. If an electrolytic capacitor is used, its behavior with temperature can cause oscillations at extremely low temperature. Oscillation problems can be avoided by adding a 47 nF capacitor in parallel with the electrolytic capacitor. The following example describes how to select the value of output capacitor.

12.4.1 Example regulator 2

Regulator 2 is stabilized with an electrolytic output capacitor of 10 µF which has an ESR of 4 Ω. At T_{amb} = −30 °C the capacitor value decreases to 3 µF and its ESR increases to 28 Ω which is above the maximum allowed as shown in Figure 32, and which will make the regulator unstable. To avoid problems with stability at low temperatures, the recommended solution is to use tantalum capacitors. Either use a tantalum capacitor of 10 µF, or an electrolytic capacitor with a higher value.

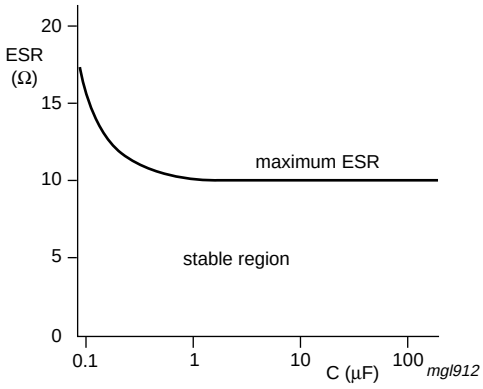
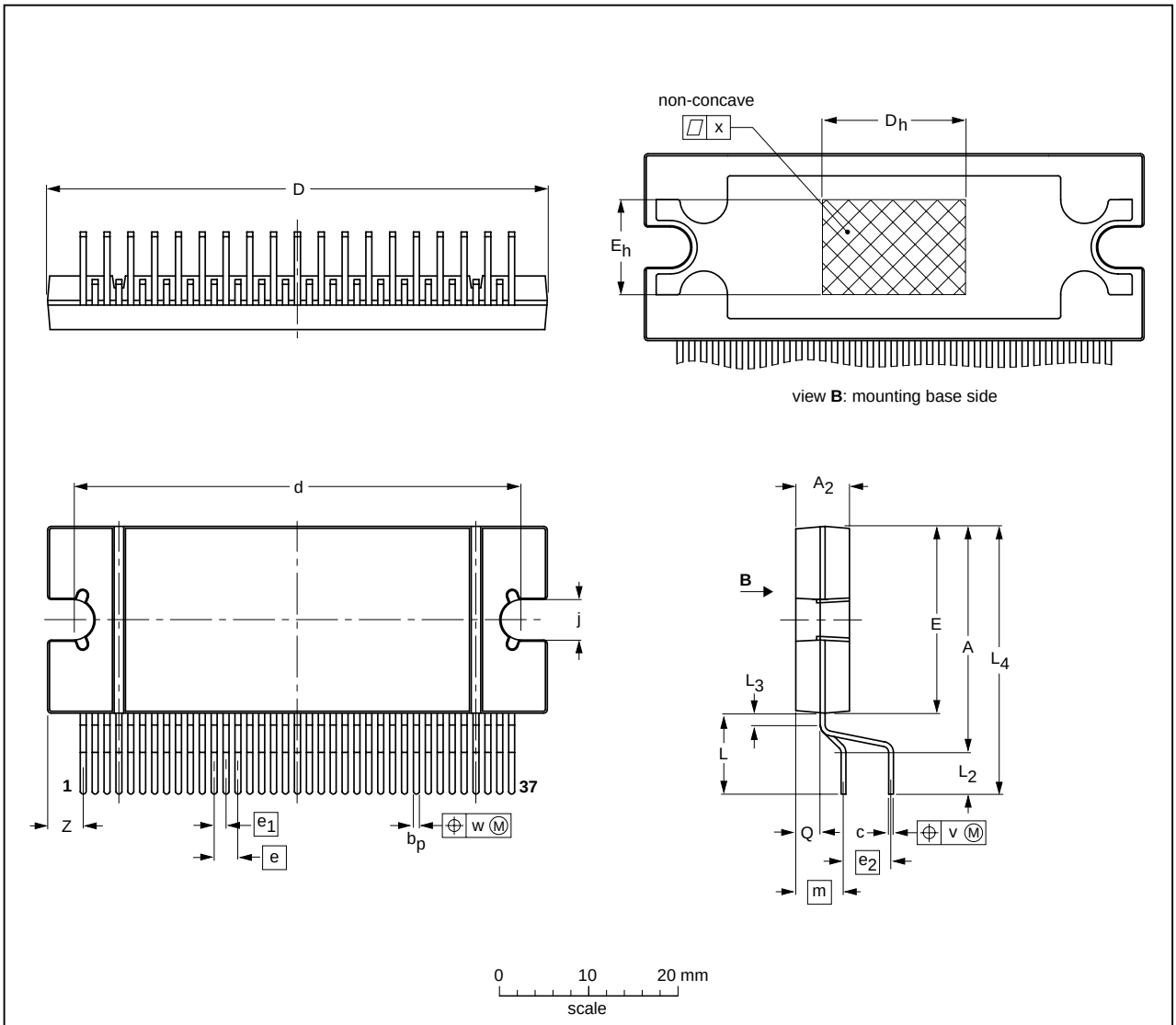


Fig 32. Curve for selecting the value of output capacitors for regulators 1 to 6

13. Package outline

DBS37P: plastic DIL-bent-SIL power package; 37 leads (lead length 6.8 mm) **SOT725-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_2	b_p	c	$D^{(1)}$	d	D_h	$E^{(1)}$	e	e_1	e_2	E_h	j	L	L_2	L_3	L_4	m	Q	v	w	x	$Z^{(1)}$
mm	19	4.65 4.35	0.60 0.45	0.5 0.3	42.2 41.7	37.8 37.4	12	15.9 15.5	2	1	4	8	3.4 3.1	6.8	3.9 3.1	1.15 0.85	22.9 22.1	4	2.1 1.8	0.6	0.25	0.03	3.30 2.65

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT725-1	- - -	- - -	- - -			~~01-11-14~~ 02-11-22

Fig 33. Package outline SOT725-1 (DBS37P)

14. Soldering of through-hole mount packages

14.1 Introduction to soldering through-hole mount packages

This text gives a very brief insight into wave, dip and manual soldering.

Wave soldering is the preferred method for mounting of through-hole mount IC packages on a printed-circuit board.

14.2 Soldering by dipping or by solder wave

Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing. Typical dwell time of the leads in the wave ranges from 3 seconds to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg(max)}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

14.3 Manual soldering

Apply the soldering iron (24 V or less) to the lead(s) of the package, either below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 °C and 400 °C, contact may be up to 5 seconds.

14.4 Package related soldering information

Table 18. Suitability of through-hole mount IC packages for dipping and wave soldering

Package	Soldering method	
	Dipping	Wave
CPGA, HCPGA	-	suitable
DBS, DIP, HDIP, RDBS, SDIP, SIL	suitable	suitable[1]
PMFP[2]	-	not suitable

[1] For SDIP packages, the longitudinal axis must be parallel to the transport direction of the printed-circuit board.

[2] For PMFP packages hot bar soldering or manual soldering is suitable.

15. Abbreviations

Table 19. Abbreviations

Acronym	Description
BCDMOS	Bipolar Complementary Double-diffused Metal-Oxide Semiconductor
DSP	Digital Signal Processor
EMC	ElectroMagnetic Compatibility
LSB	Least Significant Bit
MSB	Most Significant Bit
POR	Power-On Reset

16. Revision history

Table 20. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TDF8551J_2	20090818	Product data sheet	-	TDF8551J_1
Modifications:	• Table 16 “Characteristics” changed minimum output current (I_O) regulator 3 pin REG3.			
TDF8551J_1	20081202	Preliminary data sheet	-	-

17. Legal information

17.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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19. Contents

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