N-Channel 75-V (D-S) 200°C MOSFET

CHARACTERISTICS

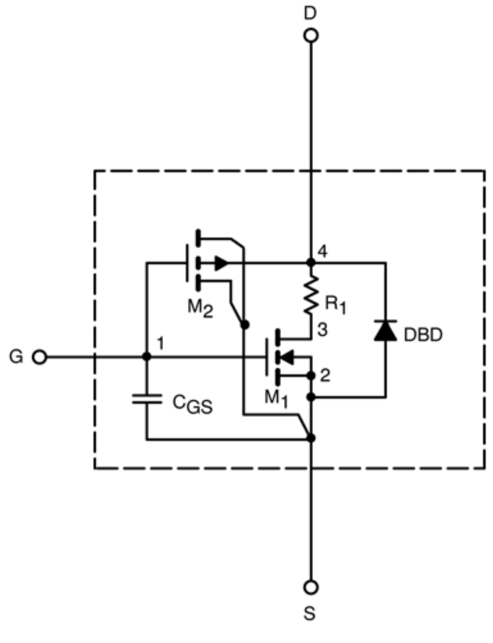
- N-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the −55 to 125°C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

DESCRIPTION

The attached spice model describes the typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model is extracted and optimized over the −55 to 125°C temperature ranges under the pulsed 0 to 10V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

SUBCIRCUIT MODEL SCHEMATIC



SPICE Device Model SUM110N08-05

Vishay Siliconix

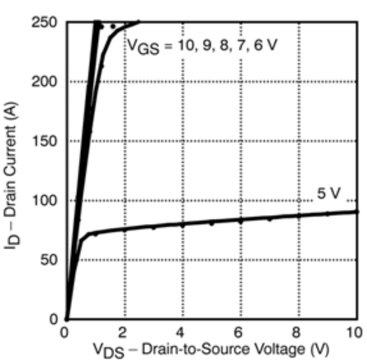
SPECIFICATIONS (T_J = 25°C UNLESS OTHERWISE NOTED)

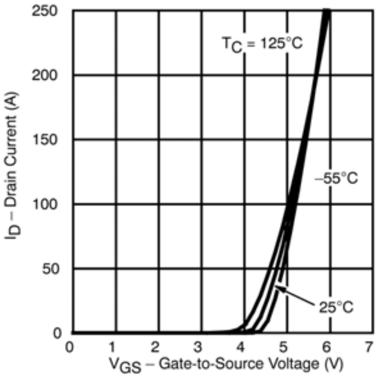
Parameter	Symbol	Test Conditions	Simulated Data	Measured Data	Unit
Static					
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\ \mu A$	3.1		V
On-State Drain Current[a]	$I_{D(on)}$	$V_{DS} > 5$ V, $V_{GS} = 10$ V	1197		A
Drain-Source On-State Resistance[a]	$r_{DS(on)}$	$V_{GS} = 10$ V, $I_D = 30$ A	0.0038	0.0038	Ω
		$V_{GS} = 10$ V, $I_D = 30$ A, $T_J = 125°C$	0.0063		
		$V_{GS} = 10$ V, $I_D = 30$ A, $T_J = 200°C$	0.0084		
Forward Transconductance[a]	g_{fs}	$V_{DS} = 15$ V, $I_D = 30$ A	109		S
Forward Voltage [a]	V_{SD}	$I_S = 110$ A, $V_{GS} = 0$ V	0.92	1	V
Dynamic [b]					
Input Capacitance	C_{iss}	$V_{GS} = 0$ V, $V_{DS} = 25$ V, f = 1 MHz	7663	7900	Pf
Output Capacitance	C_{oss}		936	950	
Reverse Transfer Capacitance	C_{rss}		406	550	
Total Gate Charge[c]	Q_g	$V_{DS} = 35$ V, $V_{GS} = 10$ V, $I_D = 110$ A	139	145	NC
Gate-Source Charge[c]	Q_{gs}		36	30	
Gate-Drain Charge[c]	Q_{gd}		45	45	
Turn-On Delay Time [c]	$t_{d(on)}$	$V_{DD} = 35$ V, $R_L = 0.40\ \Omega$ $I_D \cong 110$ A, $V_{GEN} = 10$ V, $R_G = 2.5\ \Omega$	88	25	Ns
Rise Time [c]	t_r		110	200	
Turn-Off Delay Time [c]	$t_{d(off)}$		130	65	
Fall Time [c]	t_f		149	165	
Reverse Recovery Time	t_{rr}	$I_F = 85$ A, di/dt = 100 A/µs	55	80	

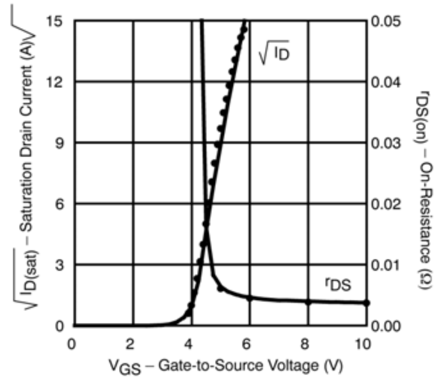
Notes:

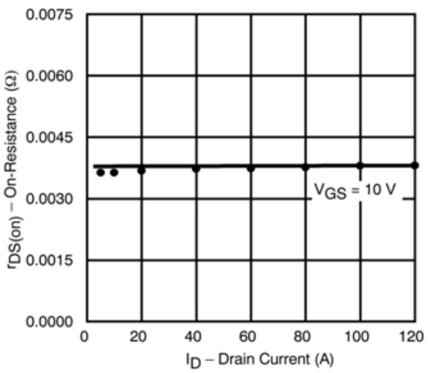
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.
c. Independent of operating temperature.

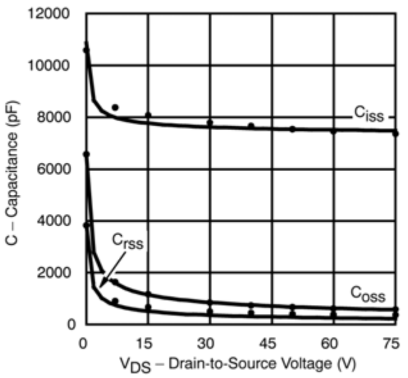
COMPARISON OF MODEL WITH MEASURED DATA (T_J=25°C UNLESS OTHERWISE NOTED)

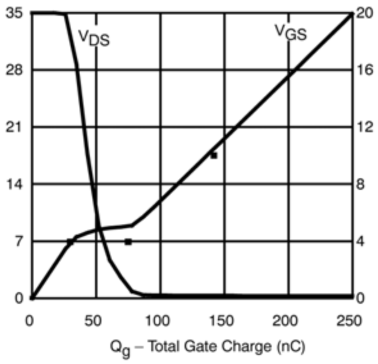












Note: Dots and squares represent measured data.