

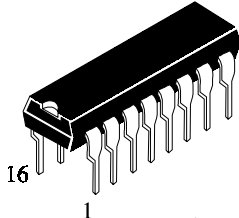
IN74HC175

Quad D Flip-Flop with  
Common Clock and Reset  
High-Performance Silicon-Gate CMOS

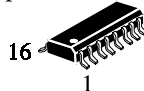
The IN74HC175 is identical in pinout to the LS/ALS175. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LS/ALSTTL outputs.

This device consists of four D flip-flops with common Reset and Clock inputs, and separate D inputs. Reset (active-low) is asynchronous and occurs when a low level is applied to the Reset input. Information at a D input is transferred to the corresponding Q output on the next positive-going edge of the Clock input.

- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices



N SUFFIX  
PLASTIC



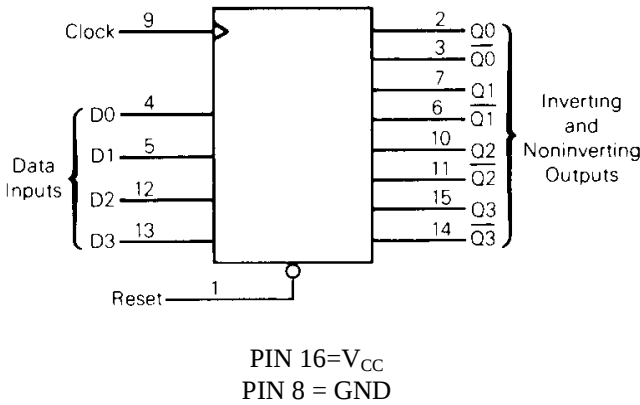
D SUFFIX  
SOIC

**ORDERING INFORMATION**  
IN74HC175N Plastic  
IN74HC175D SOIC  
 $T_A = -55^\circ$  to  $125^\circ$  C for all packages

PIN ASSIGNMENT

|                 |   |    |                 |
|-----------------|---|----|-----------------|
| RESET           | 1 | 16 | $V_{CC}$        |
| Q0              | 2 | 15 | Q3              |
| $\overline{Q0}$ | 3 | 14 | $\overline{Q3}$ |
| D0              | 4 | 13 | D3              |
| D1              | 5 | 12 | D2              |
| $\overline{Q1}$ | 6 | 11 | $\overline{Q2}$ |
| Q1              | 7 | 10 | Q2              |
| GND             | 8 | 9  | CLOCK           |

LOGIC DIAGRAM



FUNCTION TABLE

| Inputs |                                                                                       |   | Outputs   |                |
|--------|---------------------------------------------------------------------------------------|---|-----------|----------------|
| Reset  | Clock                                                                                 | D | Q         | $\overline{Q}$ |
| L      | X                                                                                     | X | L         | H              |
| H      |  | H | H         | L              |
| H      |  | L | L         | H              |
| H      | L                                                                                     | X | no change |                |

X = Don't care

**MAXIMUM RATINGS\***

| Symbol    | Parameter                                                                        | Value                  | Unit |
|-----------|----------------------------------------------------------------------------------|------------------------|------|
| $V_{CC}$  | DC Supply Voltage (Referenced to GND)                                            | -0.5 to +7.0           | V    |
| $V_{IN}$  | DC Input Voltage (Referenced to GND)                                             | -1.5 to $V_{CC} + 1.5$ | V    |
| $V_{OUT}$ | DC Output Voltage (Referenced to GND)                                            | -0.5 to $V_{CC} + 0.5$ | V    |
| $I_{IN}$  | DC Input Current, per Pin                                                        | $\pm 20$               | mA   |
| $I_{OUT}$ | DC Output Current, per Pin                                                       | $\pm 25$               | mA   |
| $I_{CC}$  | DC Supply Current, $V_{CC}$ and GND Pins                                         | $\pm 50$               | mA   |
| $P_D$     | Power Dissipation in Still Air, Plastic DIP+<br>SOIC Package+                    | 750<br>500             | mW   |
| Tstg      | Storage Temperature                                                              | -65 to +150            | °C   |
| $T_L$     | Lead Temperature, 1 mm from Case for 10 Seconds<br>(Plastic DIP or SOIC Package) | 260                    | °C   |

\*Maximum Ratings are those values beyond which damage to the device may occur.  
Functional operation should be restricted to the Recommended Operating Conditions.

+Derating - Plastic DIP: - 10 mW/°C from 65° to 125°C  
SOIC Package: : - 7 mW/°C from 65° to 125°C

**RECOMMENDED OPERATING CONDITIONS**

| Symbol            | Parameter                                            | Min | Max      | Unit |
|-------------------|------------------------------------------------------|-----|----------|------|
| $V_{CC}$          | DC Supply Voltage (Referenced to GND)                | 2.0 | 6.0      | V    |
| $V_{IN}, V_{OUT}$ | DC Input Voltage, Output Voltage (Referenced to GND) | 0   | $V_{CC}$ | V    |
| $T_A$             | Operating Temperature, All Package Types             | -55 | +125     | °C   |
| $t_r, t_f$        | Input Rise and Fall Time (Figure 1)                  |     |          |      |
|                   | $V_{CC} = 2.0\text{ V}$                              | 0   | 1000     | ns   |
|                   | $V_{CC} = 4.5\text{ V}$                              | 0   | 500      |      |
|                   | $V_{CC} = 6.0\text{ V}$                              | 0   | 400      |      |

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{IN}$  and  $V_{OUT}$  should be constrained to the range  $GND \leq (V_{IN} \text{ or } V_{OUT}) \leq V_{CC}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or  $V_{CC}$ ). Unused outputs must be left open.

**DC ELECTRICAL CHARACTERISTICS**(Voltages Referenced to GND)

| Symbol          | Parameter                                      | Test Conditions                                                                                                        | V <sub>CC</sub><br>V | Guaranteed Limit     |                    |                    | Unit |
|-----------------|------------------------------------------------|------------------------------------------------------------------------------------------------------------------------|----------------------|----------------------|--------------------|--------------------|------|
|                 |                                                |                                                                                                                        |                      | 25 °C<br>to<br>-55°C | ≤85<br>°C          | ≤125<br>°C         |      |
| V <sub>IH</sub> | Minimum High-Level Input Voltage               | V <sub>OUT</sub> =0.1 V or V <sub>CC</sub> -0.1 V<br>  I <sub>OUT</sub>   ≤ 20 µA                                      | 2.0<br>4.5<br>6.0    | 1.5<br>3.15<br>4.2   | 1.5<br>3.15<br>4.2 | 1.5<br>3.15<br>4.2 | V    |
| V <sub>IL</sub> | Maximum Low - Level Input Voltage              | V <sub>OUT</sub> =0.1 V or V <sub>CC</sub> -0.1 V<br>  I <sub>OUT</sub>   ≤ 20 µA                                      | 2.0<br>4.5<br>6.0    | 0.3<br>0.9<br>1.2    | 0.3<br>0.9<br>1.2  | 0.3<br>0.9<br>1.2  | V    |
| V <sub>OH</sub> | Minimum High-Level Output Voltage              | V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub><br>  I <sub>OUT</sub>   ≤ 20 µA                                    | 2.0<br>4.5<br>6.0    | 1.9<br>4.4<br>5.9    | 1.9<br>4.4<br>5.9  | 1.9<br>4.4<br>5.9  | V    |
|                 |                                                | V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub><br>  I <sub>OUT</sub>   ≤ 4.0 mA<br>  I <sub>OUT</sub>   ≤ 5.2 mA  | 4.5<br>6.0           | 3.98<br>5.48         | 3.84<br>5.34       | 3.7<br>5.2         |      |
| V <sub>OL</sub> | Maximum Low-Level Output Voltage               | V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub><br>  I <sub>OUT</sub>   ≤ 20 µA                                   | 2.0<br>4.5<br>6.0    | 0.1<br>0.1<br>0.1    | 0.1<br>0.1<br>0.1  | 0.1<br>0.1<br>0.1  | V    |
|                 |                                                | V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub><br>  I <sub>OUT</sub>   ≤ 4.0 mA<br>  I <sub>OUT</sub>   ≤ 5.2 mA | 4.5<br>6.0           | 0.26<br>0.26         | 0.33<br>0.33       | 0.4<br>0.4         |      |
| I <sub>IN</sub> | Maximum Input Leakage Current                  | V <sub>IN</sub> =V <sub>CC</sub> or GND                                                                                | 6.0                  | ±0.1                 | ±1.0               | ±1.0               | µA   |
| I <sub>CC</sub> | Maximum Quiescent Supply Current (per Package) | V <sub>IN</sub> =V <sub>CC</sub> or GND<br>I <sub>OUT</sub> =0µA                                                       | 6.0                  | 8.0                  | 80                 | 160                | µA   |

**AC ELECTRICAL CHARACTERISTICS**( $C_L=50\text{pF}$ , Input  $t_r=t_f=6.0\text{ ns}$ )

| Symbol             | Parameter                                                               | V <sub>CC</sub><br>V | Guaranteed Limit     |                 |                 | Unit |
|--------------------|-------------------------------------------------------------------------|----------------------|----------------------|-----------------|-----------------|------|
|                    |                                                                         |                      | 25 °C<br>to<br>-55°C | ≤85°C           | ≤125°C          |      |
| $f_{\max}$         | Maximum Clock Frequency (50% Duty Cycle)<br>(Figures 1 and 4)           | 2.0<br>4.5<br>6.0    | 6.0<br>30<br>35      | 4.8<br>24<br>28 | 4.0<br>20<br>24 | MHz  |
| $t_{PLH}, t_{PHL}$ | Maximum Propagation Delay, Clock to Q or $\bar{Q}$<br>(Figures 1 and 4) | 2.0<br>4.5<br>6.0    | 150<br>30<br>26      | 190<br>38<br>33 | 225<br>45<br>38 | ns   |
| $t_{PHL}, t_{PLH}$ | Maximum Propagation Delay, Reset to Q or $\bar{Q}$<br>(Figures 2 and 4) | 2.0<br>4.5<br>6.0    | 125<br>25<br>21      | 155<br>31<br>26 | 190<br>38<br>32 | ns   |
| $t_{TLH}, t_{THL}$ | Maximum Output Transition Time, Any Output<br>(Figures 1 and 4)         | 2.0<br>4.5<br>6.0    | 75<br>15<br>13       | 95<br>19<br>16  | 110<br>22<br>19 | ns   |
| $C_{IN}$           | Maximum Input Capacitance                                               | -                    | 10                   | 10              | 10              | pF   |

|                 |                                                                                                                                                         |                                      |    |
|-----------------|---------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------|----|
| C <sub>PD</sub> | Power Dissipation Capacitance (Per Flip-Flop)                                                                                                           | Typical @25°C,V <sub>CC</sub> =5.0 V | pF |
|                 | Used to determine the no-load dynamic power consumption: P <sub>D</sub> =C <sub>PD</sub> V <sub>CC</sub> <sup>2</sup> f+I <sub>CC</sub> V <sub>CC</sub> | 35                                   |    |

**TIMING REQUIREMENTS** ( $C_L=50\text{pF}$ , Input  $t_r=t_f=6.0\text{ ns}$ )

| Symbol     | Parameter                                                       | V <sub>CC</sub><br>V | Guaranteed Limit   |                    |                    | Unit |
|------------|-----------------------------------------------------------------|----------------------|--------------------|--------------------|--------------------|------|
|            |                                                                 |                      | 25 °C to<br>-55°C  | ≤85°C              | ≤125°C             |      |
| $t_{SU}$   | Minimum Setup Time, Data to<br>Clock (Figure 3)                 | 2.0<br>4.5<br>6.0    | 100<br>20<br>17    | 125<br>25<br>21    | 150<br>30<br>26    | ns   |
| $t_h$      | Minimum Hold Time, Clock<br>to Data (Figure 3)                  | 2.0<br>4.5<br>6.0    | 3<br>3<br>3        | 3<br>3<br>3        | 3<br>3<br>3        | ns   |
| $t_{rec}$  | Minimum Recovery Time,<br>Reset Inactive to Clock<br>(Figure 2) | 2.0<br>4.5<br>6.0    | 100<br>20<br>17    | 125<br>25<br>21    | 150<br>30<br>26    | ns   |
| $t_w$      | Minimum Pulse Width, Clock<br>(Figure 1)                        | 2.0<br>4.5<br>6.0    | 80<br>16<br>14     | 100<br>20<br>17    | 120<br>24<br>20    | ns   |
| $t_w$      | Minimum Pulse Width, Reset<br>(Figure 2)                        | 2.0<br>4.5<br>6.0    | 80<br>16<br>14     | 100<br>20<br>17    | 120<br>24<br>20    | ns   |
| $t_r, t_f$ | Maximum Input Rise and Fall<br>Times (Figure 1)                 | 2.0<br>4.5<br>6.0    | 1000<br>500<br>400 | 1000<br>500<br>400 | 1000<br>500<br>400 | ns   |

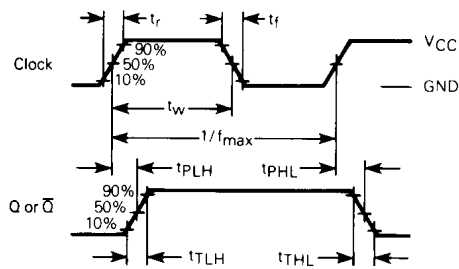


Figure 1. Switching Waveforms

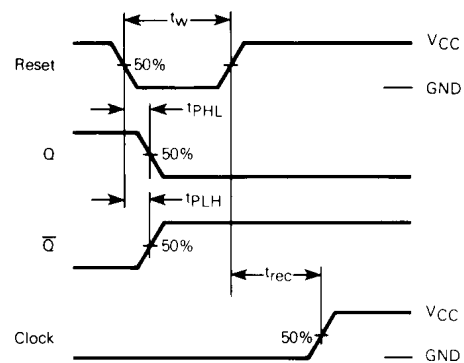


Figure 2. Switching Waveforms

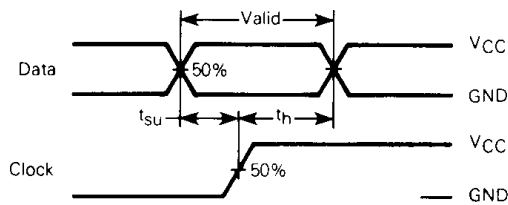
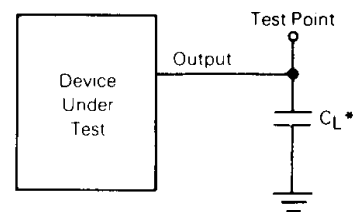


Figure 3. Switching Waveforms



\* Includes all probe and jig capacitance.

Figure 4. Test Circuit

## EXPANDED LOGIC DIAGRAM

