# UCC2912
# UCC3912
# PROGRAMMABLE HOT SWAP POWER MANAGER

SLUS241D − MARCH 1994 - REVISED NOVEMBER 2003

- **Integrated 0.15-Ω Power MOSFET**
- **3-V to 8-V Operation**
- **Digital Programmable Current Limit from 0 A to 3 A**
- **Electronic Circuit Breaker Function**
- **1μA $I_{CC}$ When Disabled**
- **Programmable On-Time**
- **Programmable Start Delay**
- **Fixed 3% Duty Cycle**
- **Unidirectional Switch**
- **Thermal Shutdown**
- **Fault-Output Indicator**
- **Maximum-Output Current Can Be Set to 1 A Above the Programmed Fault Level or to a Full 4 A**
- **Power SOIC, Low-Thermal Resistance Packaging**

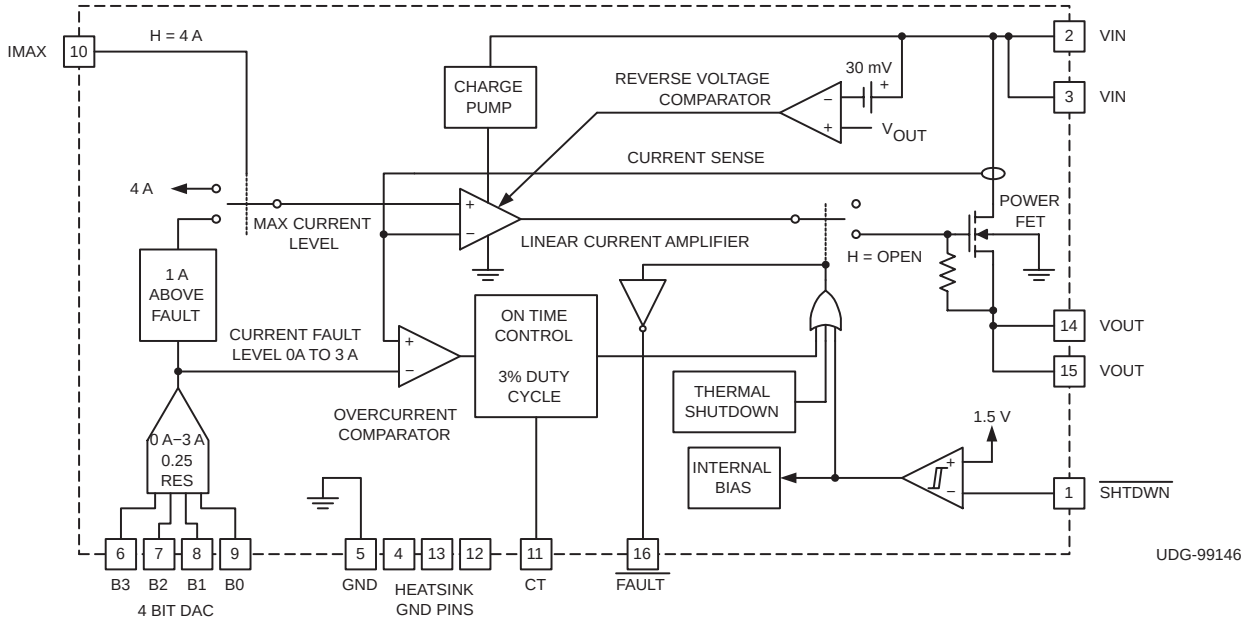
## description

The UCC3912 family of hot swap power managers provides complete power management, hot swap capability, and circuit breaker functions. The only component required to operate the device, other than supply bypassing, is the fault timing capacitor, $C_T$. All control and housekeeping functions are integrated, and externally programmable. These include the fault current level, maximum output-sourcing current, maximum fault time, and startup delay. In the event of a constant fault, the internal fixed 3% duty cycle ratio limits average output power.

The internal 4-bit DAC allows programming of the fault level current from 0 A to 3 A with 0.25-A resolution. The IMAX control pin sets the maximum sourcing current to 1 A above the fault level when driven low, and to a full 4 A when driven high for applications which require fast output capacitor charging.

When the output current is below the fault level, the output MOSFET is switched on with a nominal on resistance of 0.15 Ω. When the output current exceeds the fault level, but is less than the maximum sourcing level, the output remains switched on, but the fault timer starts charging $C_T$. Once $C_T$ charges to a preset threshold, the switch is turned off, and remains off for 30 times the programmed fault time. When the output current reaches the maximum sourcing level, the MOSFET transitions from a switch to a constant current source. (continued)

## block diagram

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## description (continued)

The UCC3912 family is designed for unidirectional current flow, emulating an ideal diode in series with the power switch. This feature is particularly attractive in applications where many devices are powering a common bus, such as with SCSI Termpwr.

The UCC3912 family can be put into sleep mode drawing only 1-μA of supply current. The $\overline{\text{SHTDWN}}$ pin has a preset threshold hysteresis which allows the user the ability to set a time delay upon startup to achieve sequencing of power. Other features include an open drain $\overline{\text{FAULT}}$ output indicator, thermal shutdown, under voltage lockout, and a low thermal resistance small outline package.

## absolute maximum ratings over operating free-air temperature (unless otherwise noted)†‡

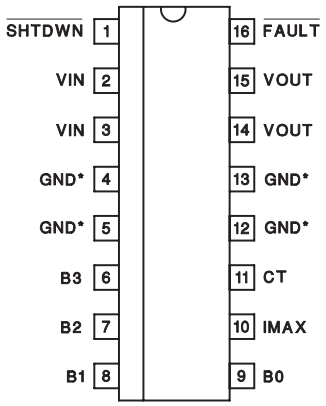
| | |
|---|---|
| VIN | 8 V |
| $\overline{\text{FAULT}}$ sink current | 50 mA |
| $\overline{\text{FAULT}}$ voltage | -0.3 to $V_{IN}$ |
| Output current | Self Limiting |
| Input voltage (B0, B1, B2, B3, IMAX, $\overline{\text{SHTDWN}}$) | -0.3 to $V_{IN}$ |
| Storage temperature range, $T_{stg}$ | -65°C to 150°C |
| Operating junction temperature range, $T_J$ | -55°C to 150°C |
| Lead temperature (soldering, 10 sec.) | 300°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

‡ Currents are positive into, negative out of the specified terminal. Consult Packaging Section of the Interface Products Data book (TI Literature Number SLUD002) for thermal limitations and considerations of packages.

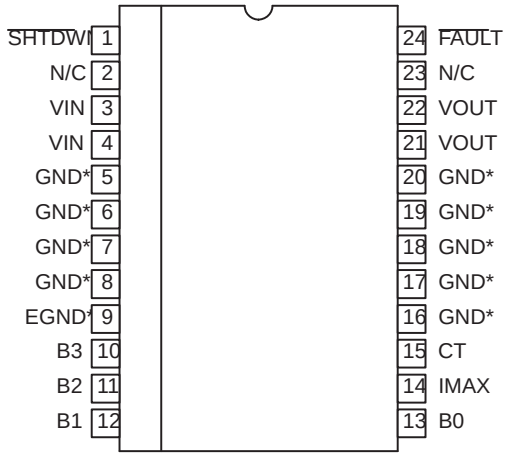
## package information

**DIL-16, SOIC-16**
**N, DP Package**
**(TOP VIEW)**




*Pin 5 serves as lowest impedance to the electrical ground; Pins 4, 12, and 13 serve as heat sink/ground. These pins should be connected to large etch areas to help dissipate heat. For N package, pins 4, 12, and 13 are N/C.

**TSSOP-24,**
**PWP Package**
**(TOP VIEW)**




*Pin 9 serves as lowest impedance to the electrical ground; other GND pins serve as heat sink/ground. These pins should be connected to large etch areas to help dissipate heat.

## electrical characteristics, these specifications apply for $T_A$ = −40°C to 85°C for the UCC2912; $T_A$ = 0°C to 70°C for the UCC3912, VIN = 5 V, IMAX = 0.4 V, $\overline{SHTDWN}$ = 2.4 V (unless otherwise stated)

### supply section

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| Voltage input range | | 3.0 | | 8.0 | V |
| Supply current | | | 1.0 | 2.0 | mA |
| Sleep mode current | $\overline{SHTDWN}$ = 0.2 V | | 0.5 | 5.0 | µA |

NOTE 1: All voltages are with respect to ground. Current is positive into and negative out of the specified terminal.

### output section

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| Voltage drop | $I_{OUT}$ = 1 A | | 0.15 | 0.22 | V |
| | $I_{OUT}$ = 2 A | | 0.3 | 0.45 | V |
| | $I_{OUT}$ = 3 A | | 0.45 | 0.68 | V |
| | $I_{OUT}$ = 1A, VIN = 3 V | | 0.17 | 0.27 | V |
| | $I_{OUT}$ = 2 A, VIN = 3 V | | 0.35 | 0.56 | V |
| | $I_{OUT}$ = 3 A, VIN = 3 V | | 0.5 | 0.8 | V |
| Reverse leakage current | $V_{IN} < V_{OUT}$ , $\overline{SHTDWN}$ = 0.2 V, $V_{OUT}$ = 5 V | | 5 | 20 | µA |
| Initial startup time | See Note 2 | | 100 | | µs |
| Short circuit response | See Note 2 | | 100 | | ns |
| Thermal shutdown | See Note 2 | | 170 | | °C |
| Thermal hysteresis | See Note 2 | | 10 | | °C |

NOTE 1: All voltages are with respect to ground. Current is positive into and negative out of the specified terminal.
NOTE 2: Ensured by design. Not production tested.

### DAC section

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Output leakage | | Code = 0000−0011 | | | 0 | 20 | µA |
| Trip current | | Code = 0100 | | 0.1 | 0.25 | 0.45 | A |
| | | Code = 0101 | | 0.25 | 0.50 | 0.75 | A |
| | | Code = 0110 | | 0.5 | 0.75 | 1.0 | A |
| | | Code = 0111 | | 0.75 | 1.00 | 1.25 | A |
| | | Code = 1000 | | 1.0 | 1.25 | 1.5 | A |
| | | Code = 1001 | | 1.25 | 1.50 | 1.75 | A |
| | | Code = 1010 | | 1.5 | 1.75 | 2.0 | A |
| | | Code = 1011 | | 1.7 | 2.00 | 2.3 | A |
| | | Code = 1100 | | 1.9 | 2.25 | 2.58 | A |
| | | Code = 1101 | | 2.1 | 2.50 | 2.9 | A |
| | | Code = 1110 | | 2.3 | 2.75 | 3.2 | A |
| | | Code = 1111 | | 2.5 | 3.0 | 3.5 | A |
| Maximum output current | | Code = 0000 to 0011 | | | | 0.02 | mA |
| Maximum output current over trip (current source mode) | UCC2912 | Code = 0100 to 1111, | $I_{MAX}$ = 0 V | 0.5 | 1.0 | 2.0 | A |
| | UCC3912 | Code = 0100 to 1111, | $I_{MAX}$ = 0 V | 0.5 | 1.0 | 1.8 | A |
| Maximum output current (current source mode) | | Code = 0100 to 1111, | $I_{MAX}$ = 2.4 V | 3.0 | 4.0 | 5.2 | A |

NOTE 1: All voltages are with respect to ground. Current is positive into and negative out of the specified terminal.

**electrical characteristics, these specifications apply for $T_A$ = −40°C to 85°C for the UCC2912; $T_A$ = 0°C to 70°C for the UCC3912, VIN = 5 V, IMAX = 0.4 V, $\overline{SHTDWN}$ = 2.4 V (unless otherwise stated)**

### timer section

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| CT charge current | | $V_{CT}$ = 1.0 V | −45.0 | -36.0 | −22.0 | µA |
| CT discharge current | UCC2912 | $V_{CT}$ = 1.0 V | 0.72 | 1.20 | 1.57 | µA |
| | UCC3912 | $V_{CT}$ = 1.0 V | 0.72 | 1.20 | 1.50 | µA |
| Output duty cycle | | $V_{OUT}$ = 0 V | 2.0 | 3.0 | 6.0 | % |
| CT fault threshold | | | 1.3 | 1.5 | 1.7 | V |
| CT reset threshold | | | 0.4 | 0.5 | 0.6 | V |

NOTE 1: All voltages are with respect to ground. Current is positive into and negative out of the specified terminal.

### shutdown section

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| Shutdown threshold | | 1.1 | 1.5 | 1.9 | V |
| Shutdown hysteresis | | | 100 | | mV |
| Input current | $\overline{SHTDWN}$ = 1 V | | 100 | 500 | nA |

### fault output section

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| Output leakage current | | | | 500 | nA |
| Low level output voltage | $I_{OUT}$ = 10 mA | | 0.4 | 0.8 | V |

### TTL input dc characteristics section

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| TTL input voltage high | (can be connected to $V_{IN}$) | 2.0 | | | V |
| TTL input voltage low | | | | 0.8 | V |
| TTL input high current | $V_{IH}$ = 2.4 V | | 3 | 10 | µA |
| TTL input low current | $V_{IL}$ = 0.4 V | | | 1 | µA |

NOTE 1: All voltages are with respect to ground. Current is positive into and negative out of the specified terminal.

## pin description

**B0−B3:** These pins provide digital input to the DAC which sets the fault current threshold. They can be used to provide a digital soft-start, adaptive current limiting.

**CT:** A capacitor connected to ground sets the maximum fault time. The maximum fault time must be more than the time to charge the external capacitance in one cycle. The maximum fault time is defined as FAULT = $27.8 \times 10^3 \times$ CT. Once the fault time is reached the output will shutdown for a time given by: $T_{SD} = 833 \times 10^3 \times$ CT, this equates to a 3% duty cycle.

**$\overline{FAULT}$:** Open drain output which pulls low upon any condition which causes the output to open: fault, thermal shutdown, or shutdown.

**IMAX:** When this pin is set to logic low the maximum sourcing current will always be 1 A above the programmed fault level. When set to logic high, the maximum sourcing current will be a constant 4 A for applications which require fast charging of load capacitance.

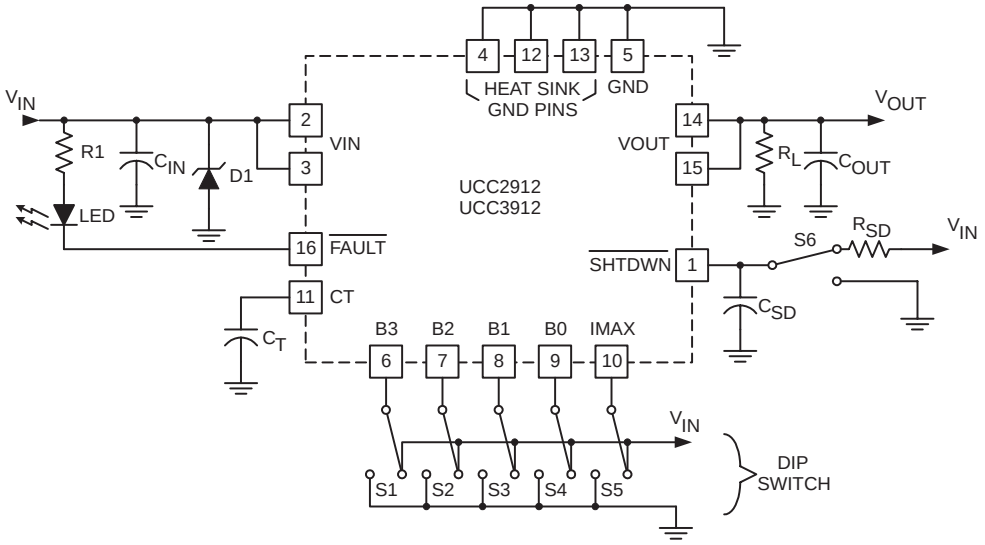
## pin description (continued)

**$\overline{\text{SHTDWN}}$:** When this pin is brought to a logic low, the IC is put into a sleep mode drawing typically less than 1 μA of $I_{CC}$. The input threshold is hysteretic, allowing the user to program a startup delay with an external RC circuit.

**VIN:** Input voltage to the UCC3912. The recommended voltage range is 3 V to 8 V. Both VIN pins should be connected together and to the power source.

**VOUT:** Output voltage from the UCC3912. When switched the output voltage will be approximately $V_{IN} - (0.15\ \Omega \times I_{OUT})$. Both VOUT pins should be connected together and to the load.

## APPLICATION INFORMATION




NOTE: For demonstration board schematic see Design Note DN-58 (TI Literature Number SLUA187).

UDG-99171

**Figure 1. Evaluation Circuit**

### protecting the UCC3912 from voltage transients

The parasitic inductance associated with the power distribution can cause a voltage spike at $V_{IN}$ if the load current is suddenly interrupted by the UCC3912. It is important to limit the peak of this spike to less than 8 V to prevent damage to the UCC3912. This voltage spike can be minimized by:

- Reducing the power distribution inductance (e.g., twist the positive and negative leads of the power supply feeding $V_{IN}$, locate the power supply close to the UCC3912, use a PCB ground plane,...etc.).
- Decoupling $V_{IN}$ with a capacitor, $C_{IN}$ (refer to Figure 1), located close to pins 2 and 3. This capacitor is typically less than 1 μF to limit the inrush current.
- Clamping the voltage at $V_{IN}$ below 8 V with a zener diode, D1 (refer to Figure 1), located close to pins 2 and 3.

## APPLICATION INFORMATION

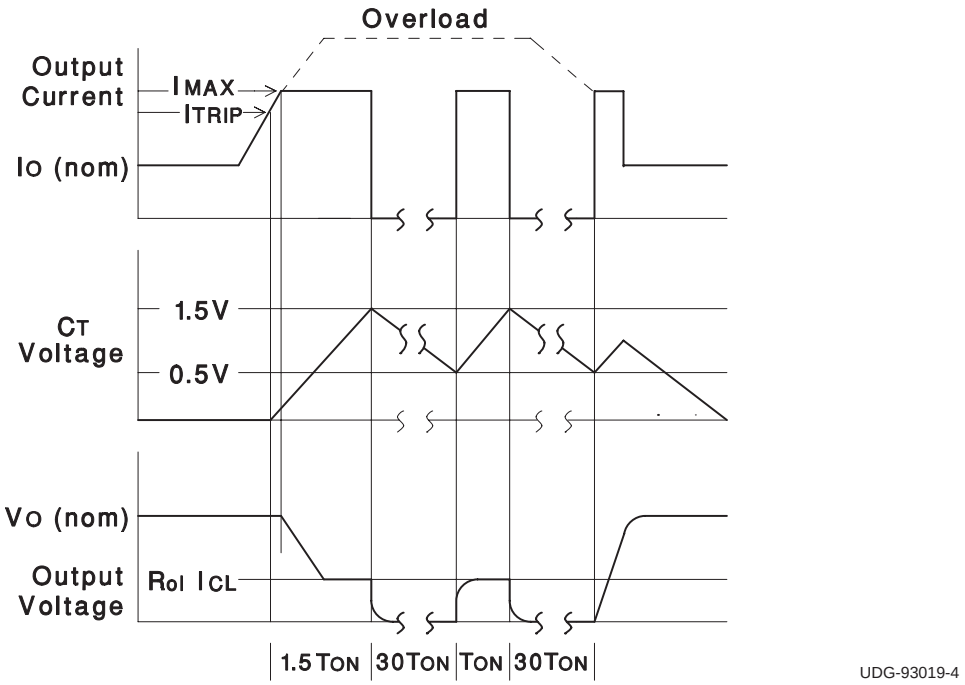



**Figure 2. Load Current, Timing-Capacitor Voltage, and Output Voltage of the UCC3912 Under Fault Conditions.**

### estimating maximum load capacitance

For hot-swap applications, the rate at which the total output capacitance can be charged depends on the maximum output current available and the nature of the load. For a constant-current current-limited controller, the output will come up if the load asks for less than the maximum available short-circuit current.

To ensure recovery of a duty-cycle from a short-circuited load condition, there is a maximum total output capacitance which can be charged for a given unit ON time (fault time). The design value of ON or fault time can be adjusted by changing the timing capacitor $C_T$.

For worst-case constant-current load of value just less than the trip limit; $C_{OUT(max)}$ can be estimated from:

$$C_{OUT(max)} \approx \left(I_{MAX} - I_{LOAD}\right) \times \left(\frac{28 \times 10^3 \times CT}{V_{OUT}}\right)$$

where $V_{OUT}$ is the output voltage.

## APPLICATION INFORMATION

For a resistive load of value RL, the value of $C_{OUT(max)}$ can be estimated from:

$$C_{OUT(max)} \approx \left( \frac{28 \times 10^3 \times CT}{RL \times \ell n \left( \frac{1}{1 - \left( \frac{V_{OUT}}{I_{MAX} \times RL} \right)} \right)} \right)$$

The overcurrent comparator senses both the DAC output and a representation of the output current. When the output current exceeds the programmed level the timing capacitor $C_T$ charges with 36 μA of current. If the fault occurs for the time it takes for $C_T$ to charge up to 1.5 V, the fault latch is set and the output switch is opened. The output remains opened until $C_T$ discharges to 0.5 V with a 1.2-μA current source. Once the 0.5 V is reached the output is enabled and will either appear as a switch, if the fault is removed, or a current source if the fault remains. If the over current condition is still present, then $C_T$ will begin charging, starting the cycle over, resulting in approximately a 3% on time.

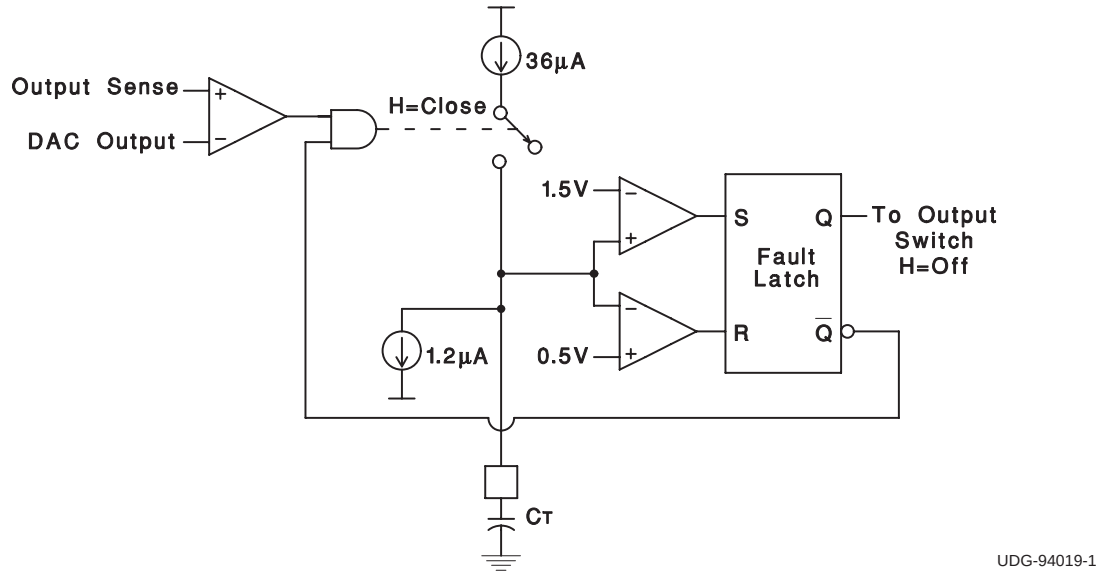



**Figure 3. UCC3912 On-Time Circuitry**

## APPLICATION INFORMATION

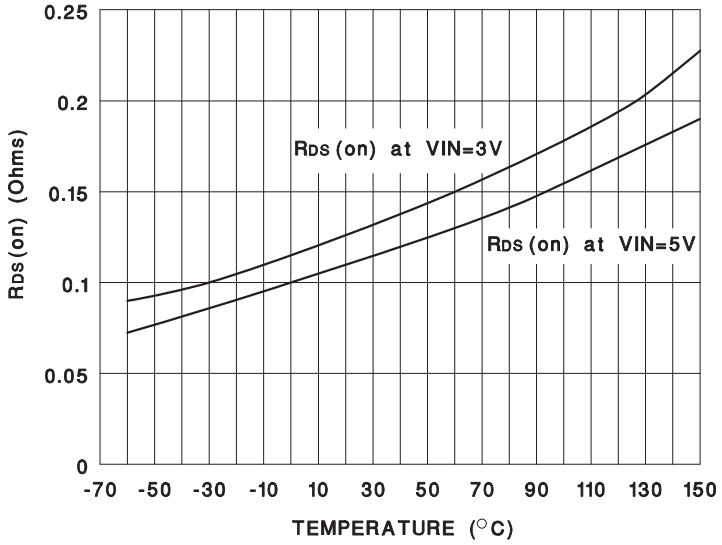



**Figure 4. $R_{DS(on)}$ vs. Temperature at 2-A Load Current.**

### safety recommendations

Although the UCC3912 family is designed to provide system protection for all fault conditions, all integrated circuits can ultimately fail short. For this reason, if the UCC3912 is intended for use in safety critical applications where UL or some other safety rating is required, a redundant safety device such as a fuse should be placed in series with the device. The UCC3912 will prevent the fuse from blowing virtually for all fault conditions, increasing system reliability and reducing maintenance cost, in addition to providing the hot swap benefits of the device.

## PACKAGING INFORMATION

| Orderable Device | Status [1] | Package Type | Package Drawing | Pins | Package Qty | Eco Plan [2] | Lead/Ball Finish | MSL Peak Temp [3] |
|---|---|---|---|---|---|---|---|---|
| UCC2912DP | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| UCC2912DPG4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| UCC2912DPR | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| UCC2912DPRG4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| UCC2912N | ACTIVE | PDIP | N | 16 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | N / A for Pkg Type |
| UCC2912NG4 | ACTIVE | PDIP | N | 16 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | N / A for Pkg Type |
| UCC2912PWP | ACTIVE | TSSOP | PW | 24 | 60 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| UCC2912PWPG4 | ACTIVE | TSSOP | PW | 24 | 60 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| UCC2912PWPR | ACTIVE | TSSOP | PW | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| UCC2912PWPRG4 | ACTIVE | TSSOP | PW | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| UCC3912DP | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| UCC3912DPG4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| UCC3912DPTR | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| UCC3912DPTRG4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| UCC3912PWP | ACTIVE | TSSOP | PW | 24 | 60 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| UCC3912PWPG4 | ACTIVE | TSSOP | PW | 24 | 60 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| UCC3912PWPTR | ACTIVE | TSSOP | PW | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| UCC3912PWPTRG4 | ACTIVE | TSSOP | PW | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |

[1] The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and

package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

**(3)** MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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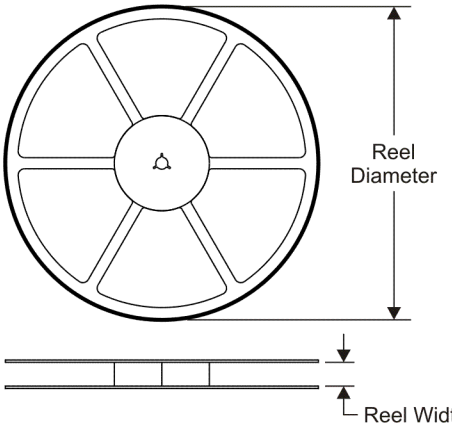
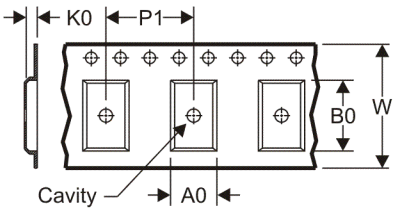
## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

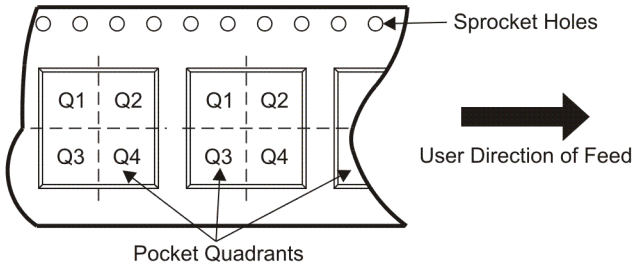



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

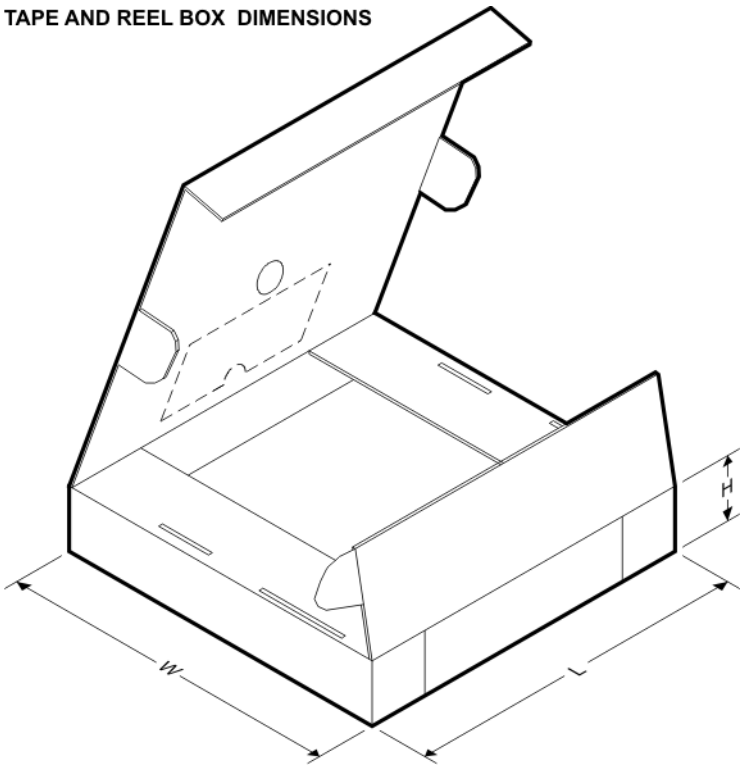
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| UCC2912DPR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| UCC3912DPTR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| UCC3912PWPTR | TSSOP | PW | 24 | 2000 | 330.0 | 16.4 | 6.95 | 8.3 | 1.6 | 8.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS

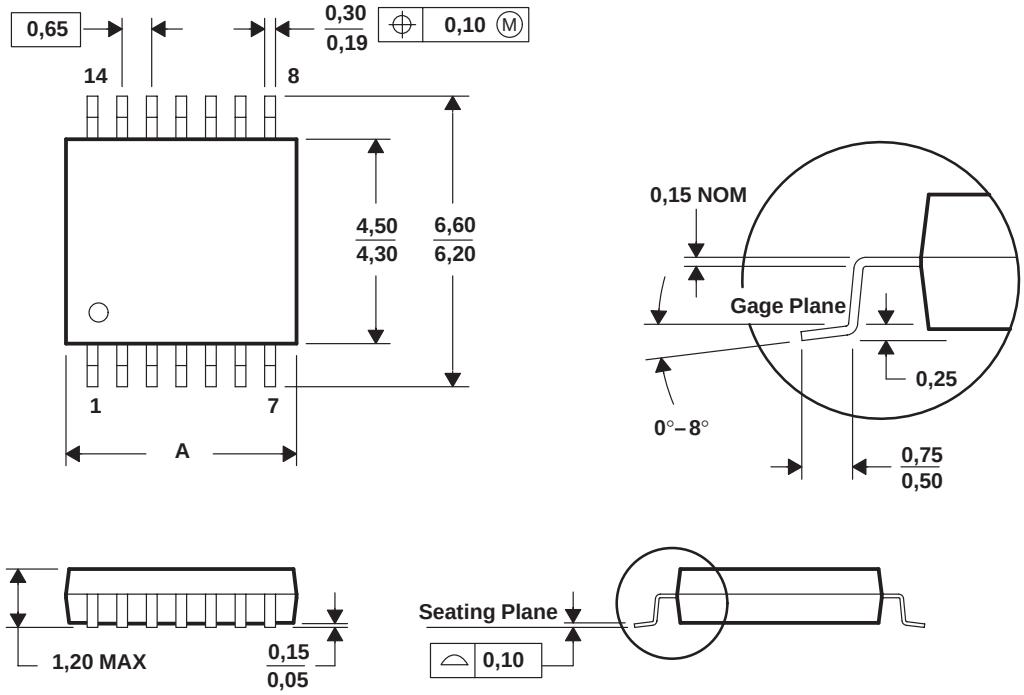



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| UCC2912DPR | SOIC | D | 16 | 2500 | 346.0 | 346.0 | 33.0 |
| UCC3912DPTR | SOIC | D | 16 | 2500 | 346.0 | 346.0 | 33.0 |
| UCC3912PWPTR | TSSOP | PW | 24 | 2000 | 346.0 | 346.0 | 33.0 |

**PW (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**14 PINS SHOWN**

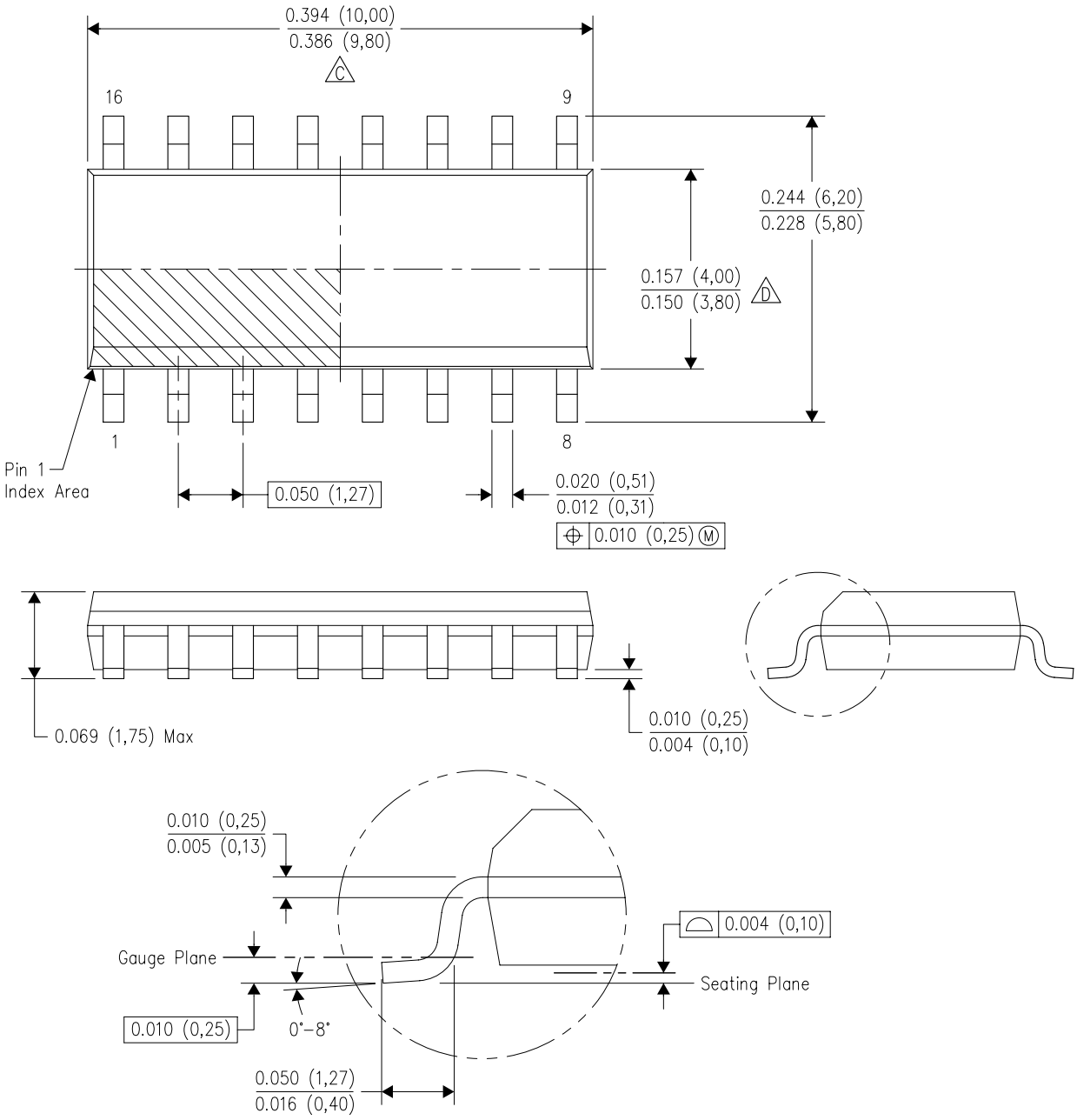



| DIM \ PINS ** | 8 | 14 | 16 | 20 | 24 | 28 |
|---|---|---|---|---|---|---|
| A MAX | 3,10 | 5,10 | 5,10 | 6,60 | 7,90 | 9,80 |
| A MIN | 2,90 | 4,90 | 4,90 | 6,40 | 7,70 | 9,60 |

**4040064/F 01/97**

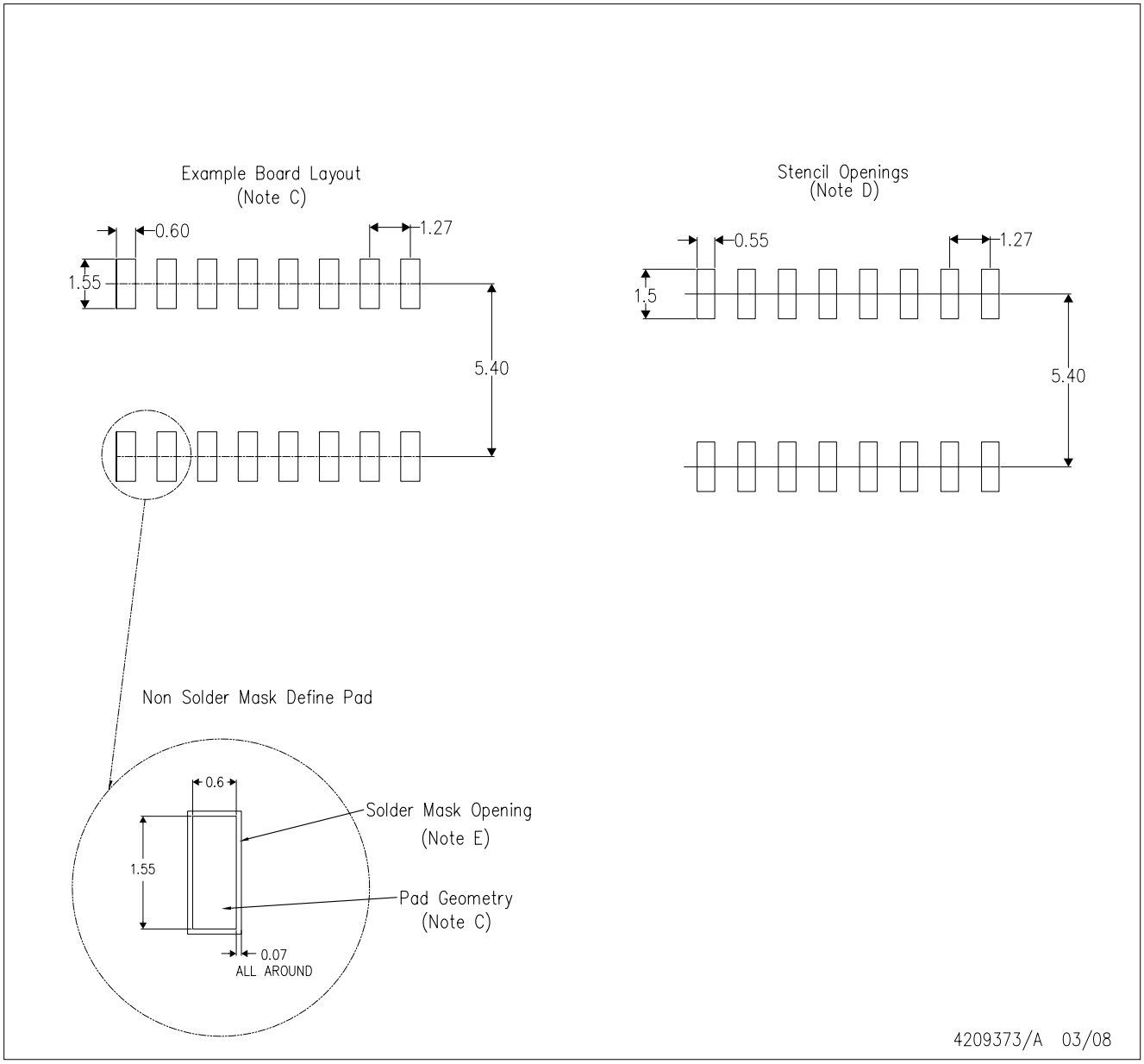
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

D (R–PDSO–G16) PLASTIC SMALL–OUTLINE PACKAGE




NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
E. Reference JEDEC MS–012 variation AC.

D(R–PDSO–G16)

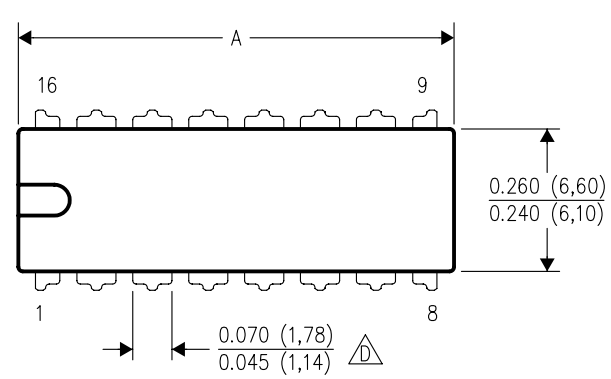



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Refer to IPC7351 for alternate board design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

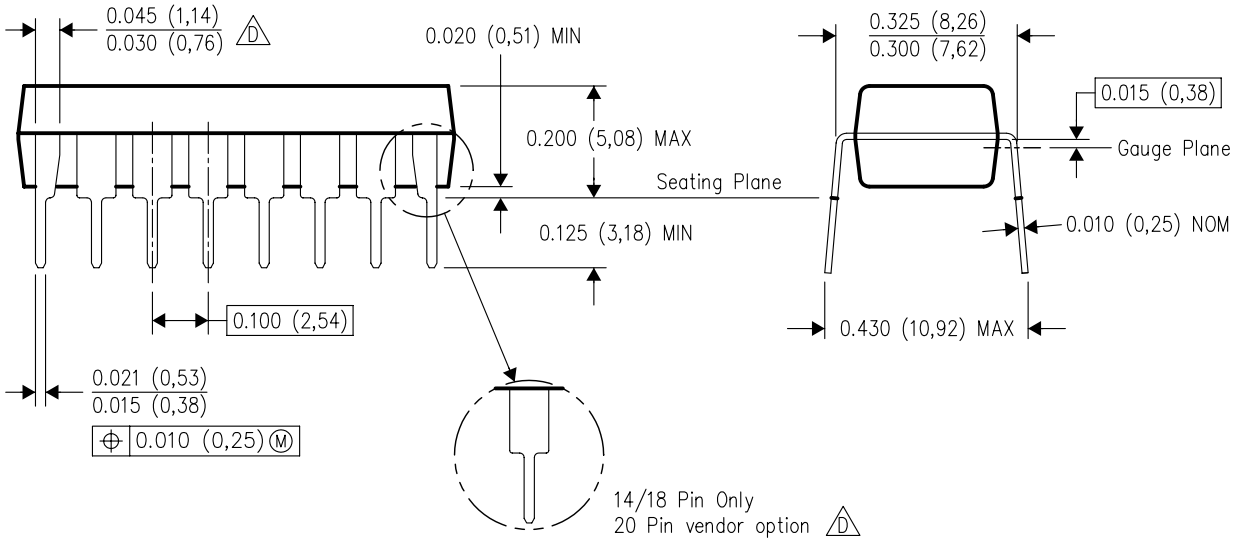
## N (R–PDIP–T**)

## PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN




| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS–001 VARIATION (C) | AA | BB | AC | AD |




4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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