



SoundPLUS™ Stereo Audio DIGITAL-TO-ANALOG CONVERTER With Programmable PLL

FEATURES

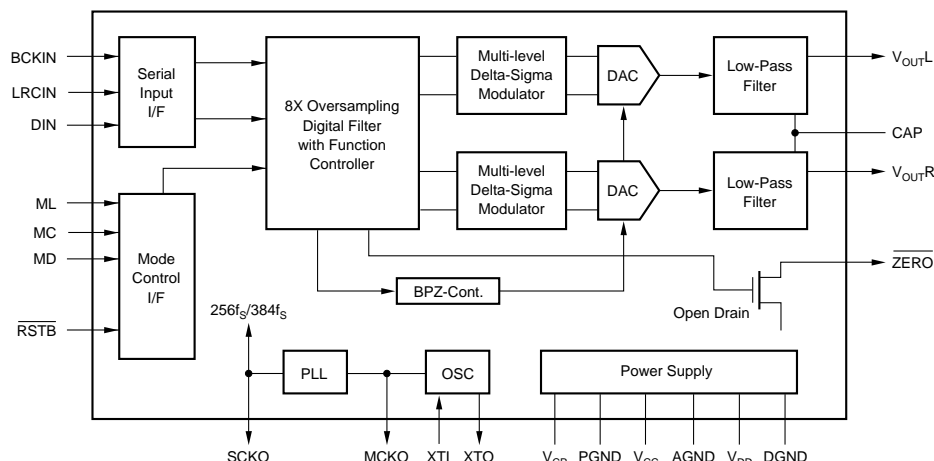
- ACCEPTS 16-, 20-, OR 24-BIT INPUT DATA
- COMPLETE STEREO DAC: Includes Digital Filter and Output Amp
- DYNAMIC RANGE: 94dB
- MULTIPLE SAMPLING FREQUENCIES:
16kHz, 22.05kHz, 24kHz
32kHz, 44.1kHz, 48kHz
64kHz, 88.2kHz, 96kHz
- PROGRAMMABLE PLL CIRCUIT:
256f_s/384f_s from 27MHz Master Clock
- NORMAL OR I²S™ DATA INPUT FORMATS
- SELECTABLE FUNCTIONS:
Soft Mute
Digital Attenuator (256 Steps)
Digital De-emphasis
- OUTPUT MODE: Left, Right, Mono, Mute

DESCRIPTION

The PCM1723 is a complete, low-cost, stereo audio digital-to-analog converter (DAC) with a phase-locked loop (PLL) circuit included. The PLL derives either a 256f_s or 384f_s system clock from an external 27MHz reference frequency. The DAC contains a 3rd-order delta-sigma (ΔΣ) modulator, a digital interpolation filter, and an analog output amplifier. The PCM1723 can accept 16-, 20-, or 24-bit input data in either normal or I²S formats.

The digital filter performs an 8X interpolation function and includes selectable features such as soft mute, digital attenuation and digital de-emphasis. The PLL can be programmed for sampling at standard digital audio frequencies as well as one-half and double sampling frequencies.

The PCM1723 is ideal for applications which combine compressed audio and video data such as DVD, DVD-ROM, set-top boxes and MPEG sound cards.



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ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

| | |
|---|-----------------------------------|
| Power Supply Voltage | +6.5V |
| +V _{CC} to +V _{DD} Difference | ±0.1V |
| Input Logic Voltage | –0.3V to (V _{DD} + 0.3V) |
| Input Current (except power supply) | ±10mA |
| Power Dissipation | 530mW |
| Operating Temperature Range | –25°C to +85°C |
| Storage Temperature | –55°C to +125°C |
| Lead Temperature (soldering, 5s) | +260°C |
| Thermal Resistance, θ_{JA} | +70°C/W |

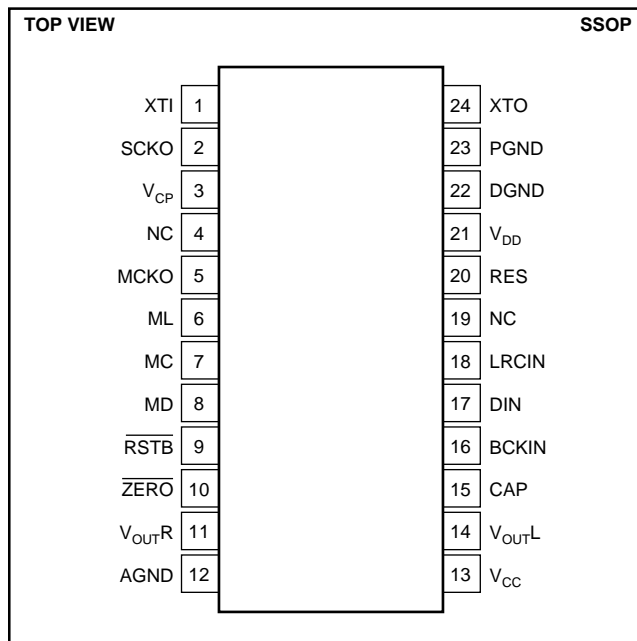
NOTE: (1) Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

PACKAGE INFORMATION⁽¹⁾

| PRODUCT | PACKAGE | PACKAGE DESIGNATOR |
|----------|-------------|--------------------|
| PCM1723E | 24-Pin SSOP | DB |

NOTE: (1) For the most current package and ordering information, see the Package Option Addendum at the end of this data sheet, or see the TI web site at www.ti.com

PIN CONFIGURATION



PIN ASSIGNMENTS

| PIN | NAME | TYPE | FUNCTION |
|-------------------|-------------------|------|---|
| 1 | XTI | IN | Master Clock Input. |
| 2 | SCKO | OUT | System Clock Out. This output is 256f _S or 384f _S system clock generated by the internal PLL. |
| 3 | V _{CP} | PWR | PLL Power Supply (+5V). |
| 4 | NC | N/A | No connection. |
| 5 | MCKO | Out | Buffered clock output of crystal oscillator. |
| 6 ⁽¹⁾ | ML | IN | Latch for serial control data. |
| 7 ⁽¹⁾ | MC | IN | Clock for serial control data. |
| 8 ⁽¹⁾ | MD | IN | Data for serial control. |
| 9 ⁽¹⁾ | RSTB | IN | Reset Input. When this pin is low, the digital filters and modulators are held in reset. |
| 10 | ZERO | OUT | Zero Data Flag. This pin is low when the input data is continuously zero for more than 65, 535 cycles of BCKIN. |
| 11 | V _{OUTR} | OUT | Right Channel Analog Output. |
| 12 | AGND | GND | Analog Ground. |
| 13 | V _{CC} | PWR | Analog Power Supply (+5V). |
| 14 | V _{OUTL} | OUT | Left Channel Analog Output. |
| 15 | CAP | | Common pin for analog output amplifiers. |
| 16 ⁽²⁾ | BCKIN | IN | Bit clock for clocking in the audio data. |
| 17 ⁽²⁾ | DIN | IN | Serial audio data input. |
| 18 ⁽²⁾ | LRCIN | IN | Left/Right Word Clock. Frequency is equal to f _S . |
| 19 | NC | N/A | No connection. |
| 20 | RES | N/A | Reserved for factory use, do not connect. |
| 21 | V _{DD} | PWR | Analog Power Supply (+5V). |
| 22 | DGND | GND | Digital Ground. |
| 23 | PGND | GND | PLL Ground. |
| 24 | XTO | Out | Crystal oscillator output. |

NOTES: (1) Schmitt trigger input with internal pull-up resistors.
(2) Schmitt trigger input.

ELECTRICAL CHARACTERISTICS

All specifications at +25°C, +V_{CC} = +V_{DD} = +V_{CP} = +5V, f_S = 44.1kHz, and 16-bit input data, SYSCLK = 384f_S, unless otherwise noted.

| PARAMETER | CONDITIONS | PCM1723 | | | UNITS |
|--|--|---|--|--|---|
| | | MIN | TYP | MAX | |
| RESOLUTION | | 16 | | | Bits |
| DATA FORMAT Audio Data Interface Format Data Bit Length Audio Data Format Sampling Frequency (f _S) | | Standard/I ² S Selectable 16/20/24 Selectable MSB First, Binary Two's Complement | | | |
| | Standard f _S | 32 | 44.1 | 48 | kHz |
| | One-half f _S | 16 | 22.05 | 24 | kHz |
| | Double f _S | 64 | 88.2 | 96 | kHz |
| PLL PERFORMANCE Master Clock Input Frequency ⁽⁴⁾ Master Clock Output Frequency Generated SYSCLK Frequency Output Logic Level V _{OH} (MCKO, SCKO) V _{OL} Generated SYSCLK Jitter Generated SYSCLK Transient ⁽¹⁾ Power-Up Time Generated SYSCLK Duty Cycle | I _{OH} = 2mA I _{OL} = 4mA Standard Dev f _M = 27MHz To Programmed Frequency f _M = 27MHz, C _L = 15pF | 26.73 4.096 V _{DD} – 0.4 40 | 27 256f _S /384f _S ±150 15 50 | 27.27 36.864 0.5 20 30 60 | MHz MHz VDC VDC ps ms ms % |
| DIGITAL INPUT LOGIC LEVEL | | | TTL | | |
| DYNAMIC PERFORMANCE⁽²⁾ THD+N at f _S (0dB) THD+N at –60dB Dynamic Range (EIAJ Method) Signal-to-Noise Ratio ⁽³⁾ (EIAJ Method) Channel Separation | f _S = 44.1kHz f _S = 96kHz f _S = 44.1kHz f _S = 96kHz f _S = 44.1kHz f _S = 96kHz f _S = 44.1kHz f _S = 96kHz f _S = 44.1kHz | 90 90 88 | –89 –87 –31 –29 94 91 96 95 93 | –80 | dB dB dB dB dB dB dB dB dB |
| DC ACCURACY Gain Error Gain Mismatch, Channel-to-Channel Bipolar Zero Error | V _{OUT} = V _{CC} /2 at BPZ | | ±1.0 ±1.0 ±30 | ±3.0 ±2.0 | % of FSR % of FSR mV |
| ANALOG OUTPUT Output Voltage Center Voltage Load Impedance | Full Scale (–0dB) AC Load | 5 | 0.62 x V _{CC} V _{CC} /2 | | V _{PP} V _{DC} kΩ |
| DIGITAL FILTER PERFORMANCE Passband Stop Band Passband Ripple Stop Band Attenuation Delay Time De-emphasis Error | | 0.555 –35 –0.2 | 11.125/f _S | 0.445 ±0.17 +0.55 | f _S f _S dB dB sec dB |
| INTERNAL ANALOG FILTER –3dB Bandwidth Passband Response | f = 20kHz | | 100 –0.16 | | kHz dB |
| POWER SUPPLY REQUIREMENTS Voltage Range Supply Current: I _{CC} + I _{DD} + I _{CP} | V _{CC} = V _{DD} = V _{CP} f _S = 44.1kHz | 4.5 | 5 20 | 5.5 24 | VDC mA |
| TEMPERATURE RANGE Operating Storage | | –25 –55 | | +85 +100 | °C °C |

NOTES: (1) Sysclk transient is the maximum frequency lock time when the PLL frequency is changed.

(2) Dynamic performance specs are tested with 20kHz low pass filter and THD+N specs are tested with 30kHz LPF, 400Hz HPF, Average-Mode.

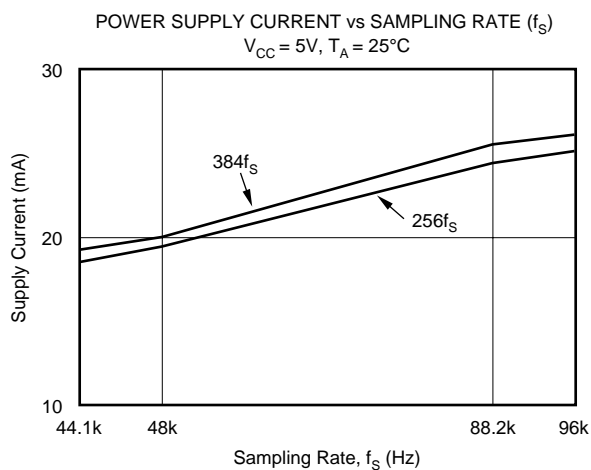
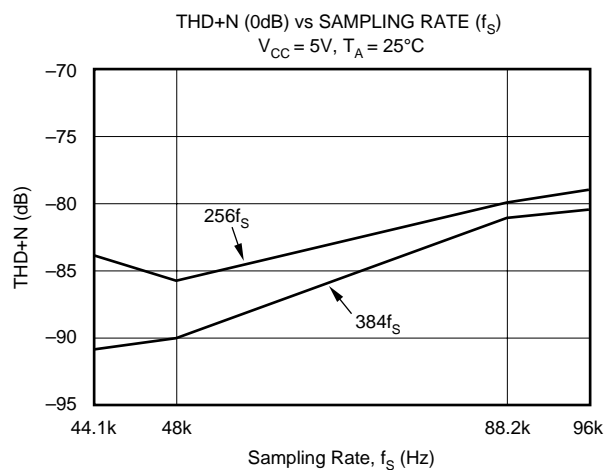
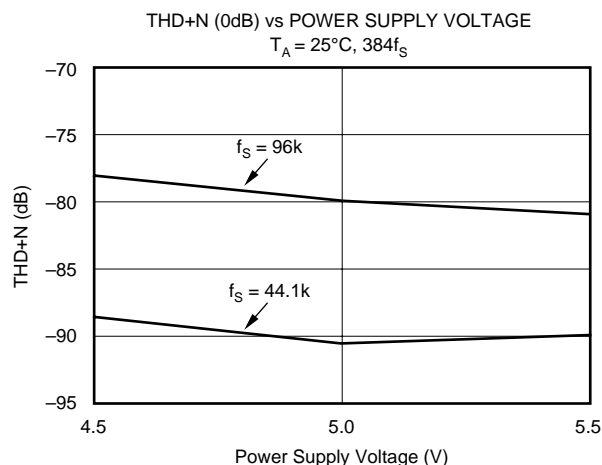
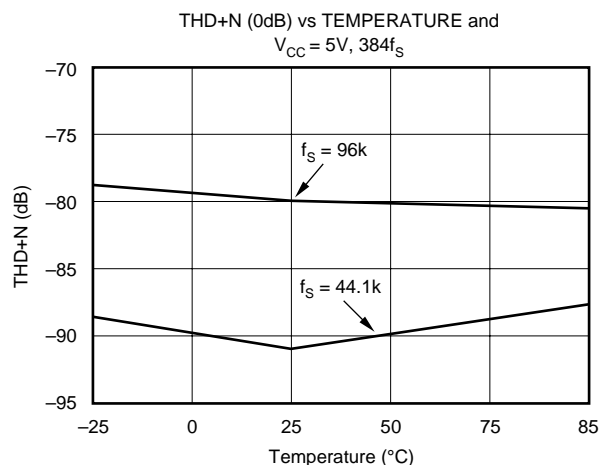
(3) SNR is tested at Infinite Zero Detection off.

(4) PLL evaluations tested with 1ns maximum jitter on the 27MHz input clock.

TYPICAL CHARACTERISTICS

At $T_A = +25^\circ\text{C}$, $V_{CC} = V_{DD} = V_{CP} = +5\text{V}$, $f_S = 44.1\text{kHz}$, 16-bit input data, $384f_S$, unless otherwise noted. Measurement bandwidth is 20kHz.

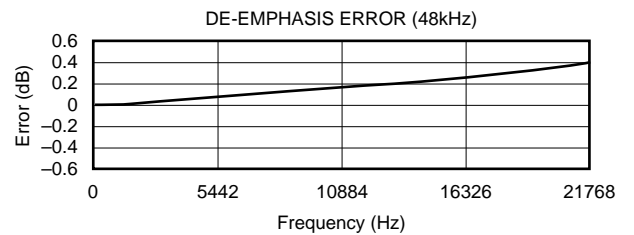
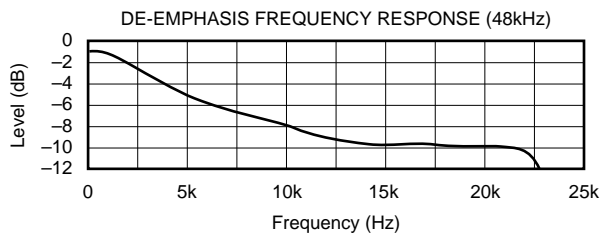
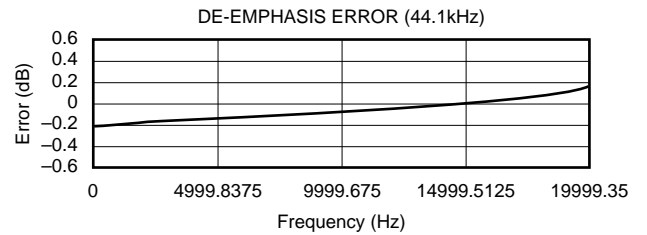
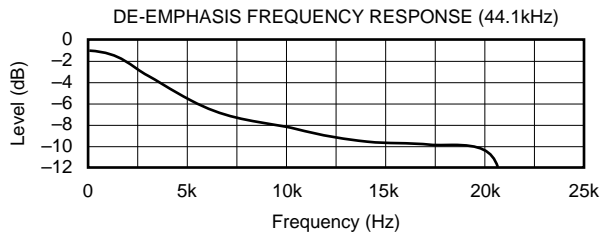
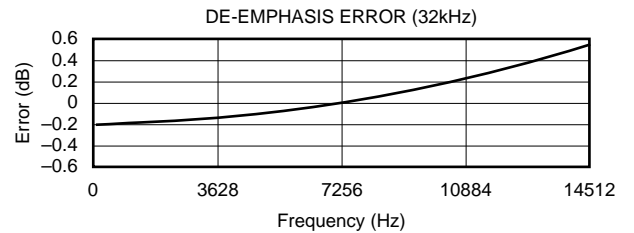
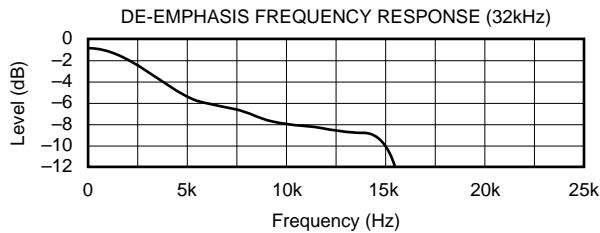
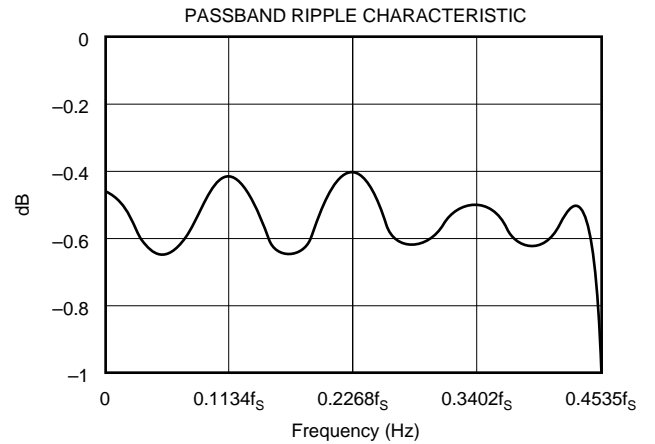
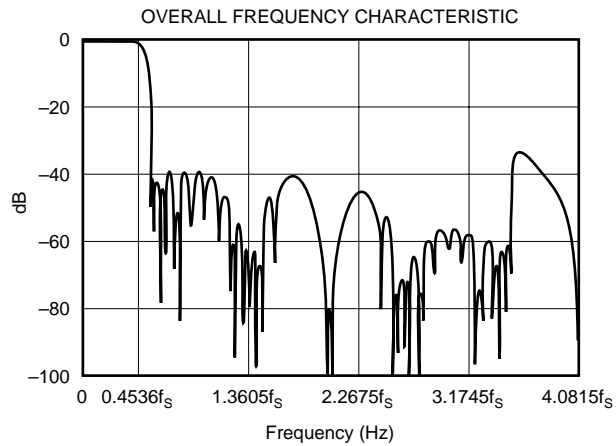
DYNAMIC PERFORMANCE



TYPICAL CHARACTERISTICS (Cont.)

At $T_A = +25^\circ\text{C}$, $V_S = +5\text{V}$, $R_L = 44.1\text{kHz}$, and $f_{\text{SYS}} = 384\text{f}_S$, unless otherwise noted.

DIGITAL FILTER



TYPICAL CONNECTION DIAGRAM

Figure 1 illustrates the typical connection diagram for the PCM1723 in an MPEG-2 application. The 27MHz master video clock (f_M) drives XTI (pin 1) of the PCM1723. A programmable system clock is generated by the PCM1723 PLL, with SCKO used to drive the MPEG-2 decoder system clock input. The standard audio signals (data, bit clock, and word clock) are generated in the decoder from the PCM1723 system clock, providing synchronization of audio and video signals.

PLL CIRCUIT

The PCM1723 has a programmable internal PLL circuit, as shown in Figure 2. The PLL is designed to accept a 27MHz master clock or crystal oscillator and generate all internal system clocks required to operate the digital filter and $\Delta\Sigma$ modulator, either at $256f_S$ or $384f_S$. If an external master clock is used, XTO must be connected to GND. In both cases, the signal amplitude on XTI must satisfy the specification described in Figure 3. Therefore, careful C1 and C2 determination is required to keep this specification satisfied when

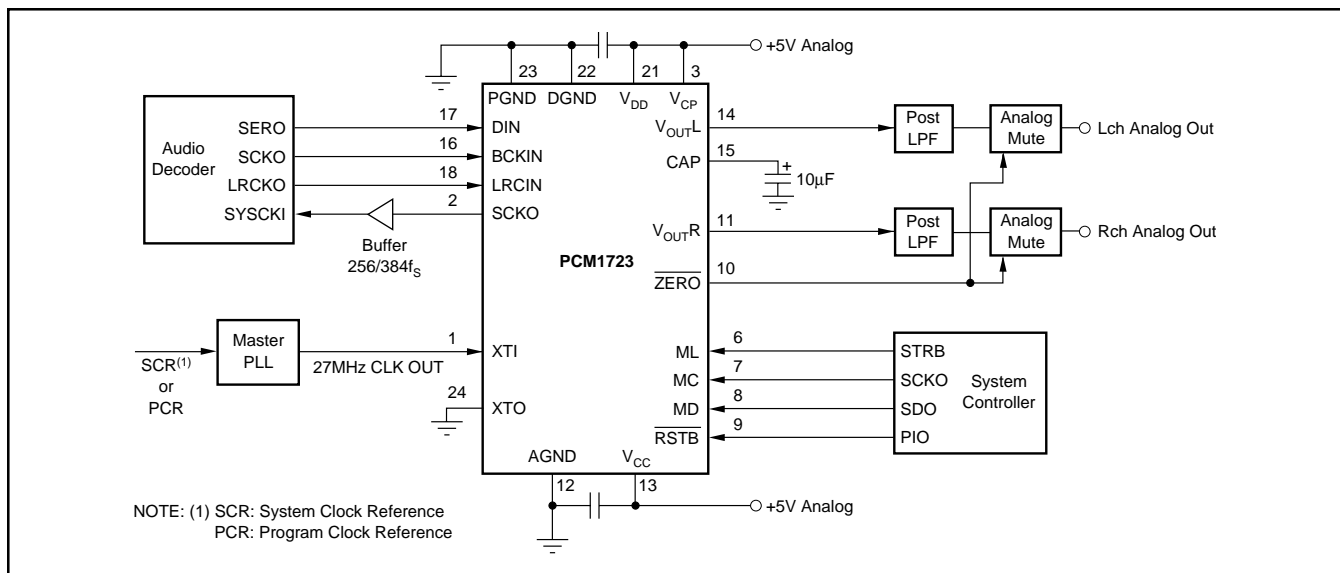


FIGURE 1. Connection Diagram for External Master Clock in a Typical MPEG-2 Application.

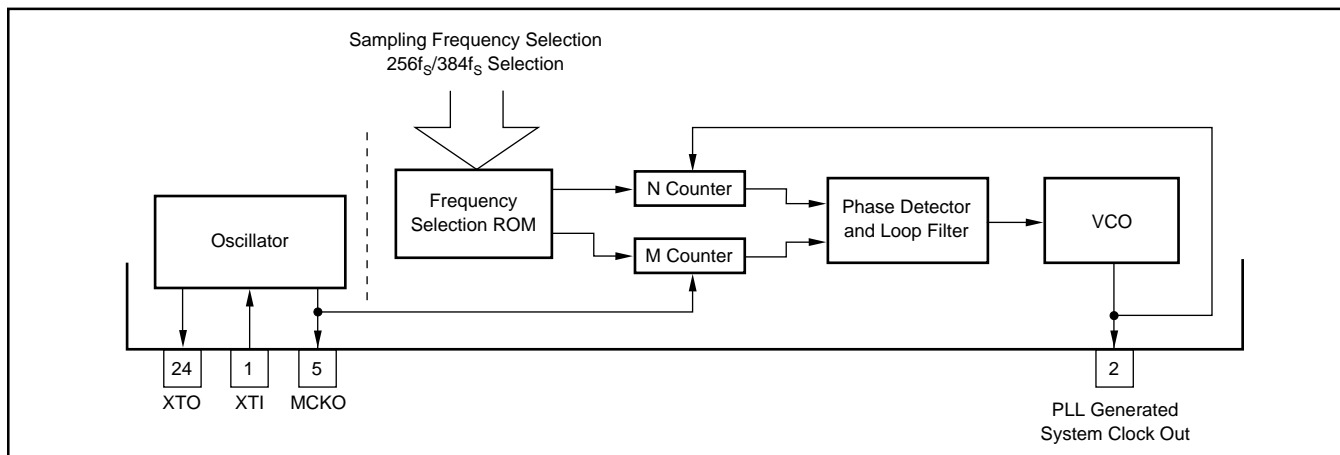


FIGURE 2. PLL Block Diagram.

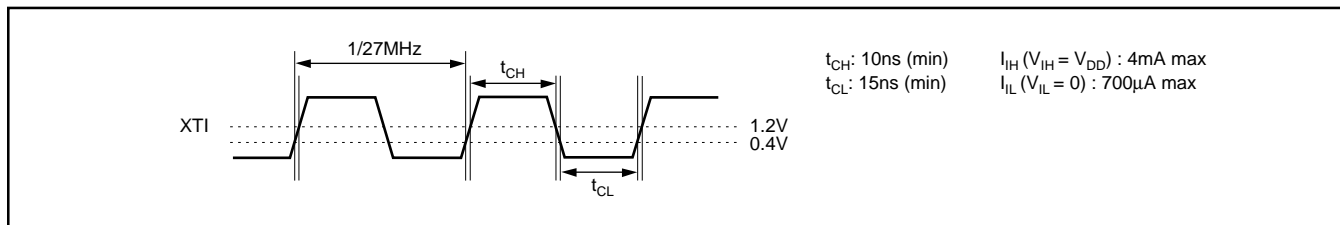


FIGURE 3. XTI Input Timing.

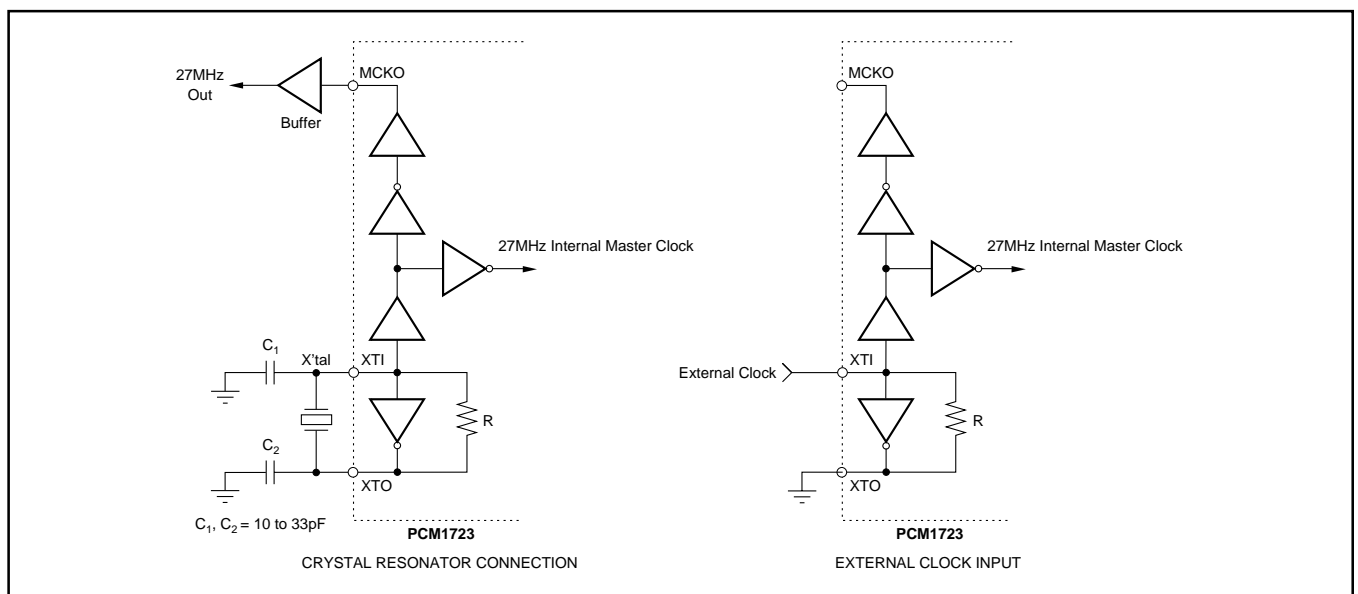


FIGURE 4. System Clock Connection.

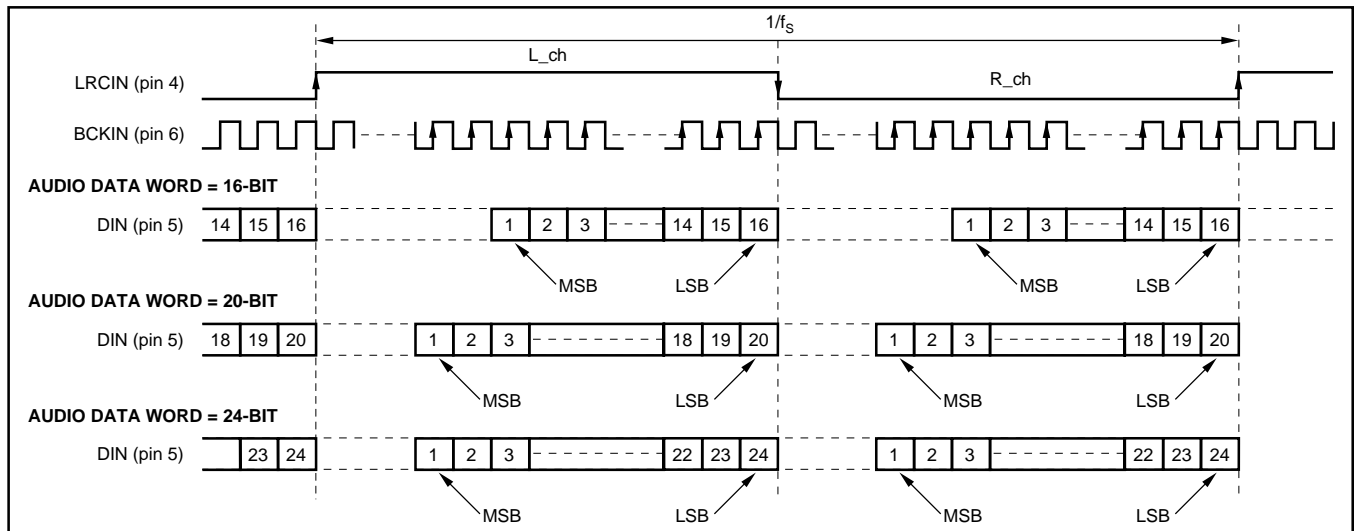


FIGURE 5. Normal Data Input Timing.

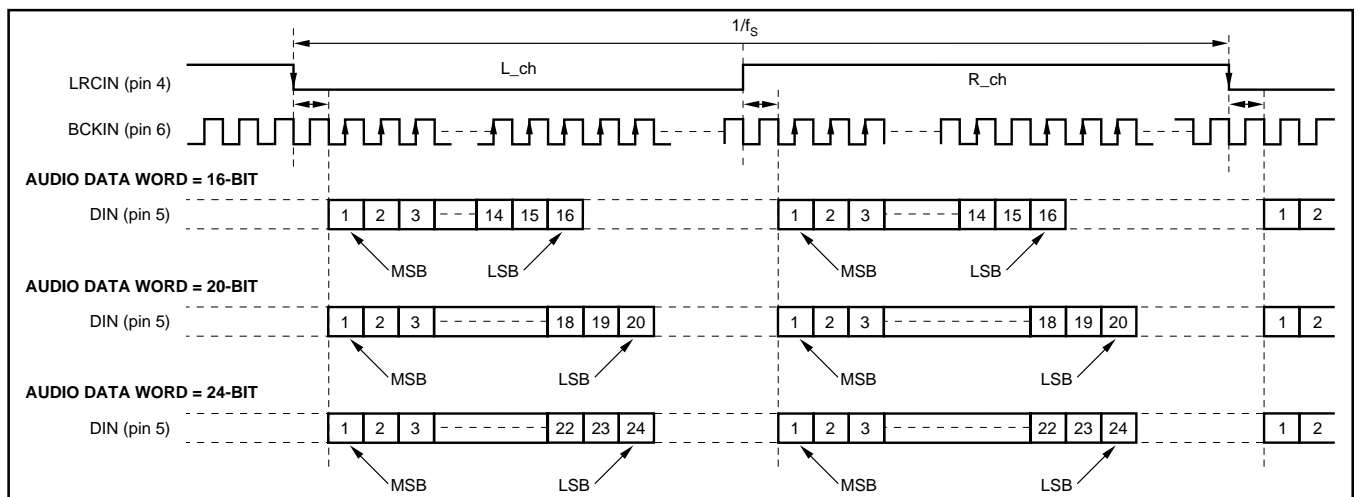


FIGURE 6. I²S Data Input Timing.

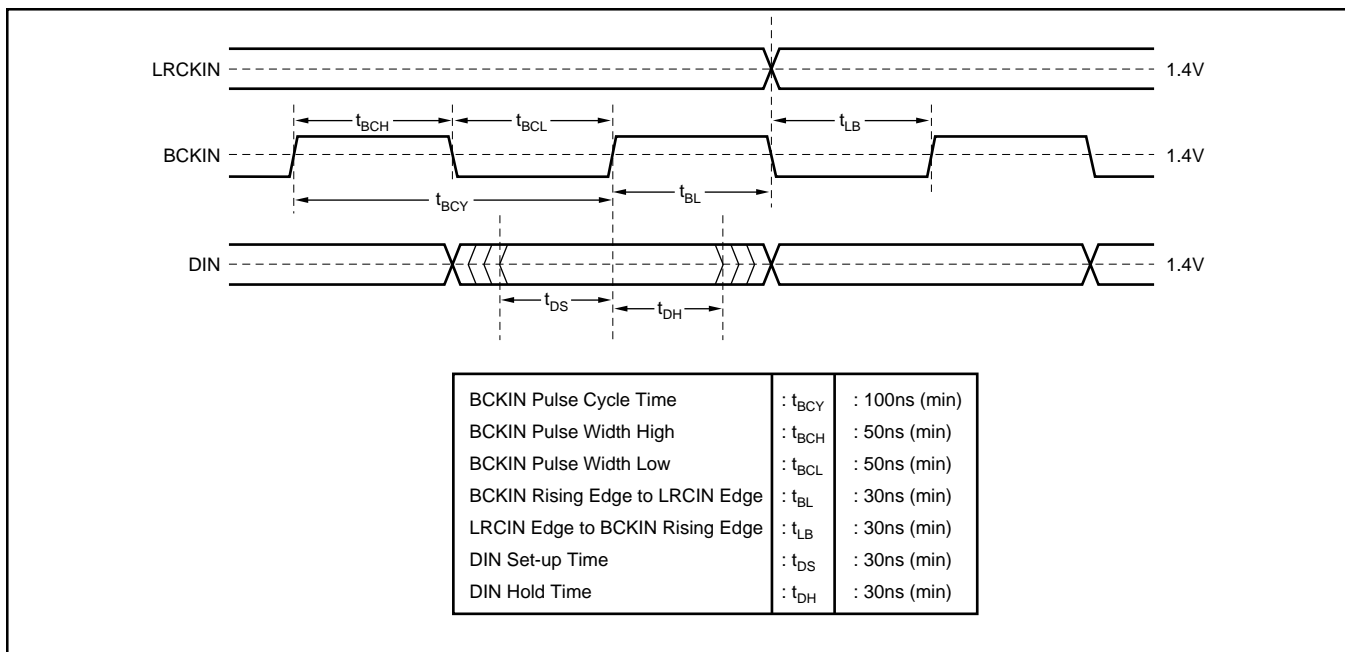


FIGURE 7. Audio Data Input Timing.

using a crystal oscillator. The PLL will directly track any variations in the master clock frequency, and jitter on the system clock is specified at 250ps maximum. Figure 3 illustrates the timing requirements for the 27MHz master clock. Figure 4 illustrates the system clock connections for an external clock or crystal oscillator.

The PCM1723 internal PLL can be programmed for nine different sampling frequencies (LRCIN), as shown in Table I. The internal sampling clocks generated by the various programmed frequencies are shown in Table II. The system clock output frequency for the PCM1723 is 100% accurate. To provide MCKO clock and SCKO clock for external circuit, external buffer circuit is effective to avoid degrading audio performance.

| | Sampling Frequencies-LRCIN (kHz) | | |
|----------------------------------|----------------------------------|-------|----|
| Half of Standard Sampling Freq | 16 | 22.05 | 24 |
| Standard Sampling Freq | 32 | 44.1 | 48 |
| Double of Standard Sampling Freq | 64 | 88.2 | 96 |

TABLE I. Sampling Frequencies.

| Sampling Frequency (LRCIN) | | System Clock 256f _s | System Clock 384f _s |
|----------------------------|----------|--------------------------------|--------------------------------|
| 16kHz | Half | 4.096MHz | 6.144MHz |
| 32kHz | Standard | 8.192MHz | 12.288MHz |
| 64kHz | Double | 16.384MHz | 24.576MHz |
| 22.05kHz | Half | 5.6448MHz | 8.4672MHz |
| 44.1kHz | Standard | 11.2896MHz | 16.9344MHz |
| 88.2kHz | Double | 22.5792MHz | 33.8688MHz |
| 24kHz | Half | 6.144MHz | 9.216MHz |
| 48kHz | Standard | 12.288MHz | 18.432MHz |
| 96kHz | Double | 24.576MHz | 36.864MHz |

TABLE II. Sampling Frequencies vs Internal System Clock (= Output Frequencies of PLL).

SPECIAL FUNCTIONS

The PCM1723 includes several special functions, including digital attenuation, digital de-emphasis, soft mute, data format selection and input word resolution. These functions are controlled using a three-wire interface. MD (pin 8) is used for the program data, MC (pin 7) is used to clock in the program data, and ML (pin 6) is used to latch in the program data. Table III lists the selectable special functions.

| FUNCTION | DEFAULT MODE |
|---|------------------------------------|
| Input Audio Data Format Selection Normal Format I ² S Format | Normal Format |
| Input Audio Data Bit Selection 16/20/24 Bits | 16 Bits |
| Input LRCIN Polarity Selection Lch/Rch = High/Low Lch/Rch = Low/High | Lch/Rch = High/Low |
| De-emphasis Control | OFF |
| Soft Mute Control | OFF |
| Attenuation Control Lch, Rch Individually Lch, Rch Common | 0dB Lch, Rch Individually Fixed |
| Infinite Zero Detection Circuit Control | OFF |
| Operation Enable (OPE) | Enabled |
| Sample Rate Selection Internal System Clock Selection 256f _s 384f _s | 384f _s |
| Double Sampling Rate Selection Standard Sampling Rate—44.1/48/32kHz Double Sampling Rate—88.2/96/32kHz Half Sampling Rate—22.05/24/16kHz | Standard Sampling Rate |
| Sampling Frequency 44.1kHz Group 48kHz Group 32kHz Group | 44.1kHz |
| Analog Output Mode L, R, Mono, Mute | Stereo |

TABLE III. Selectable Functions.

MAPPING OF PROGRAM REGISTERS

| | B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|-------|-----|-----|-----|-----|-----|-----|----|-----|-----|-----|------|------|-----|-----|-----|------------------|
| MODE0 | res | res | res | res | res | A1 | A0 | LDL | AL7 | AL6 | AL5 | AL4 | AL3 | AL2 | AL1 | AL0 |
| MODE1 | res | res | res | res | res | A1 | A0 | LDR | AR7 | AR6 | AR5 | AR4 | AR3 | AR2 | AR1 | AR0 |
| MODE2 | res | res | res | res | res | A1 | A0 | PL3 | PL2 | PL1 | PL0 | IW1 | IW0 | OPE | DEM | MUT |
| MODE3 | res | res | res | res | res | A1 | A0 | IZD | SF1 | SF0 | DSR1 | DSR0 | SYS | ATC | LRP | I ² S |

PROGRAM REGISTER BIT MAPPING

The PCM1723 special functions are controlled using four program registers that are 16 bits long. These registers are all loaded using MD. After the 16 data bits are clocked in, ML is used to latch in the data to the appropriate register. Table IV shows the complete mapping of the four registers and Figure 8 illustrates the serial interface timing.

| REGISTER NAME | BIT NAME | DESCRIPTION |
|---------------|---|---|
| Register 0 | AL (7:0) LDL A (1:0) Res | DAC Attenuation Data for Lch Attenuation Data Load Control for Lch Register Address Reserved |
| Register 1 | AR (7:0) LDL A (1:0) Res | DAC Attenuation Data for Rch Attenuation Data Load Control for Rch Register Address Reserved |
| Register 2 | MUT DEM OPE IW (1:0) PL (3:0) A (1:0) res | Left and Right DACs Soft Mute Control De-emphasis Control Left and Right DACs Operation Control Input Audio Data Bit Select Output Mode Select Register Address Reserved |
| Register 3 | I ² S LRP ATC SYS DSR (1:0) SF (1:0) IZD A (1:0) Res | Audio Data Format Select Polarity of LRCIN (pin 7) Select Attenuator Control System Clock Select Double Sampling Rate Select Sampling Rate Select Infinite Zero Detection Circuit Control Register Address Reserved |

TABLE IV. Internal Register Mapping.

REGISTER 0 (A1 = 0, A0 = 0)

| B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|-----|-----|-----|-----|-----|-----|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| res | res | res | res | res | A1 | A0 | LDL | AL7 | AL6 | AL5 | AL4 | AL3 | AL2 | AL1 | AL0 |

Register 0 is used to control left channel attenuation. Bits 0 - 7 (AL0 - AL7) are used to determine the attenuation level. The level of attenuation is given by:

$$ATT = [20 \log_{10} (ATT_DATA/255)] \text{ dB}$$

ATTENUATION DATA LOAD CONTROL

Bit 8 (LDL) is used to control the loading of attenuation data in B0:B7. When LDL is set to 0, attenuation data will be loaded into AL0:AL7, but it will not affect the attenuation

level until LDL is set to 1. LDR in Register 1 has the same function for right channel attenuation.

Attenuation Level (ATT) can be controlled as following Resistor set AL (R) (7:0).

| AL (R) (7:0) | ATT LEVEL |
|--------------|-------------|
| 00h | −∞dB (Mute) |
| 01h | −48.16dB |
| ⋮ | ⋮ |
| FEh | −0.07dB |
| FFh | 0dB |

REGISTER 1 (A1 = 0, A0 = 1)

| B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|-----|-----|-----|-----|-----|-----|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| res | res | res | res | res | A1 | A0 | LDR | AR7 | AR6 | AR5 | AR4 | AR3 | AR2 | AR1 | AR0 |

Register 1 is used to control right channel attenuation. As in Register 1, bits 0 - 7 (AR0 - AR7) control the level of attenuation.

REGISTER 2 (A1 = 1, A0 = 0)

| B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|-----|-----|-----|-----|-----|-----|----|-----|-----|-----|-----|-----|-----|-----|-----|------|
| res | res | res | res | res | A1 | A0 | PL3 | PL2 | PL1 | PL0 | IW1 | IW0 | OPE | DEM | MUTE |

Register 2 is used to control soft mute, de-emphasis, operation enable, input resolution, and output format. Bit 0 is used for soft mute: a HIGH level on bit 0 will cause the output to be muted (this is ramped down in the digital domain, so no *click* is audible). Bit 1 is used to control de-emphasis. A LOW level on bit 1 disables de-emphasis, while a HIGH level enables de-emphasis.

Bit 2 (OPE) is used for operational control. Table V illustrates the features controlled by OPE.

| | DATA INPUT | DAC OUTPUT | SOFTWARE MODE INPUT |
|---------|------------|------------------------------|---------------------|
| OPE = 1 | Zero | Forced to BPZ ⁽¹⁾ | Enabled |
| | Other | Forced to BPZ ⁽¹⁾ | Enabled |
| OPE = 0 | Zero | Controlled by IZD | Enabled |
| | Other | Normal | Enabled |

NOTE: (1) $\Delta\Sigma$ is disconnected from output amplifier.

TABLE V. Operation Enable (OPE) Function.

OPE controls the operation of the DAC: when OPE is LOW, the DAC will convert all non-zero input data. If the input data is continuously zero for 65,536 cycles of BCKIN, the output will be forced to zero only if IZD is HIGH. When OPE is HIGH, the output of the DAC will be forced to bipolar zero, irrespective of any input data.

| | DATA INPUT | DAC OUTPUT |
|---------|------------|------------------------------|
| IZD = 1 | Zero | Forced to BPZ ⁽¹⁾ |
| | Other | Normal |
| IZD = 0 | Zero | Zero ⁽²⁾ |
| | Other | Normal |

NOTES: (1) $\Delta\Sigma$ is disconnected from output amplifier.
(2) $\Delta\Sigma$ is connected to output amplifier.

TABLE VI. Infinite Zero Detection (IZD) Function.

| | DATA INPUT | DAC OUTPUT | SOFTWARE MODE INPUT |
|-------------|------------|------------------------------|---------------------|
| RSTB = HIGH | Zero | Controlled by OPE and IZD | Enabled |
| | Other | Controlled by OPE and IZD | Enabled |
| RSTB = LOW | Zero | Forced to BPZ ⁽¹⁾ | Disabled |
| | Other | Forced to BPZ ⁽¹⁾ | Disabled |

NOTE: (1) $\Delta\Sigma$ is disconnected from output amplifier.

TABLE VII. Reset (RSTB) Function.

Bits 3 (IW0) and 4 (IW1) are used to determine input word resolution. PCM1723 can be set up for input word resolutions of 16, 20, or 24 bits:

| Bit 4 (IW1) | Bit 3 (IW0) | Input Resolution |
|-------------|-------------|------------------|
| 0 | 0 | 16-bit Data Word |
| 0 | 1 | 20-bit Data Word |
| 1 | 0 | 24-bit Data Word |
| 1 | 1 | Reserved |

Bits 5, 6, 7, and 8 (PL0:3) are used to control output format. The output of PCM1723 can be programmed for 16 different states, as shown in Table VIII.

| PL0 | PL1 | PL2 | PL3 | Lch OUTPUT | Rch OUTPUT | NOTE |
|-----|-----|-----|-----|------------|------------|---------|
| 0 | 0 | 0 | 0 | MUTE | MUTE | MUTE |
| 0 | 0 | 0 | 1 | MUTE | R | |
| 0 | 0 | 1 | 0 | MUTE | L | |
| 0 | 0 | 1 | 1 | MUTE | (L + R)/2 | |
| 0 | 1 | 0 | 0 | R | MUTE | |
| 0 | 1 | 0 | 1 | R | R | |
| 0 | 1 | 1 | 0 | R | L | REVERSE |
| 0 | 1 | 1 | 1 | R | (L + R)/2 | |
| 1 | 0 | 0 | 0 | L | MUTE | |
| 1 | 0 | 0 | 1 | L | R | STEREO |
| 1 | 0 | 1 | 0 | L | L | |
| 1 | 0 | 1 | 1 | L | (L + R)/2 | |
| 1 | 1 | 0 | 0 | (L + R)/2 | MUTE | |
| 1 | 1 | 0 | 1 | (L + R)/2 | R | |
| 1 | 1 | 1 | 0 | (L + R)/2 | L | |
| 1 | 1 | 1 | 1 | (L + R)/2 | (L + R)/2 | MONO |

TABLE VIII. Programmable Output Format.

REGISTER 3 (A1 = 1, A0 = 1)

| | | | | | | | | | | | | | | | |
|-----|-----|-----|-----|-----|-----|----|-----|-----|-----|------|------|-----|-----|-----|------------------|
| B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
| res | res | res | res | res | A1 | A0 | IZD | SF1 | SF0 | DSR1 | DSR0 | SYS | ATC | LRP | I ² S |

Register 3 is used to control input data format and polarity, attenuation channel control, system clock frequency, sampling frequency, and infinite zero detection.

Bits 0 (I²S) and 1 (LRP) are used to control the input data format. A LOW on bit 0 sets the format to Normal (MSB-first, right-justified Japanese format), and a HIGH sets the format to I²S (Philips serial data protocol). Bit 1 (LRP) is used to select the polarity of LRCIN (sample rate clock). When bit 1 is LOW, left channel data are assumed when LRCIN is in a HIGH phase and right channel data are assumed when LRCIN is in a LOW phase. When bit 1 is HIGH, the polarity assumption is reversed.

Bit 2 (ATC) is used for controlling the attenuator. When bit 2 is HIGH, the attenuation data loaded in program Register 0 are used for both left and right channels. When bit 2 is LOW, the attenuation data for each register are applied separately to left and right channels.

Bit 3 (SYS) is the system clock selection. When bit 3 is LOW, the system clock frequency is set to 384f_s. When bit 3 is HIGH, the system clock frequency is set to 256f_s.

Bits 4 (DSR0) and 5 (DSR1) are used to control multiples of the sampling rate:

| DSR1 | DSR0 | Multiple | |
|------|------|----------|----------------|
| 0 | 0 | Normal | 32/44.1/48kHz |
| 0 | 1 | Double | 64/88.2/96kHz |
| 1 | 0 | One-half | 16/22.05/24kHz |
| 1 | 1 | Reserved | Not Defined |

Bits 6 (SF0) and 7 (SF1) are used to select the sampling frequency. Frequency selection must be made with an interval time greater than 20μs.

| SF1 | SF0 | Sampling Frequency | |
|-----|-----|--------------------|--------------------|
| 0 | 0 | 44.1kHz group | 22.05/44.1/88.2kHz |
| 0 | 1 | 48kHz group | 24/48/96kHz |
| 1 | 0 | 32kHz group | 16/32/64kHz |
| 1 | 1 | Reserved | Not Defined |

Bit 8 is used to control the infinite zero detection function (IZD).

When IZD is LOW, the zero detect circuit is off. Under this condition, no automatic muting will occur if the input is continuously zero. When IZD is HIGH, the zero detect feature is enabled. If the input data are continuously zero for 65,536 cycles of BCKIN, the output will be immediately forced to a bipolar zero state ($V_{CC}/2$). The zero detection feature is used to avoid noise which may occur when the input is DC. When the output is forced to bipolar zero, there may be an audible click. PCM1723 allows the zero detect feature to be disabled so the user can implement an external muting circuit.

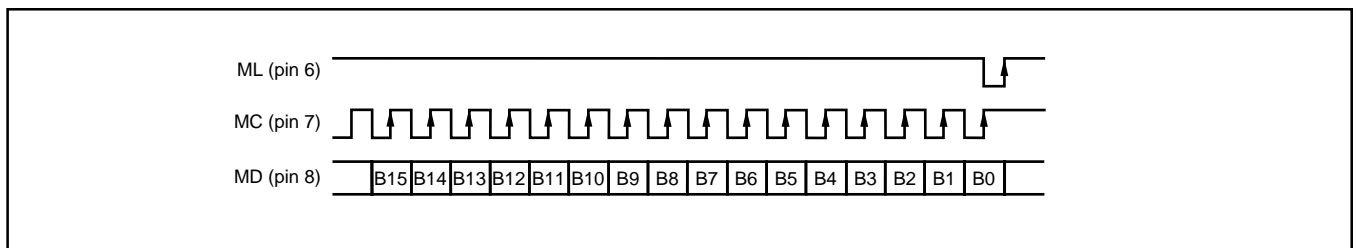


FIGURE 8. Three-Wire Serial Interface.

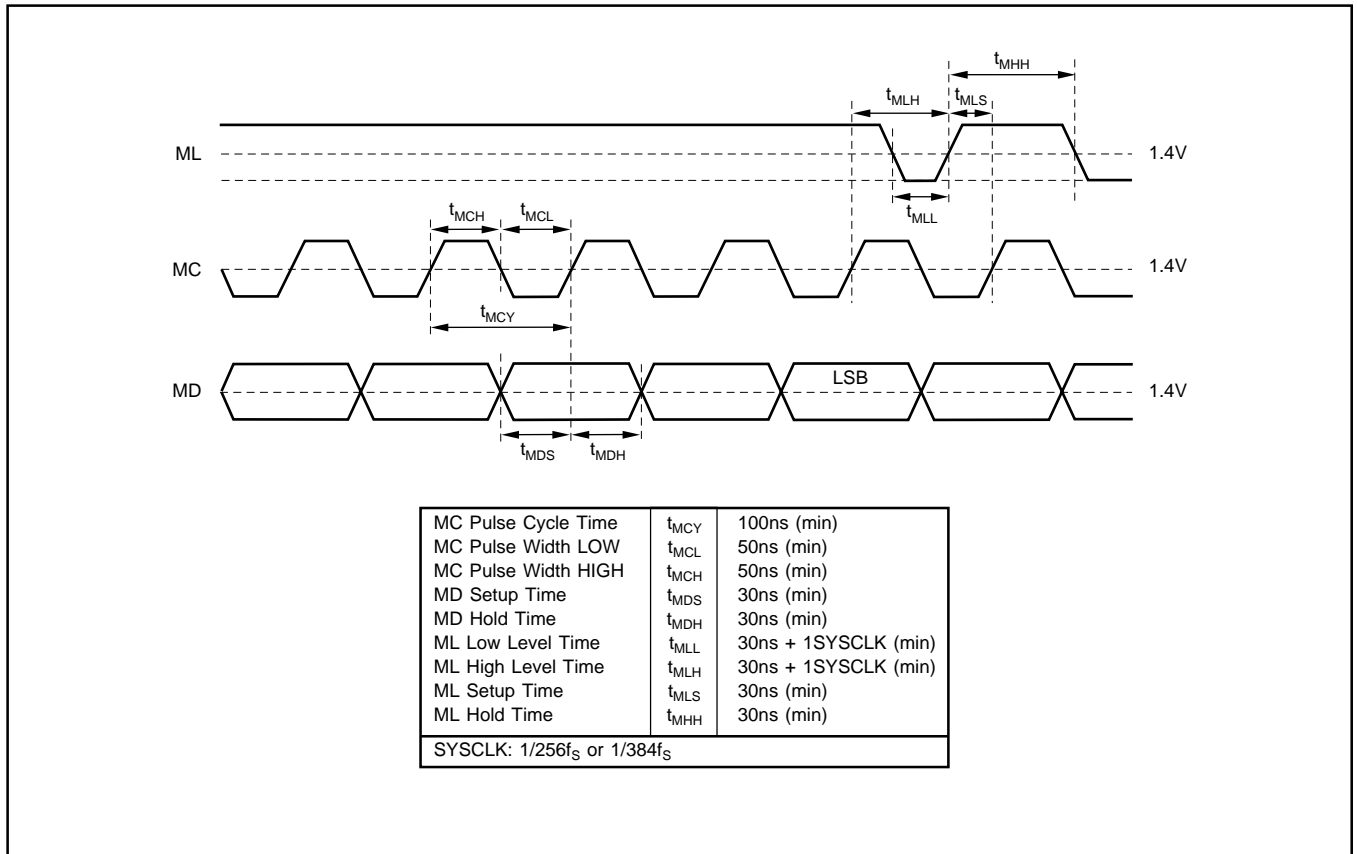


FIGURE 9. Program Register Input Timing.

APPLICATION CONSIDERATIONS

DELAY TIME

There is a finite delay time in delta-sigma converters. In analog-to-digital converters (ADCs), this is commonly referred to as latency. For a delta-sigma DAC, delay time is determined by the order number of the FIR filter stage, and the chosen sampling rate. The following equation expresses the delay time of PCM1723:

$$t_D = 11.125 \times 1/f_S$$

$$\text{For } f_S = 44.1\text{kHz, } t_D = 11.125/44.1\text{kHz} = 251.4\mu\text{s}$$

Applications using data from a disc or tape source, such as CD audio, CD-Interactive, Video CD, DAT, Minidisc, etc., generally are not affected by delay time. For some profes-

sional applications such as broadcast audio for studios, it is important for total delay time to be less than 2ms.

OUTPUT FILTERING

For testing purposes all dynamic tests are done on the PCM1723 using a 20kHz low-pass filter. This filter limits the measured bandwidth for THD+N, etc. to 20kHz. Failure to use such a filter will result in higher THD+N and lower SNR and Dynamic Range readings than are found in the specifications. The low-pass filter removes out of band noise. Although it is not audible, it may affect dynamic specification numbers.

The performance of the internal low-pass filter from DC to 24kHz is shown in Figure 10. The higher frequency rolloff of the filter is shown in Figure 11. If an application has the PCM1723 driving a wideband amplifier, it is recommended to use an external low-pass filter. A simple 3rd-order filter is shown in Figure 12. For some applications, a passive RC filter or 2nd-order filter may be adequate.

Reset

The PCM1723 has both internal power-on reset circuit and the $\overline{\text{RSTB}}$ pin (pin 9) that accepts an external forced reset by

$\overline{\text{RSTB}} = \text{LOW}$. For internal power on reset, initialize (reset) is done automatically at power on $V_{\text{DD}} > 2.2\text{V}$ (typ). During internal reset = LOW, the output of the DAC is invalid and the analog outputs are forced to $V_{\text{CC}}/2$. Figure 13 illustrates the timing of internal power on reset.

The PCM1723 accepts an external forced reset when $\overline{\text{RSTB}} = \text{L}$. During $\overline{\text{RSTB}} = \text{L}$, the output of the DAC is invalid and the analog outputs are forced to $V_{\text{CC}}/2$ after internal initialize (1024 system clocks count after $\overline{\text{RSTB}} = \text{H}$). Figure 14 illustrates the timing of $\overline{\text{RSTB}}$ pin reset.

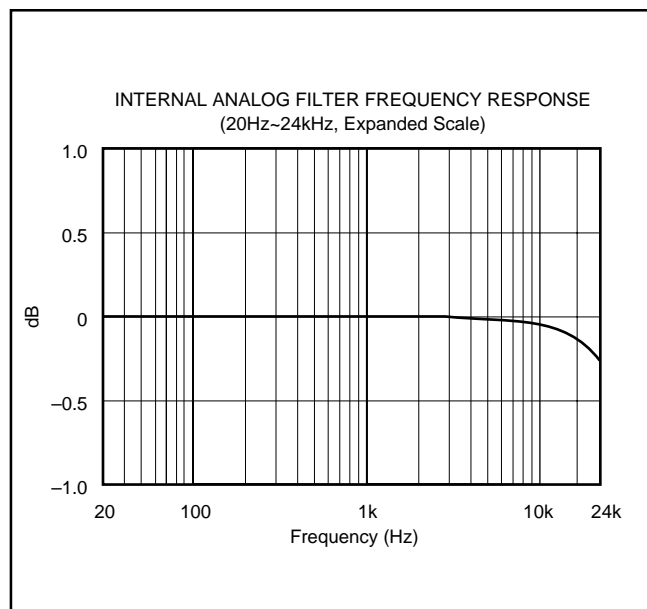


FIGURE 10. Low-Pass Filter Frequency Response.

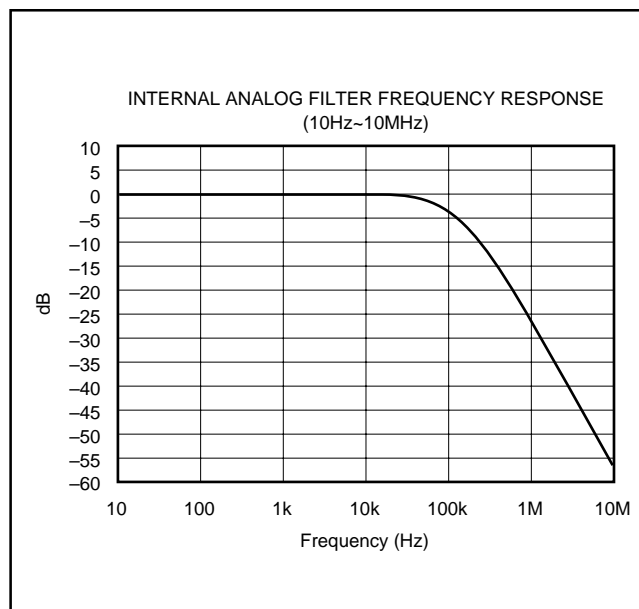


FIGURE 11. Low-Pass Filter Wideband Frequency Response.

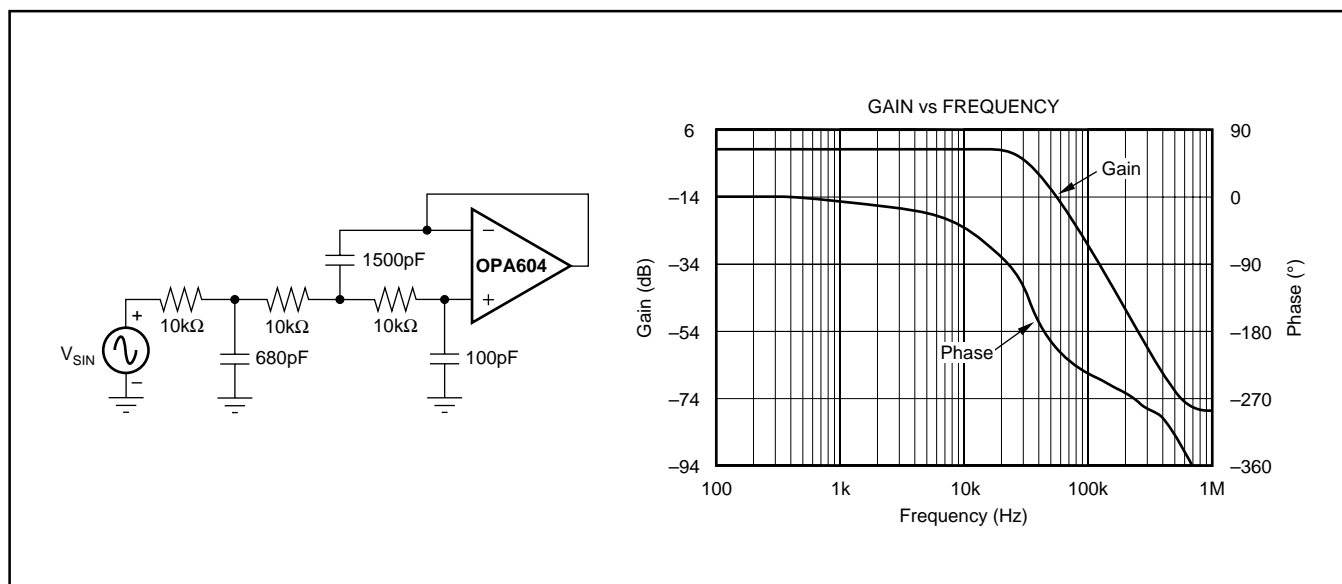


FIGURE 12. 3rd-Order Low-Pass Filter.

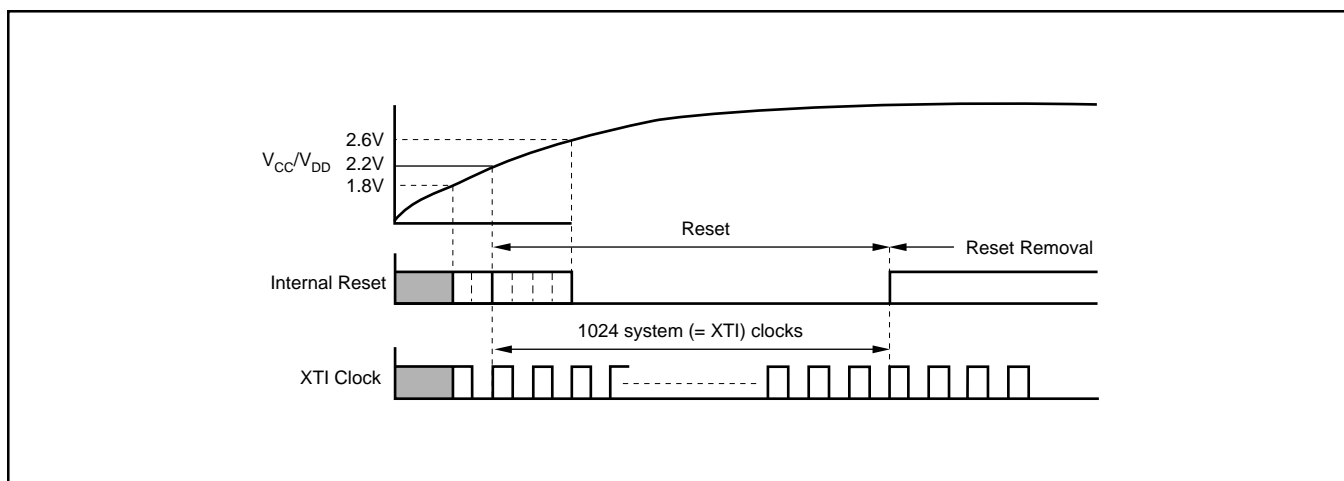


FIGURE 13. Internal Power-On Reset Timing.

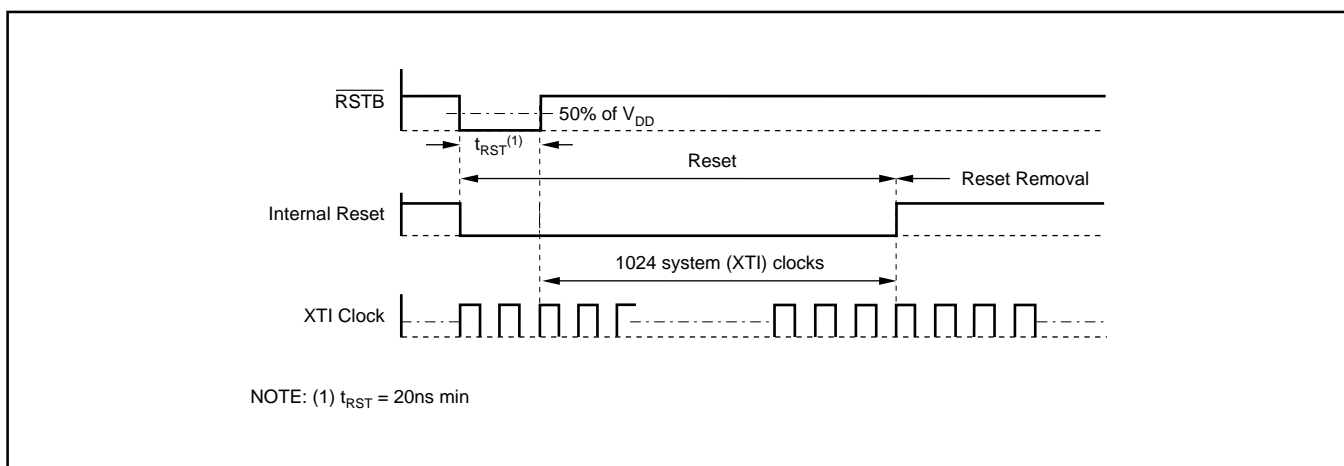


FIGURE 14. RSTB-Pin Reset Timing.

POWER SUPPLY CONNECTIONS

The PCM1723 has three power supply connections: digital (V_{DD}), analog (V_{CC}), and PLL (V_{CP}). Each connection also has a separate ground return pin. It is acceptable to use a common +5V power supply for all three power pins. If separate supplies are used without a common connection, the delta between the supplies during ramp-up time must be less than 0.6V. An application circuit to avoid a power-on latch-up condition is shown in Figure 15.

BYPASSING POWER SUPPLIES

The power supplies should be bypassed as close as possible to the unit. Refer to Figure 18 for optimal values of bypass capacitors. It is also recommended to include a 0.1 μ F ceramic capacitor in parallel with the 10 μ F tantalum capacitor.

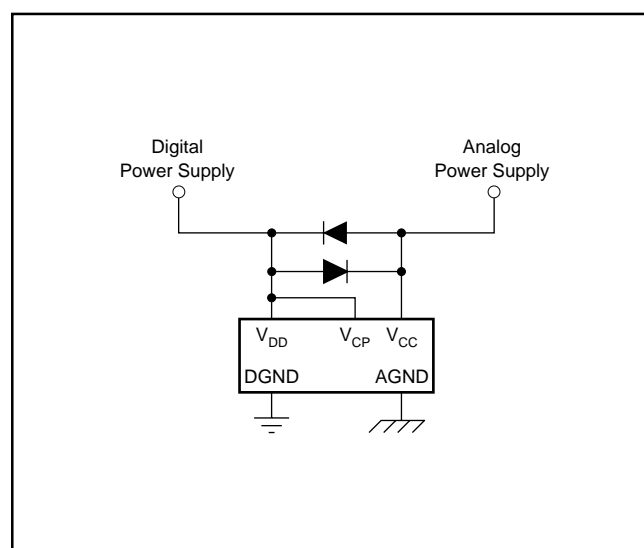


FIGURE 15. Latch-up Prevention Circuit.

THEORY OF OPERATION

The delta-sigma section of the PCM1723 is based on a 5-level amplitude quantizer and a 3rd-order noise shaper. This section converts the oversampled input data to 5-level delta-sigma format.

A block diagram of the 5-level delta-sigma modulator is shown in Figure 16. This 5-level delta-sigma modulator has the advantage of stability and clock jitter sensitivity over the typical one-bit (2 level) delta-sigma modulator.

The combined oversampling rate of the delta-sigma modulator and the internal 8X interpolation filter is $48f_s$ for a $384f_s$ system clock, and $64f_s$ for a $256f_s$ system clock. The theoretical quantization noise performance of the 5-level delta-sigma modulator is shown in Figure 17.



AC-3 APPLICATION CIRCUIT

A typical application for the PCM1723 is AC-3 5.1 channel audio decoding and playback. This circuit uses the PCM1723 to develop the audio system clock from the 27MHz video clock, with the SCKO pin used to drive the AC-3 decoder and two PCM1720 units, the non-PLL version of the PCM1723.

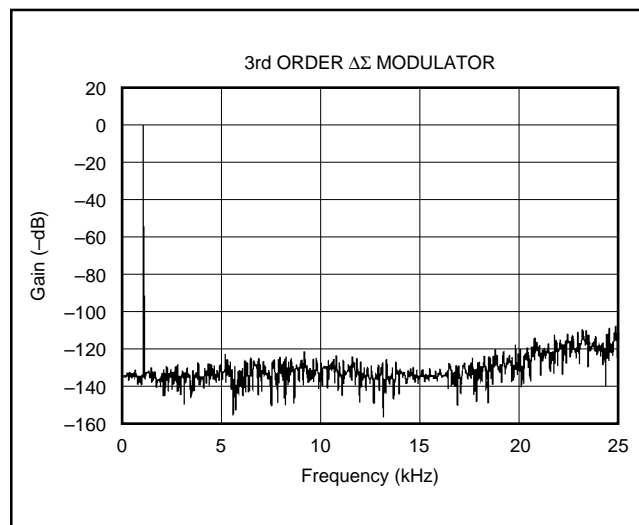


FIGURE 17. Quantization Noise Spectrum.

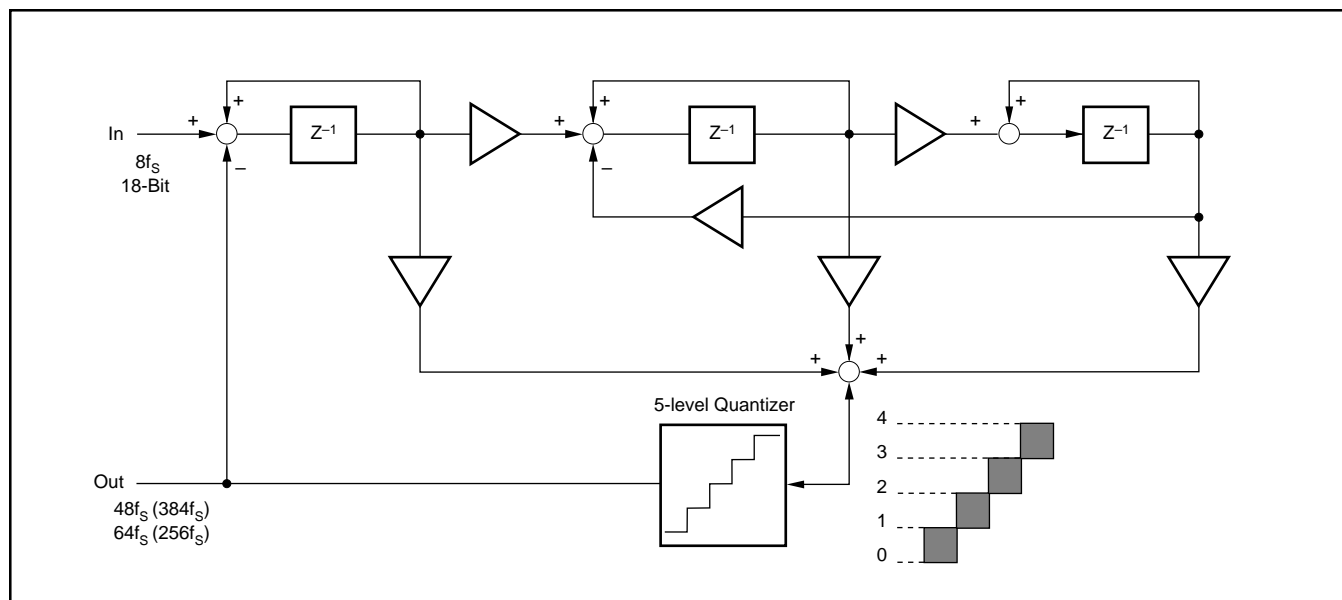


FIGURE 16. 5-Level $\Delta\Sigma$ Modulator Block Diagram.

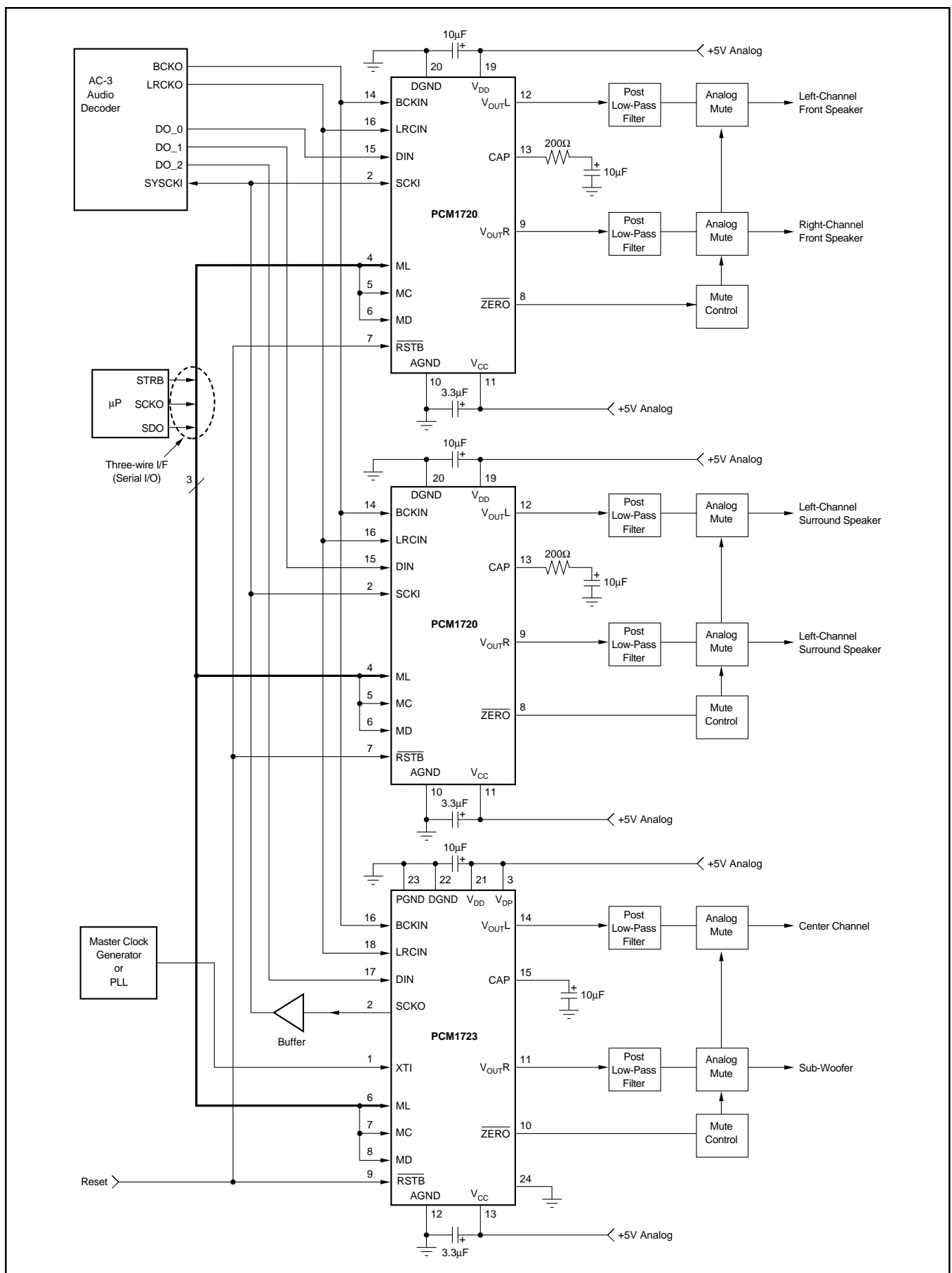


FIGURE 18. Connection Diagram for a 6-Channel AC-3 Application.

Revision History

| DATE | REVISION | PAGE | SECTION | DESCRIPTION |
|------|----------|------|----------------------------|--|
| 5/07 | A | — | Entire Document | Updated format and added missing overbars to RSTB and ZERO pins. |
| | | 2 | Electrical Characteristics | Added "Selectable" to <i>Audio Data Interface Format</i> typical value column. |
| | | | | Deleted "Selectable" from <i>Audio Data Format</i> unit column. |
| | | 6 | PLL Circuit | Changed "XTO should be connected" to "XTO must be connected." |
| | | | | Added sentence regarding XTI signal amplitude and C1, C2 determination. |
| | | | Figure 3 | Changed 2.0V/0.8V to 1.2V/0.4V. |
| | | 8 | PLL Circuit | Deleted paragraph regarding frequency error. |
| | | 10 | Register 3 | Added sentence to Bit 6 regarding interval time must be greater than 20μs. |

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|-----------------------------|---------------|----------------------|----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| PCM1723E | Active | Production | SSOP (DB) 24 | 58 TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -25 to 85 | PCM1723E |
| PCM1723E.B | Active | Production | SSOP (DB) 24 | 58 TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -25 to 85 | PCM1723E |
| PCM1723E/2K | Active | Production | SSOP (DB) 24 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -25 to 85 | PCM1723E |
| PCM1723E/2K.B | Active | Production | SSOP (DB) 24 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -25 to 85 | PCM1723E |

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| PCM1723E/2K | SSOP | DB | 24 | 2000 | 330.0 | 17.4 | 8.5 | 8.6 | 2.4 | 12.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-------------|--------------|-----------------|------|------|-------------|------------|-------------|
| PCM1723E/2K | SSOP | DB | 24 | 2000 | 336.6 | 336.6 | 28.6 |

TUBE



*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| PCM1723E | DB | SSOP | 24 | 58 | 500 | 10.6 | 500 | 9.6 |
| PCM1723E.B | DB | SSOP | 24 | 58 | 500 | 10.6 | 500 | 9.6 |

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

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