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Kind regards,

Team Nexperia

PDTA113E series

PNP resistor-equipped transistors; R1 = 1 kΩ, R2 = 1 kΩ

Rev. 05 — 2 September 2009 Product data sheet

1. Product profile

1.1 General description

PNP Resistor-Equipped Transistors (RET).

Table 1. Product overview

Type number	Package			NPN complement
	NXP	JEITA	JEDEC	
PDTA113EE	SOT416	SC-75	-	PDTC113EE
PDTA113EK	SOT346	SC-59A	TO-236	PDTC113EK
PDTA113EM	SOT883	SC-101	-	PDTC113EM
PDTA113ES[1]	SOT54 (TO-92)	SC-43A	TO-92	PDTC113ES
PDTA113ET	SOT23	-	TO-236AB	PDTC113ET
PDTA113EU	SOT323	SC-70	-	PDTC113EU

[1] Also available in SOT54A and SOT54 variant packages (see Section 2)

1.2 Features

- Built-in bias resistors
- Simplifies circuit design
- Reduces component count
- Reduces pick and place costs

1.3 Applications

- General purpose switching and amplification
- Inverter and interface circuits
- Circuit drivers

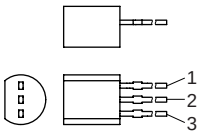
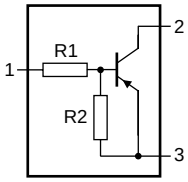
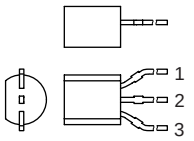
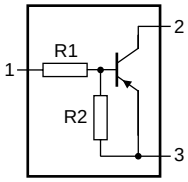
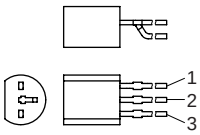
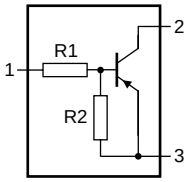
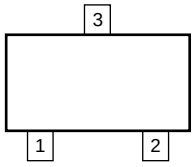
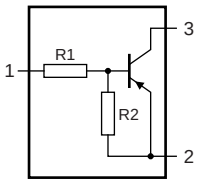
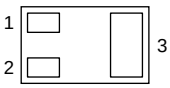
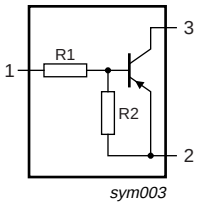
1.4 Quick reference data

Table 2. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CEO}	collector-emitter voltage	open base	-	-	–50	V
I_O	output current (DC)		-	-	–100	mA
R1	bias resistor 1 (input)		0.7	1	1.3	kΩ
R2/R1	bias resistor ratio		0.8	1	1.2	

2. Pinning information

Table 3. Pinning

Pin	Description	Simplified outline	Symbol
SOT54			
1	input (base)	 001aab347	 006aaa148
2	output (collector)		
3	GND (emitter)		
SOT54A			
1	input (base)	 001aab348	 006aaa148
2	output (collector)		
3	GND (emitter)		
SOT54 variant			
1	input (base)	 001aab447	 006aaa148
2	output (collector)		
3	GND (emitter)		
SOT23, SOT323, SOT346, SOT416			
1	input (base)	 006aaa144	 sym003
2	GND (emitter)		
3	output (collector)		
SOT883			
1	input (base)	 Transparent top view	 sym003
2	GND (emitter)		
3	output (collector)		

3. Ordering information

Table 4. Ordering information

Type number	Package		
	Name	Description	Version
PDTA113EE	SC-75	plastic surface mounted package; 3 leads	SOT416
PDTA113EK	SC-59A	plastic surface mounted package; 3 leads	SOT346
PDTA113EM	SC-101	leadless ultra small plastic package; 3 solder lands; body 1.0 × 0.6 × 0.5 mm	SOT883
PDTA113ES[1]	SC-43A	plastic single-ended leaded (through hole) package; 3 leads	SOT54
PDTA113ET	-	plastic surface mounted package; 3 leads	SOT23
PDTA113EU	SC-70	plastic surface mounted package; 3 leads	SOT323

[1] Also available in SOT54A and SOT54 variant packages (see Section 2 and Section 9).

4. Marking

Table 5. Marking codes

Type number	Marking code[1]
PDTA113EE	16
PDTA113EK	17
PDTA113EM	G4
PDTA113ES	TA113E
PDTA113ET	*15
PDTA113EU	*14

[1] * = -: made in Hong Kong
* = p: made in Hong Kong
* = t: made in Malaysia
* = W: made in China

5. Limiting values

Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CBO}	collector-base voltage	open emitter		-	–50	V
V_{CEO}	collector-emitter voltage	open base		-	–50	V
V_{EBO}	emitter-base voltage	open collector		-	–10	V
V_I	input voltage					
	positive			-	+10	V
	negative			-	–10	V
I_O	output current (DC)			-	–100	mA
I_{CM}	peak collector current			-	–100	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C				
	SOT416		[1]	-	150	mW
	SOT346		[1]	-	250	mW
	SOT883		[2][3]	-	250	mW
	SOT54		[1]	-	500	mW
	SOT23		[1]	-	250	mW
	SOT323		[1]	-	200	mW
T_{stg}	storage temperature			–65	+150	°C
T_j	junction temperature			-	150	°C
T_{amb}	ambient temperature			–65	+150	°C

[1] Refer to standard mounting conditions

[2] Reflow soldering is the only recommended soldering method.

[3] Refer to SOT883 standard mounting conditions; FR4 printed-circuit board with 60 μm copper strip line.

6. Thermal characteristics

Table 7. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air					
	SOT416		[1]	-	-	833	K/W
	SOT346		[1]	-	-	500	K/W
	SOT883		[2][3]	-	-	500	K/W
	SOT54		[1]	-	-	250	K/W
	SOT23		[1]	-	-	500	K/W
	SOT323		[1]	-	-	625	K/W

[1] Refer to standard mounting conditions.

[2] Reflow soldering is the only recommended soldering method.

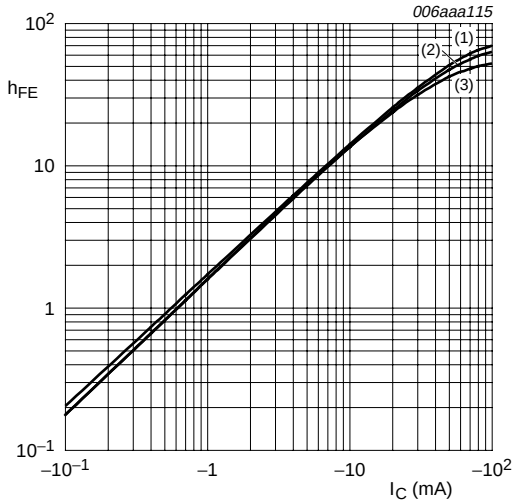
[3] Refer to SOT883 standard mounting conditions; FR4 printed-circuit board with 60 μm copper strip line.

7. Characteristics

Table 8. Characteristics

T_{amb} = 25 °C unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{CBO}	collector-base cut-off current	V_{CB} = –50 V; I_E = 0 A	-	-	–100	nA
I_{CEO}	collector-emitter cut-off current	V_{CE} = –30 V; I_B = 0 A	-	-	–1	µA
		V_{CE} = –30 V; I_B = 0 A; T_j = 150 °C	-	-	–50	µA
I_{EBO}	emitter-base cut-off current	V_{EB} = –5 V; I_C = 0 A	-	-	–4	mA
h_{FE}	DC current gain	V_{CE} = –5 V; I_C = –40 mA	30	-	-	
V_{CEsat}	collector-emitter saturation voltage	I_C = –30 mA; I_B = –1.5 mA	-	-	–150	mV
$V_{I(off)}$	off-state input voltage	V_{CE} = –5 V; I_C = –100 µA	-	–1.3	–0.5	V
$V_{I(on)}$	on-state input voltage	V_{CE} = –300 mV; I_C = –20 mA	–2	–1.7	-	V
R1	bias resistor 1 (input)		0.7	1	1.3	kΩ
R2/R1	bias resistor ratio		0.8	1	1.2	
C_c	collector capacitance	V_{CB} = –10 V; I_E = i_e = 0 A; f = 1 MHz	-	-	2	pF



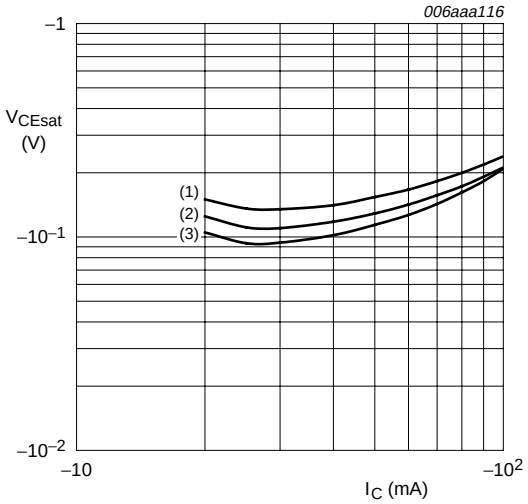
V_{CE} = −5 V

(1) T_{amb} = 100 °C

(2) T_{amb} = 25 °C

(3) T_{amb} = −40 °C

Fig 1. DC current gain as a function of collector current; typical values



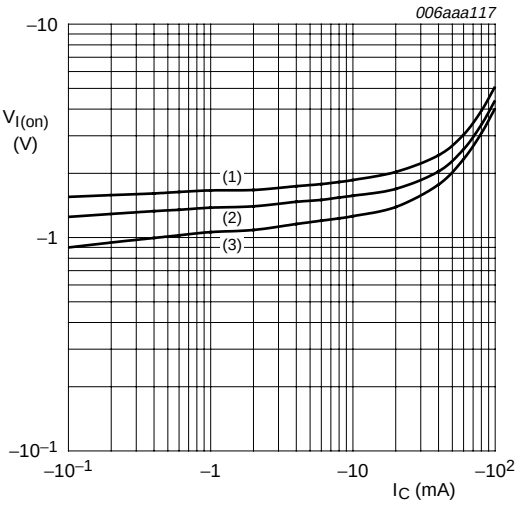
I_C/I_B = 20

(1) T_{amb} = 100 °C

(2) T_{amb} = 25 °C

(3) T_{amb} = −40 °C

Fig 2. Collector-emitter saturation voltage as a function of collector current; typical values



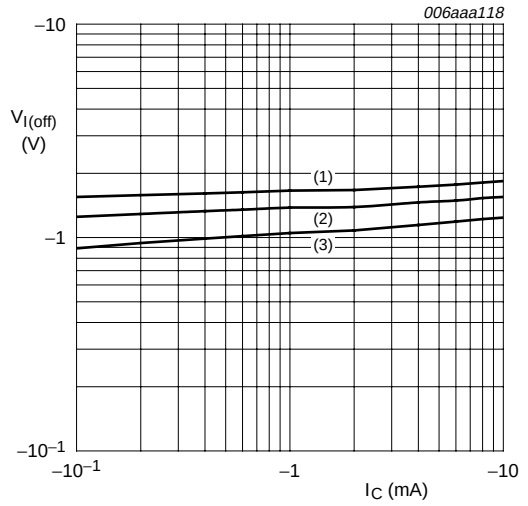
V_{CE} = −0.3 V

(1) T_{amb} = −40 °C

(2) T_{amb} = 25 °C

(3) T_{amb} = 100 °C

Fig 3. On-state input voltage as a function of collector current; typical values



V_{CE} = −5 V

(1) T_{amb} = −40 °C

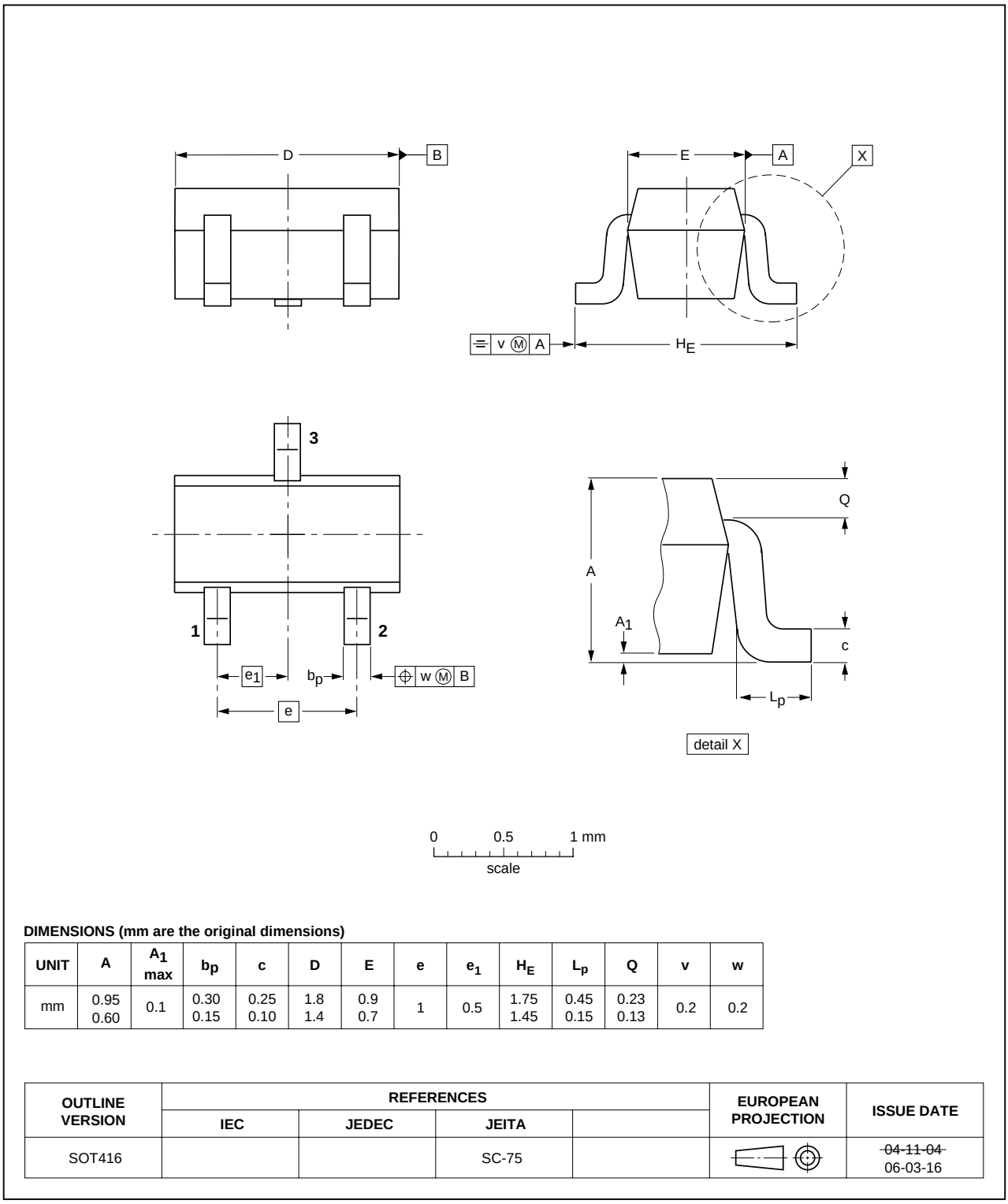
(2) T_{amb} = 25 °C

(3) T_{amb} = 100 °C

Fig 4. Off-state input voltage as a function of collector current; typical values

8. Package outline

Plastic surface-mounted package; 3 leads **SOT416**



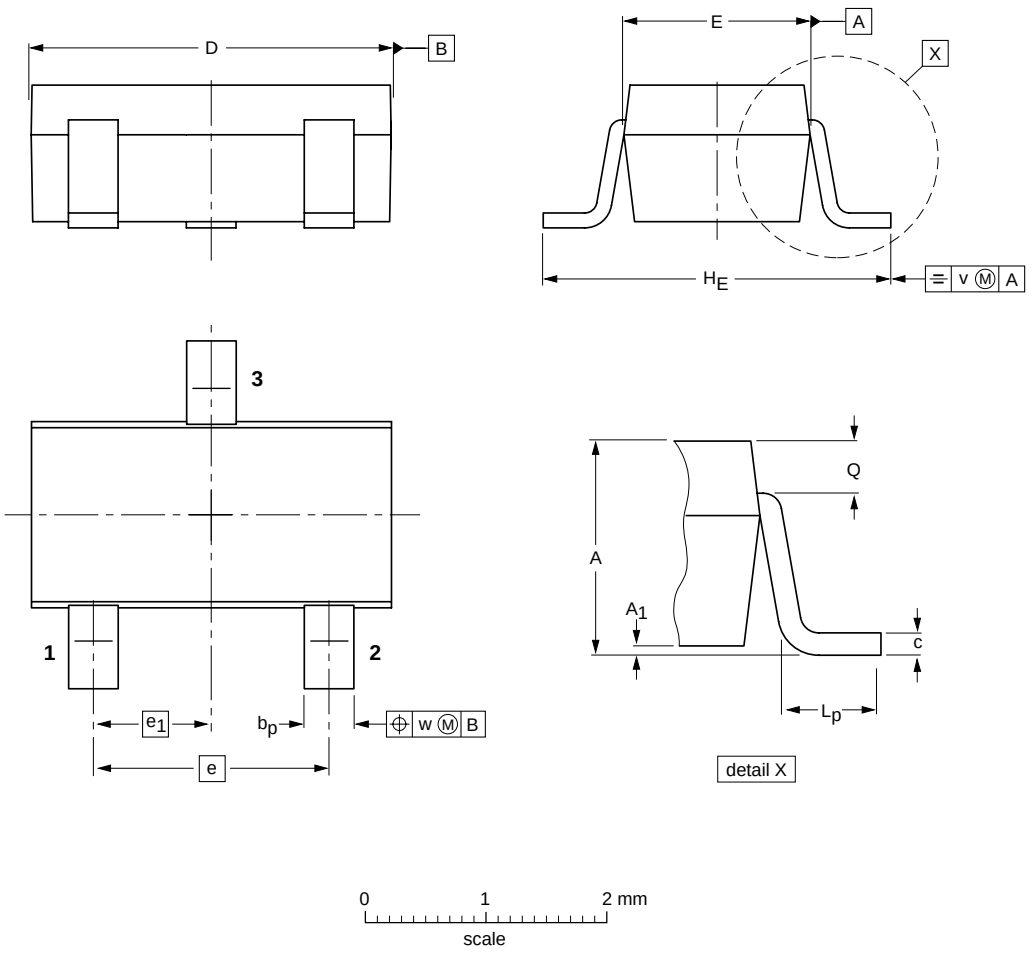
DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1 max	b_p	c	D	E	e	e_1	H_E	L_p	Q	v	w
mm	0.95 0.60	0.1	0.30 0.15	0.25 0.10	1.8 1.4	0.9 0.7	1	0.5	1.75 1.45	0.45 0.15	0.23 0.13	0.2	0.2

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT416			SC-75			~~04-11-04~~ 06-03-16

Fig 5. Package outline SOT416 (SC-75)

Plastic surface-mounted package; 3 leads **SOT346**



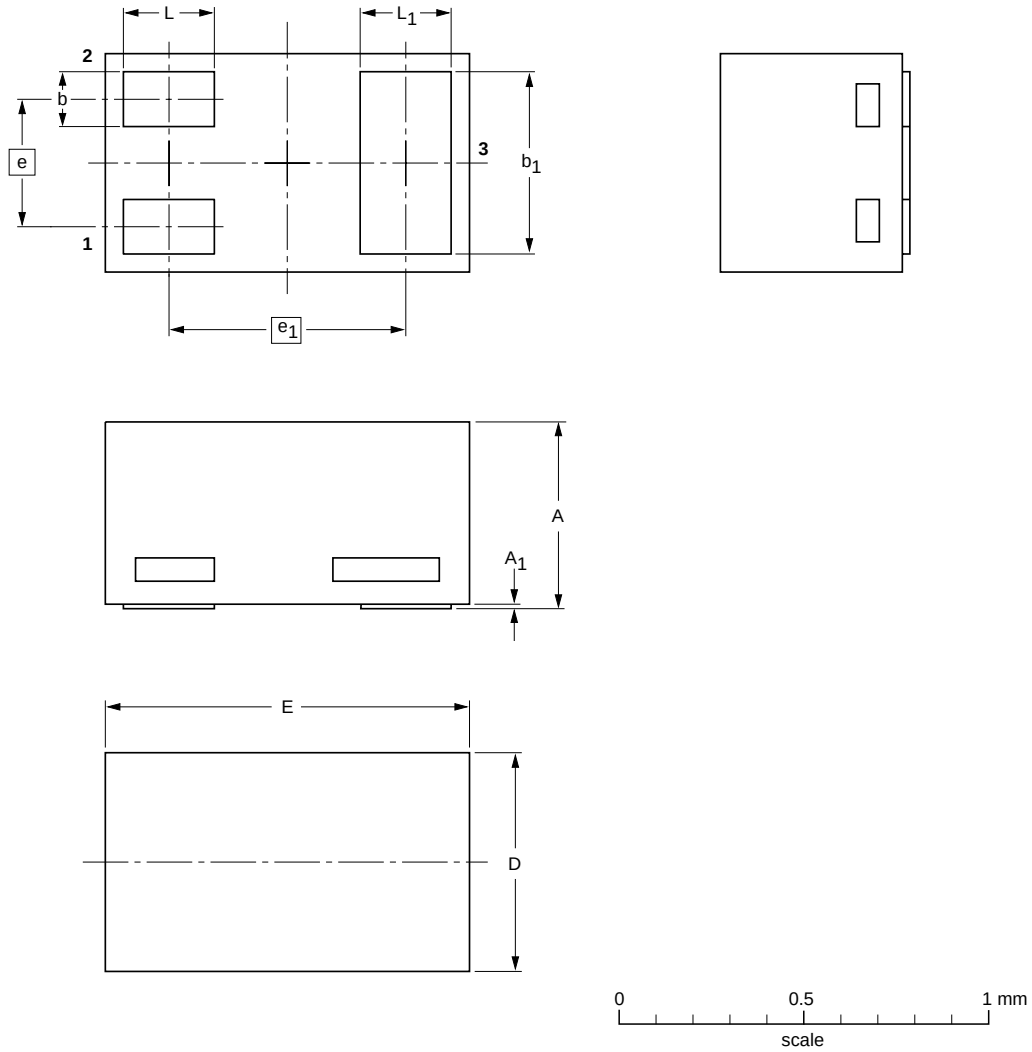
DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b_p	c	D	E	e	e_1	H_E	L_p	Q	v	w
mm	1.3 1.0	0.1 0.013	0.50 0.35	0.26 0.10	3.1 2.7	1.7 1.3	1.9	0.95	3.0 2.5	0.6 0.2	0.33 0.23	0.2	0.2

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT346		TO-236	SC-59A			~~04-11-11~~ 06-03-16

Fig 6. Package outline SOT346 (SC-59A/TO-236)

Leadless ultra small plastic package; 3 solder lands; body 1.0 x 0.6 x 0.5 mm **SOT883**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1)	A1 max.	b	b1	D	E	e	e1	L	L1
mm	0.50 0.46	0.03	0.20 0.12	0.55 0.47	0.62 0.55	1.02 0.95	0.35	0.65	0.30 0.22	0.30 0.22

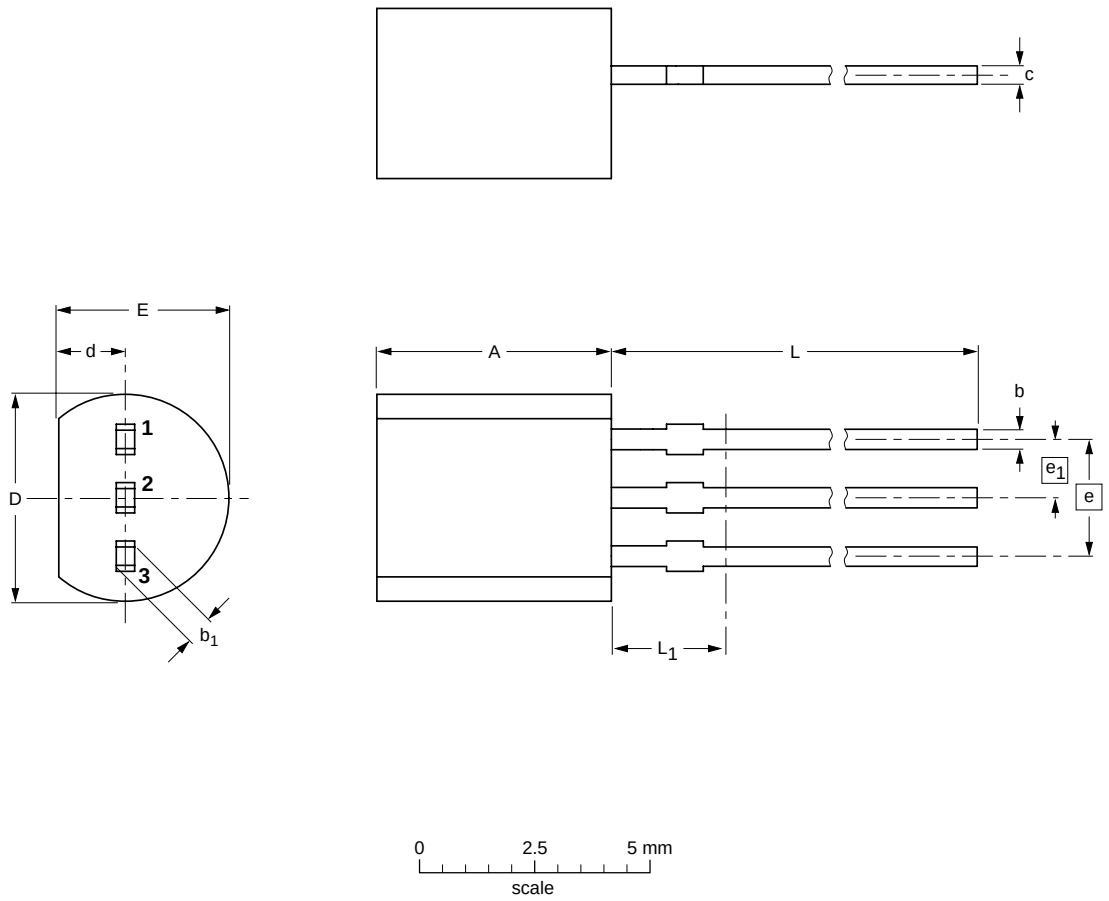
Note

1. Including plating thickness

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT883			SC-101			~~03-02-05~~ 03-04-03

Fig 7. Package outline SOT883 (SC-101)

Plastic single-ended leaded (through hole) package; 3 leads **SOT54**



DIMENSIONS (mm are the original dimensions)

UNIT	A	b	b_1	c	D	d	E	e	e_1	L	L_1 (1) max.
mm	5.2 5.0	0.48 0.40	0.66 0.55	0.45 0.38	4.8 4.4	1.7 1.4	4.2 3.6	2.54	1.27	14.5 12.7	2.5

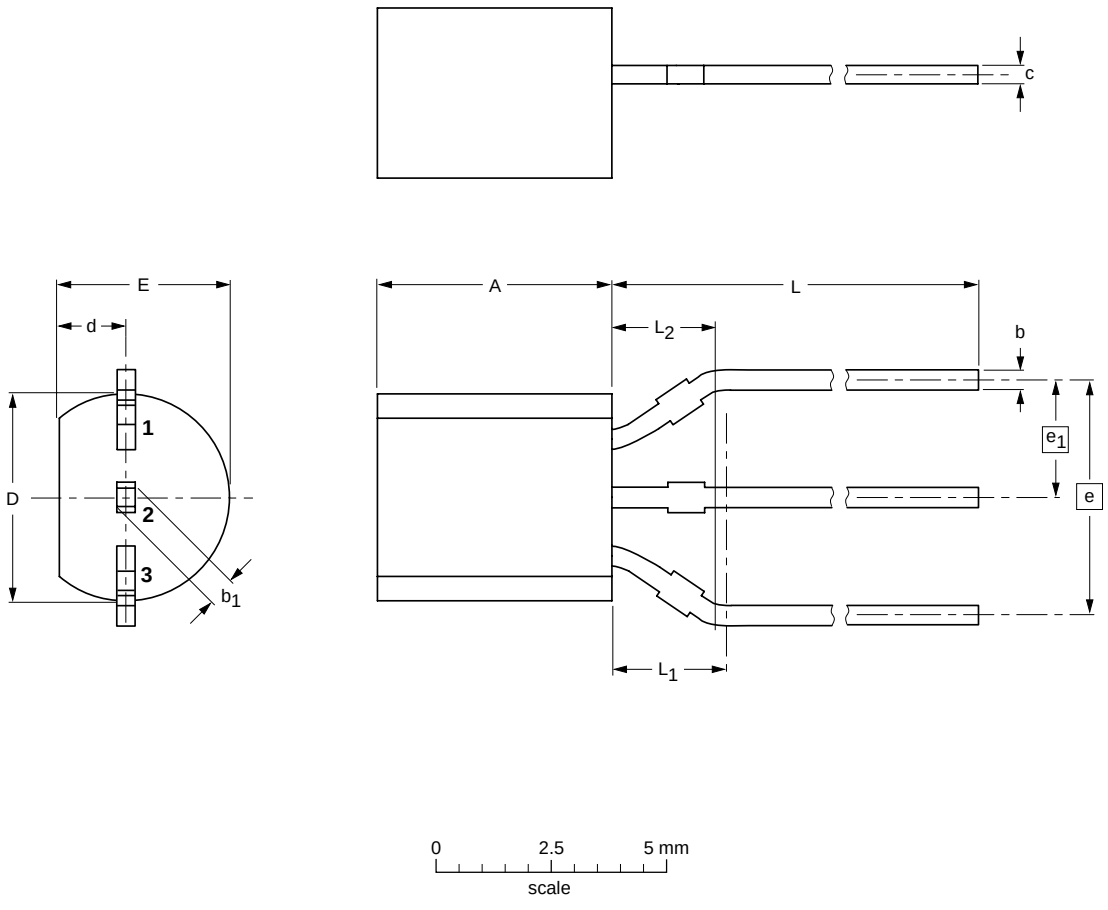
Note

1. Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT54		TO-92	SC-43A			~~04-06-28~~ 04-11-16

Fig 8. Package outline SOT54 (SC-43A/TO-92)

Plastic single-ended leaded (through hole) package; 3 leads (wide pitch) **SOT54A**



DIMENSIONS (mm are the original dimensions)

UNIT	A	b	b_1	c	D	d	E	e	e_1	L	L_1 (1) max.	L_2
mm	5.2 5.0	0.48 0.40	0.66 0.55	0.45 0.38	4.8 4.4	1.7 1.4	4.2 3.6	5.08	2.54	14.5 12.7	3	3 2

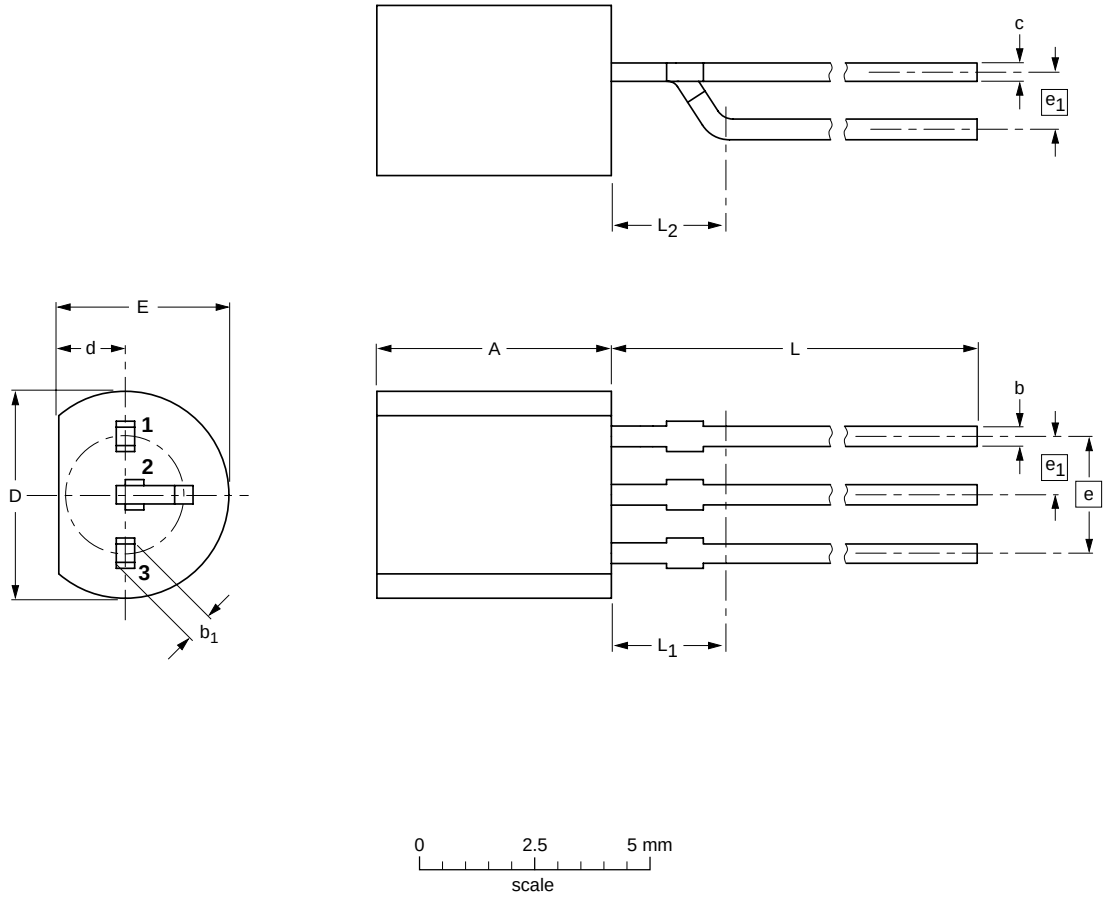
Note

1. Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT54A						~~97-05-13~~ 04-06-28

Fig 9. Package outline SOT54A

Plastic single-ended leaded (through hole) package; 3 leads (on-circle) **SOT54 variant**



DIMENSIONS (mm are the original dimensions)

UNIT	A	b	b_1	c	D	d	E	e	e_1	L	L_1 (1) max	L_2 max
mm	5.2 5.0	0.48 0.40	0.66 0.55	0.45 0.38	4.8 4.4	1.7 1.4	4.2 3.6	2.54	1.27	14.5 12.7	2.5	2.5

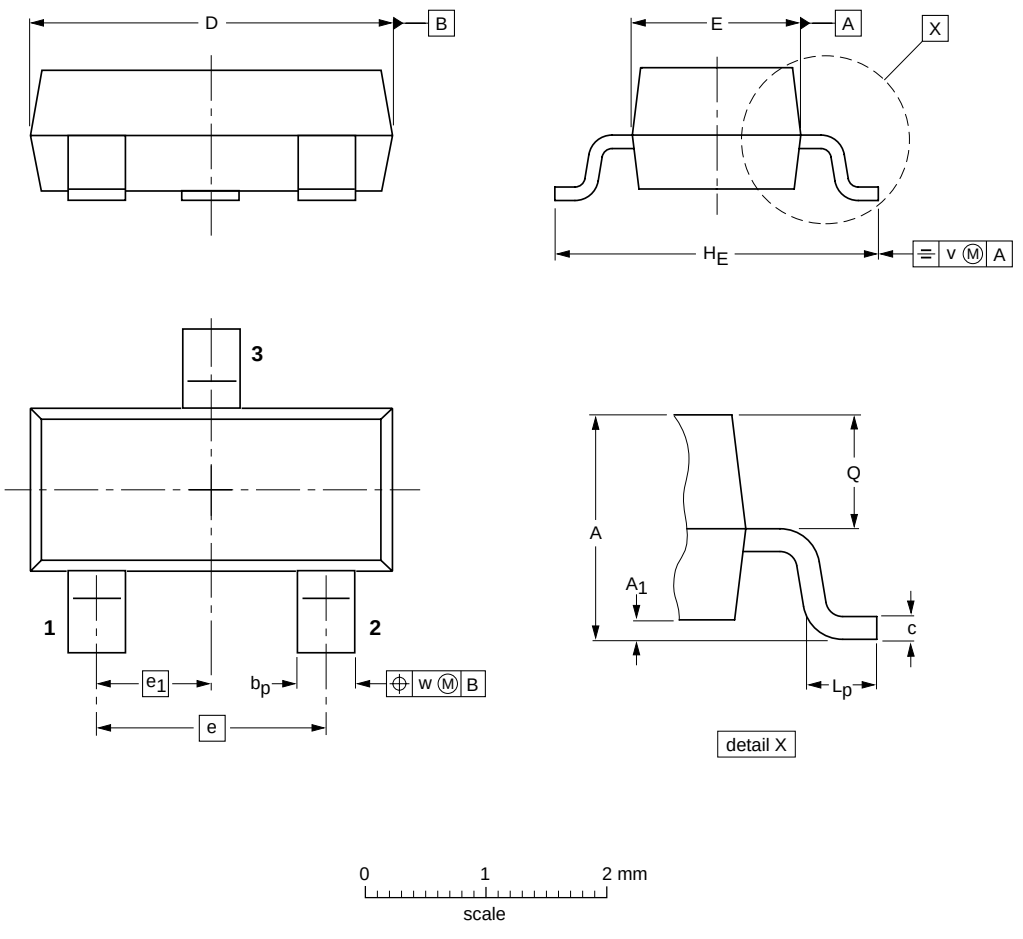
Note

1. Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT54 variant						~~04-06-28~~ 05-01-10

Fig 10. Package outline SOT54 variant

Plastic surface-mounted package; 3 leads **SOT23**



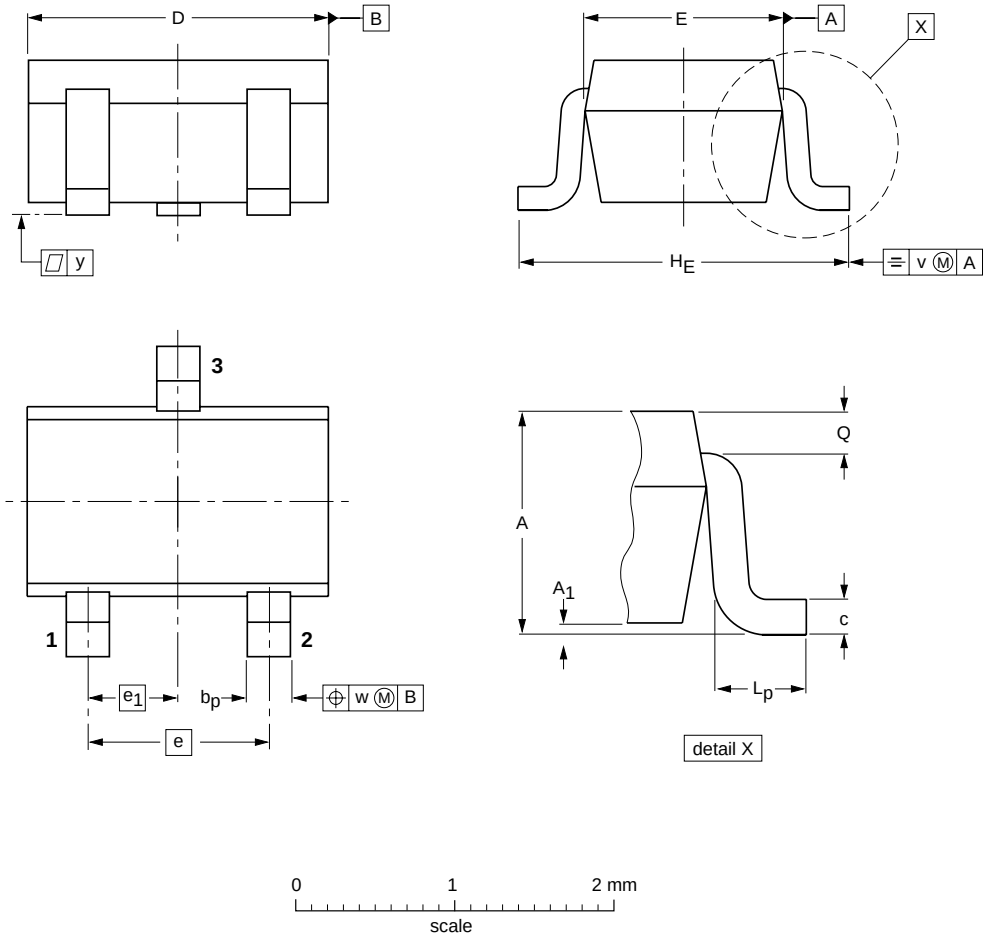
DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1 max.	b_p	c	D	E	e	e_1	H_E	L_p	Q	v	w
mm	1.1 0.9	0.1	0.48 0.38	0.15 0.09	3.0 2.8	1.4 1.2	1.9	0.95	2.5 2.1	0.45 0.15	0.55 0.45	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT23		TO-236AB				~~04-11-04~~ 06-03-16

Fig 11. Package outline SOT23 (TO-236AB)

Plastic surface-mounted package; 3 leads **SOT323**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1 max	b_p	c	D	E	e	e_1	H_E	L_p	Q	v	w
mm	1.1 0.8	0.1	0.4 0.3	0.25 0.10	2.2 1.8	1.35 1.15	1.3	0.65	2.2 2.0	0.45 0.15	0.23 0.13	0.2	0.2

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT323			SC-70			~~04-11-04~~ 06-03-16

Fig 12. Package outline SOT323 (SC-70)

9. Packing information

Table 9. Packing methods

The indicated -xxx are the last three digits of the 12NC ordering code. [1]

Type number	Package	Description	Packing quantity		
			3000	5000	10000
PDTA113EE	SOT416	4 mm pitch, 8 mm tape and reel	-115	-	-135
PDTA113EK	SOT346	4 mm pitch, 8 mm tape and reel	-115	-	-135
PDTA113EM	SOT883	2 mm pitch, 8 mm tape and reel	-	-	-315
PDTA113ES	SOT54	bulk, straight leads	-	-412	-
	SOT54A	tape and reel, wide pitch	-	-	-116
	SOT54A	tape ammopack, wide patch	-	-	-126
	SOT54 variant	bulk, delta pinning	-	-112	-
PDTA113ET	SOT23	4 mm pitch, 8 mm tape and reel	-215	-	-235
PDTA113EU	SOT323	4 mm pitch, 8 mm tape and reel	-115	-	-135

[1] For further information and the availability of packing methods, see Section 12.

10. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PDTA113E_SER_5	20090902	Product data sheet	-	PDTA113E_SER_4
Modifications:	• This data sheet was changed to reflect the new company name NXP Semiconductors, including new legal definitions and disclaimers. No changes were made to the technical content. • Figure 5 “Package outline SOT416 (SC-75)” updated • Figure 6 “Package outline SOT346 (SC-59A/TO-236)” updated • Figure 11 “Package outline SOT23 (TO-236AB)” updated • Figure 12 “Package outline SOT323 (SC-70)” updated			
PDTA113E_SER_4	20050405	Product data sheet	-	PDTA113ET_3
PDTA113ET_3	20040720	Objective data sheet	-	PDTA113ET_2
PDTA113ET_2	20040415	Objective data sheet	-	PDTA113ET_1
PDTA113ET_1	20040316	Objective data sheet	-	-

11. Legal information

11.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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