STEL-2030C
Data Sheet

STEL-2030C
17 Mbps
Convolutional Encoder
Viterbi Decoder

FEATURES

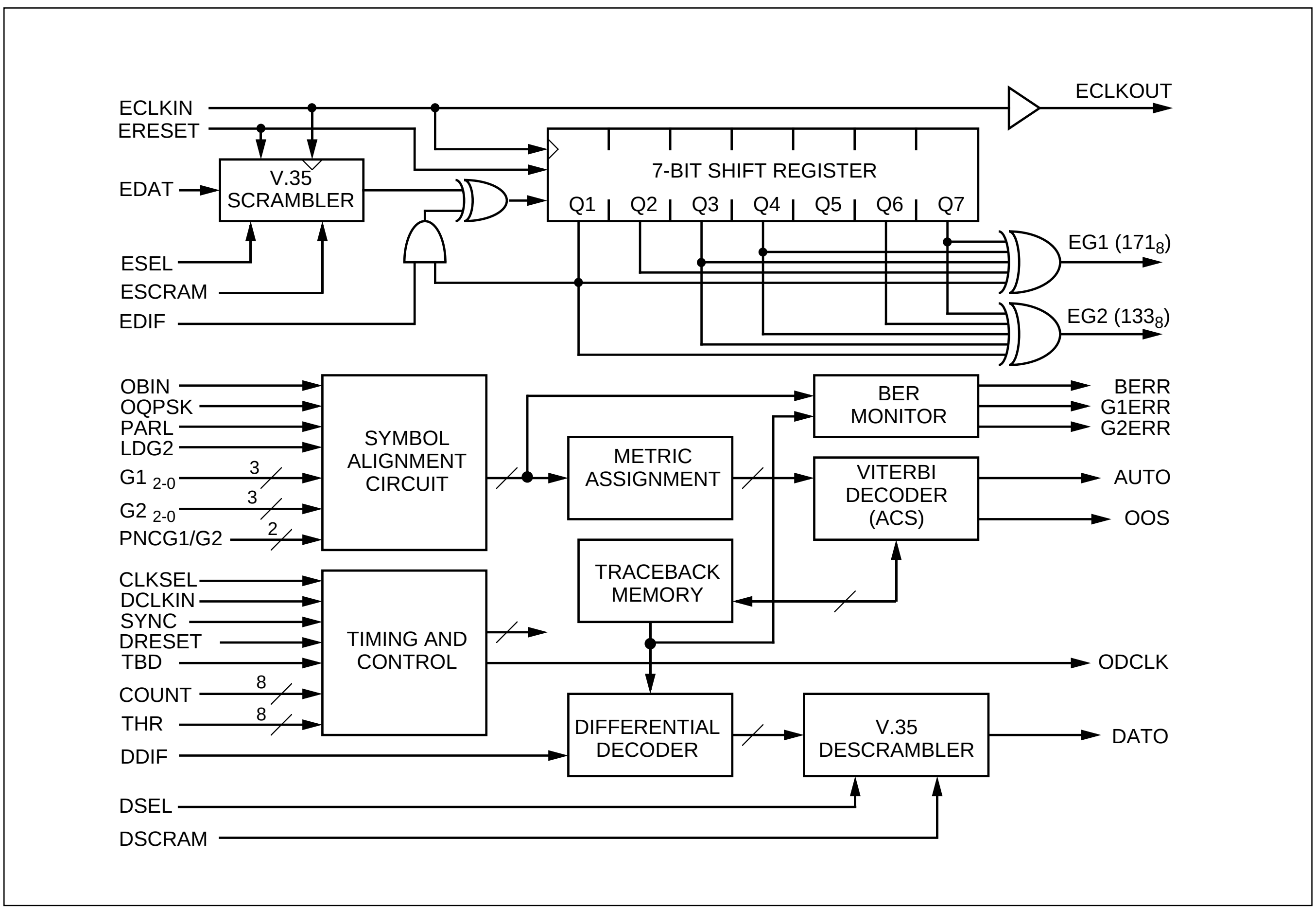
- **17 Mbps MAX. OPERATING DATA RATE**
- **CONSTRAINT LENGTH K = 7**
  $G_1 = 171_8$, $G_2 = 133_8$
- **MULTIPLE DEVICES CAN BE MULTIPLEXED TO GIVE HIGHER DATA RATES**
- **OPTIMIZED INTERFACE TO OPERATE WITH BPSK, QPSK, AND OQPSK DEMODULATORS**
- **V.35 SCRAMBLER AND DESCRAMBLER WITH CCITT AND IESS OPTIONS**
- **DIFFERENTIAL ENCODER AND DECODER**
- **AUTO NODE SYNC CAPABILITY**
- **INTERNAL BER MONITOR**
- **MULTIPLE RATES:**
  R = $^1/_2$, $^2/_3$*, $^3/_4$* (* Punctured codes)
- **INTERNAL PUNCTURING CAPABILITY**
- **5.2 dB CODING GAIN @10^{-5} BER**
- **84-PIN PLCC PACKAGE**

FUNCTIONAL DESCRIPTION

Convolutional Encoding and Viterbi Decoding are used to provide forward error correction (FEC) which improves digital communication performance over a noisy link. In satellite communication systems where transmitter power is limited, FEC techniques can reduce the required transmission power. The STEL-2030C is a specialized product designed to perform this specific communications related function. It is functionally identical to the previously available STEL-2030B, which it replaces.

The encoder creates a stream of symbols which are transmitted at twice the information rate. This encoding introduces a high degree of redundancy which enables accurate decoding of the information despite a high symbol error rate resulting from a noisy communications link.

BLOCK DIAGRAM



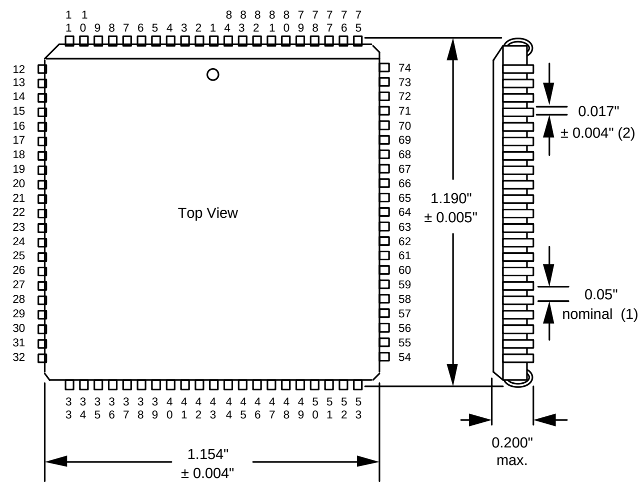
The STEL-2030C contains a K = 7 convolutional encoder and Viterbi decoder (including differential, as well as direct encoding/decoding) capable of fully independent (full duplex) operation, with completely independent data clocks. At the decoder the symbol input format can be either serial, i.e., sequential symbols, (typically for BPSK applications) or parallel (typically for QPSK and OQPSK applications).

The data inputs can be in offset binary or offset signed magnitude formats, with 3-bit soft decision. Auto node sync and a BER monitor are also provided in the device. Rate $^{2}/_{3}$ and $^{3}/_{4}$ punctured signals can be encoded and decoded, as well as non-punctured, Rate $^{1}/_{2}$, signals. The polynomials used are industry standards.

PIN CONFIGURATION

Package: 84-pin PLCC

Thermal coefficient, θ_{ia} = 30° C/W



Notes: (1) Tolerances on pin spacing are not cumulative

(2) Dimensions at seating plane

PIN CONNECTIONS

1	V_{DD}	18	EDAT	35	PARL	52	N.C.	69	DATO
2	V_{SS}	19	V_{DD}	36	OQPSK	53	V_{SS}	70	V_{DD}
3	THR_0	20	DRESET	37	V_{SS}	54	I.C.	71	V_{SS}
4	THR_1	21	DCLKIN	38	DSCRAM	55	N.C.	72	EG2
5	THR_2	22	V_{SS}	39	DSEL	56	N.C.	73	EG1
6	THR_3	23	PNCG2	40	DDIF	57	V_{SS}	74	ECLKOUT
7	THR_4	24	$G2_0$	41	TBD	58	V_{DD}	75	V_{SS}
8	V_{SS}	25	$G2_1$	42	V_{SS}	59	OOS	76	$COUNT_0$
9	THR_5	26	$G2_2$	43	N.C.	60	AUTO	77	$COUNT_1$
10	THR_6	27	PNCG1	44	V_{DD}	61	N.C.	78	$COUNT_2$
11	THR_7	28	V_{SS}	45	CLKSEL	62	N.C.	79	$COUNT_3$
12	ECLKIN	29	$G1_0$	46	V_{DD}	63	V_{SS}	80	V_{SS}
13	EDIF	30	$G1_1$	47	V_{DD}	64	BERR	81	$COUNT_4$
14	ESCRAM	31	$G1_2$	48	N.C.	65	V_{DD}	82	$COUNT_5$
15	ESEL	32	LDG2	49	N.C.	66	G2ERR	83	$COUNT_6$
16	V_{SS}	33	SYNC	50	V_{DD}	67	G1ERR	84	$COUNT_7$
17	ERESET	34	OBIN	51	V_{SS}	68	ODCLK		

Notes: I.C. denotes Internal Connection. These pins must be left unconnected. Do not use for vias.

N.C. denotes No Connection. These pins can be used for vias.

ENCODER OPERATION

The convolutional coder is functionally independent from the decoder. A single data bit is clocked into the 7-bit shift register on the rising edge of **ECLKIN**. Two symbols, G1 and G2, are generated and are brought out on separate pins, **EG1** and **EG2**.

DECODER OPERATION

The decoder section of the STEL-2030C implements the Viterbi algorithm for decoding convolutionally encoded data. It incorporates many unique features which enhance its capabilities and flexibility. The incoming symbols can be accepted either sequentially, as would be the case in a BPSK system, or in parallel, as would be the case in a QPSK system. In addition, a special circuit takes care of symbol alignment in an Offset QPSK (OQPSK) system. The signals can be in either offset binary or signed magnitude codes. In both cases the codes are offset from zero by half a quantization level, giving the same number of allowable states in both the positive and negative directions.

The Viterbi decoder itself uses the add/compare/select algorithm to determine the most likely value for each bit from the trellis created from the received symbols. Five-bit arithmetic is used to maximize the performance with the three-bit soft-decision data inputs. The decoder contains many user controlled features which enhance its performance in different environments. The depth of the trace-back used can be set to the long mode (70 states) for optimum performance in the punctured modes (R = $^2/_3$, $^3/_4$, $^7/_8$), or to the short mode (38 states) in normal mode (R = $^1/_2$). (The penalty for using the longer trace-back length is the additional delay in decoding the data.) A built-in counter estimates the probability of incorrect node synchronization from the error rate. A user selectable feedback loop allows the node synchronization to be corrected automatically, and the device also features a built-in bit error-rate (BER) monitor circuit as well as a V.35 descrambler. The true CCITT V.35 algorithm is supported as well as the IESS version of this algorithm.

INPUT SIGNALS

ERESET

Encoder **Reset**. A logic low on this asynchronous input will completely reset all internal registers in the encoder to an initial condition within 100 nanoseconds. This sets the encoder state to all zeroes.

ECLKIN

The transmit clock is the **e**ncoder system **cl**oc**k**. The maximum **ECLKIN** frequency is 17 MHz. There is no minimum frequency. Data is latched into the encoder on the falling edges of this clock.

EDAT

The **e**ncoder input **dat**a is connected to this input. The data is clocked in on the falling edge of the **ECLKIN** signal.

EDIF

When the **EDIF** signal is set high it enables the **dif**ferential encoder circuit. When it is set low this circuit will be disabled, and normal, non-differential data will be loaded into the convolutional encoder.

ESCRAM

When this input is set high it causes the **e**ncoded data to be **scram**bled before being differentially encoded and before being convolutionally encoded. The scrambling algorithm used is the standard CCITT or IESS V.35 algorithms according to the setting of **ESEL**.. When **ESCRAM** is set low the scrambler function will be inhibited.

ESEL

When this input is set low the CCITT compatible mode is selected for the V.35 scrambler in the encoder, and when it is set high the IESS compatible mode is selected.

DRESET

Decoder **Reset**. A logic low on this asynchronous input will completely reset all registers in the decoder to an initial condition within 3 clock cycles. This will not affect the values stored in the decision path memory.

DCLKIN

Decoder **clock in**put. It is the reference clock for all internal synchronous functions in the decoder. It should nominally be a square wave. When **CLKSEL** is set low the **DCLKIN** signal should be at twice the frequency of the input symbols, with a maximum frequency of 68 MHz when **PARL** = 0 and 34 MHz when **PARL** = 1, corresponding to a decoded data rate of 17 Mbps. When **CLKSEL** is set high the **DCLKIN** signal should be at the same frequency as the input symbols, with a maximum frequency of 20 MHz when **PARL** = 0 and 10 MHz when **PARL** = 1, corresponding to a decoded data rate of 10 Mbps.

$G1_{2-0}$, $G2_{2-0}$

The $\mathbf{G1_{2-0}}$ and $\mathbf{G2_{2-0}}$ signals are the 3-bit soft decision input symbols to the decoder. They are presented to the decoder either sequentially or in parallel depending on the state of the **PARL** signal. In the parallel mode (**PARL** = 1) the symbols are clocked into the device on the falling edge of **DCLKIN** (alternate edges only when **CLKSEL** = 0). In the sequential mode (**PARL** = 0) the $\mathbf{G2_{2-0}}$ inputs are not used, both the G1 and G2 symbols are loaded via the $\mathbf{G1_{2-0}}$ pins. The G1 symbols are then latched in on the falling edges of **DCLKIN** when **LDG2** is low and the G2 symbols are latched in on the falling edges of **DCLKIN** when **LDG2** is high.

OBIN

The STEL-2030C can accept the soft-decision input data in either **o**ffset **bin**ary or signed magnitude formats. When the **OBIN** signal is set high the format expected will be offset binary, and when it is set low it will be signed magnitude. The meanings of the 3-bit values for these two codes is shown in the table.

OBIN = 1	**OBIN** = 0	Value
111	111	Most confident +
110	110	(Data = 1)
101	101	
100	100	Least confident +
011	000	Least confident –
010	001	
001	010	(Data = 0)
000	011	Most confident –

When using the STEL-2030C with hard-decision data the symbols should be loaded into the $\mathbf{G1_2}$ and $\mathbf{G2_2}$ pins. The other symbol inputs should be set to a logic high level and **OBIN** should be set low.

LDG2

When this signal is high during a rising edge of **DCLKIN** the symbol loaded into the $\mathbf{G1_{2-0}}$ pins on the next falling edge of **DCLKIN** will be G2. This function is only active when **PARL** is set low (sequential input mode).

PARL

When this signal is high the input symbols are accepted in **par**al**l**el by the chip, using the $\mathbf{G1_{2-0}}$ pins for the G1 symbols and the $\mathbf{G2_{2-0}}$ pins for the G2 symbols. When it is set low the inputs are accepted sequentially, using the $\mathbf{G1_{2-0}}$ pins for both symbols. The sequential input is most suited for BPSK data and the parallel input is most suited for QPSK data.

OQPSK

When this signal is high the device is set up to operate with Offset QPSK (OQPSK) data. This is only valid when **PARL** is also set high.

DDIF

When this input is set high it causes the data out of the Viterbi **d**ecoder to be **dif**ferentially decoded. This function precedes the descrambler.

DSCRAM

When this input is set high it causes the data out of the Viterbi **d**ecoder to be de**scram**bled. The descrambling algorithm used is the CCITT or IESS V.35 algorithms according to the setting of **DSEL**, and descrambling follows differential decoding when this is enabled. When the **DSCRAM** signal is set low, this function will be inhibited.

DSEL

When this input is set low the CCITT compatible mode is selected for the V.35 descrambler in the decoder is set into and when it is set high the IESS compatible mode is selected.

PNCG1, PNCG2

The **PNCG1** and **PNCG2** signals are used to control the STEL-2030C when operating in punctured mode. In normal (Rate = $^1/_2$) operation these pins should be set low. In punctured mode the **PNCG1** signal must be set high to indicate that the G1 symbol is punctured and the **PNCG2** signal must be set high to indicate that the G2 symbol is punctured. A symbol will be punctured when the **PNCG1** or **PNCG2** signals are high during the falling edge of **DCLKIN** which latches the corresponding symbol in to the decoder. Zero value metrics will be substituted internally for the actual metrics corresponding to the signals present on the $\mathbf{G1_{2-0}}$ or $\mathbf{G2_{2-0}}$ pins at that time.

TBD

This signal selects the **T**race-**B**ack **D**epth used in the decoding process. When it is set low the traceback depth will be 70 states, and when it is set high the traceback depth will be 38 states. The longer traceback depth gives better performance, especially in the punctured modes; the shorter traceback depth gives a shorter latency.

SYNC

When the **SYNC** input is set high during the rising edge of **DCLKIN** the internal symbol synchronization will be changed. When auto node sync is not desired this pin should be set low. It should be connected to the **AUTO** output to use the auto node sync capability of the STEL-2030C. The state of this circuit will always be set to normal after a reset.

$COUNT_{7\text{-}0}$

This 8-bit input signal defines the period (number of bits) used in the node synchronization circuit. The 8-bit number N is used to set up a period of (256N+256) internally, where N is the value of **$COUNT_{7\text{-}0}$**. If the renormalization count exceeds the threshold value during a period of this number of bits then an out-of-sync condition is declared (i.e., the output pin **OOS** is switched to High and **AUTO** is toggled).

$THR_{7\text{-}0}$

This 8-bit input signal defines the threshold for node synchronization. The 8-bit number N is used to set up a threshold value of (8N+2) internally, where N is the value of **$THR_{7\text{-}0}$**. If the renormalization count is greater than this threshold value then an out-of-sync condition is declared (i.e., the output pin **OOS** is switched to High and **AUTO** is toggled).

CLKSEL

When **Cl**ock **Sel**ect is set low the STEL-2030C operates in its normal mode with **DCLKIN** running at twice the input symbol rate. When it is set high the device operates in the alternative mode with **DCLKIN** running at the same rate as the input symbols. This allows the device to be used in circuits having this clock requirement.

OUTPUT SIGNALS

EG1, EG2

The **EG1** and **EG2** signals are the two encoded sym-bols generated with the polynomials $G1 = 171_8$ and $G2 = 133_8$.

ECLKOUT

This signal is a replica of the **ECLKIN** signal. The output signals G1 and G2 change on the rising edges of this clock.

DATO

Decoded **dat**a **o**utput. This is the output of the Viterbi decoder. The output data bits are delayed by 163 clock cycles relative to the corresponding input symbols, **$G1_{2\text{-}0}$** and **$G2_{2\text{-}0}$** when operating in the short trace-back depth mode (**TBD** = 1), and 291 clock cycles when operating in the long trace-back depth mode (**TBD** = 0). This signal changes on the rising edges of **ODCLK**.

ODCLK

Output **d**ata **clock**. All outputs change on the rising edge of this clock. The falling edge of **ODCLK** can be used as a strobe for **DATO** output, which is guaranteed to be valid on this edge. Note that when **CLKSEL** = 0 and **PARL** = 1 the frequency of **ODCLK** is twice that of the data. If this clock is divided by 2 with a divider triggering on the falling edge of the clock the data will always be valid on the rising edge of the divider output.

OOS

This output pin serves as a flag for the **o**ut-**o**f-**s**ync condition. When it goes high it signifies that the renormalization count in the internal node sync circuit has exceeded the threshold value set by the **$THR_{7\text{-}0}$** signal and the out-of-sync condition is declared. It will remain high until this condition ceases to exist. i.e., the next time the threshold is not exceeded during a complete count period.

AUTO

This is the feedback signal from the internal node sync correction circuit. It will pulse high for one cycle of **DCLKIN** each time the renormalization count in the internal node sync circuit has exceeded the threshold value set by the **$THR_{7\text{-}0}$** signal and the out-of-sync condition is declared. It should be connected to the **SYNC** input when using the internal node sync facility.

BERR

The **B**it **Err**or output indicates that an error has been detected in either the G1 or G2 symbols corresponding to the current output bit. Note that when operating with punctured codes (Rates $^2/_3$ and $^3/_4$) the **BERR** output will pulse once for each symbol during which either **PNCG1** or **PNCG2** is set high. There will be a delay corresponding to the throughput delay of the decoder and encoder circuits between each instance of **PNCG2** or **PNCG2** being set high and the corresponding pulse on **BERR**.

G1ERR

The **G1 Err**or output indicates that an error has been detected in the G1 symbol corresponding to the current output bit. Note that when operating with punctured codes (Rates $^2/_3$ and $^3/_4$) the **G1ERR** output will pulse once for each symbol during which **PNCG1** is set high. There will be a delay corresponding to the throughput delay of the decoder and encoder circuits between each instance of **PNCG1** being set high and the corresponding pulse on **G1ERR**.

G2ERR

The **G2 Err**or output indicates that an error has been detected in the G2 symbol corresponding to the current output bit. Note that when operating with punctured codes (Rates $^2/_3$ and $^3/_4$) the **G2ERR** output will pulse once for each symbol during which **PNCG2** is set high. There will be a delay corresponding to the throughput delay of the decoder and encoder circuits between each instance of **PNCG2** being set high and the corresponding pulse on **G2ERR**.

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

***Warning:* Stresses greater than those shown below may cause permanent damage to the device. Exposure of the device to these conditions for extended periods may also affect device reliability.**

Symbol	Parameter	Range	Units
T_s	Storage Temperature	–40 to +125	°C (Plastic package)
		–55 to +125	°C (Ceramic package)
T_a	Operating Temperature	–40 to +85	°C (Plastic package)
		–55 to +125	°C (Ceramic package)
V_{DDmax}	Max. voltage between V_{DD} and V_{SS}	+7 to –0.7	volts
$V_{I/O(max)}$	Max. voltage on any input or output pin	V_{DD} + 0.3	volts
$V_{I/O(min)}$	Min. voltage on any input or output pin	V_{SS} – 0.3	volts

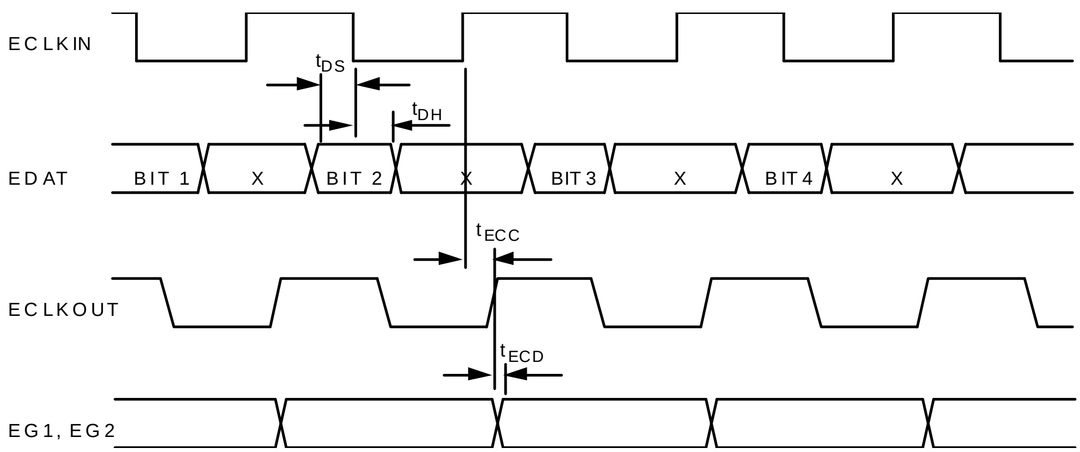
RECOMMENDED OPERATING CONDITIONS

Symbol		Parameter	Range Units
V_{DD}	Supply Voltage	+5 ± 5%	volts
T_a	Operating Temperature (Ambient)	0 to +70	°C (Plastic package)
		–55 to +125	°C (Ceramic package)

D.C. CHARACTERISTICS (Operating Conditions: V_{DD} = 5.0 ± 5% volts, T_a = 0° to 70° C)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_{DD(Q)}$	Supply Current, Quiescent			1.0	mA	Static, no clock
I_{DD}	Supply Current, Operational		2		mA / Mbps	**CLKSEL** = 0, **PARL** = 0
I_{DD}	Supply Current, Operational		8		mA / Mbps	All other modes
$V_{IH(min)}$	Min. High Level Input Voltage	2.0			volts	Guaranteed Logic '1'
$V_{IL(max)}$	Max. Low Level Input Voltage			0.8	volts	Guaranteed Logic '0'
$V_{OH(min)}$	Min. High Level Output Voltage	2.4			volts	I_O = –4.0 mA
$V_{OL(max)}$	Max. Low Level Output Voltage			0.4	volts	I_O = +4.0 mA
$I_{IH(max)}$	Max. High Level Input Current			10	µA	V_{IN} = +5.0 volts
$I_{IL(max)}$	Max. Low Level Input Current			–10	µA	V_{IN} = 0 volts

ENCODER TIMING



ENCODER A.C. CHARACTERISTICS (Operating Conditions: V_{DD} = 5.0 ± 5% volts, T_a = 0° to 70° C)

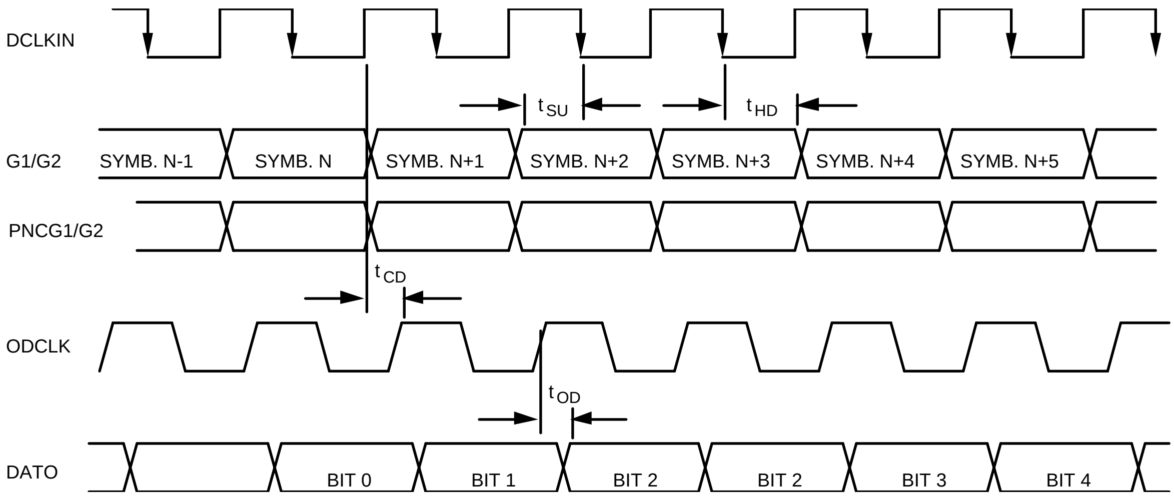
Symbol	Parameter	Min.	Max.	Units	Conditions
t_{DS}	**EDAT** to **ECLKIN** setup	10		nsec.	
t_{DH}	**EDAT** to **ECLKIN** hold	5		nsec.	
t_{ECC}	**ECLKIN** to **ECLKOUT** stable delay		30	nsec.	
t_{ECD}	**ECLKOUT** to **G1 G2** stable delay		5	nsec.	
f_{ECLK}	**ECLKIN** frequency		17	MHz	

DECODER A.C. CHARACTERISTICS (Operating Conditions: V_{DD} = 5.0 ±5% volts, T_a = 0° to 70° C)

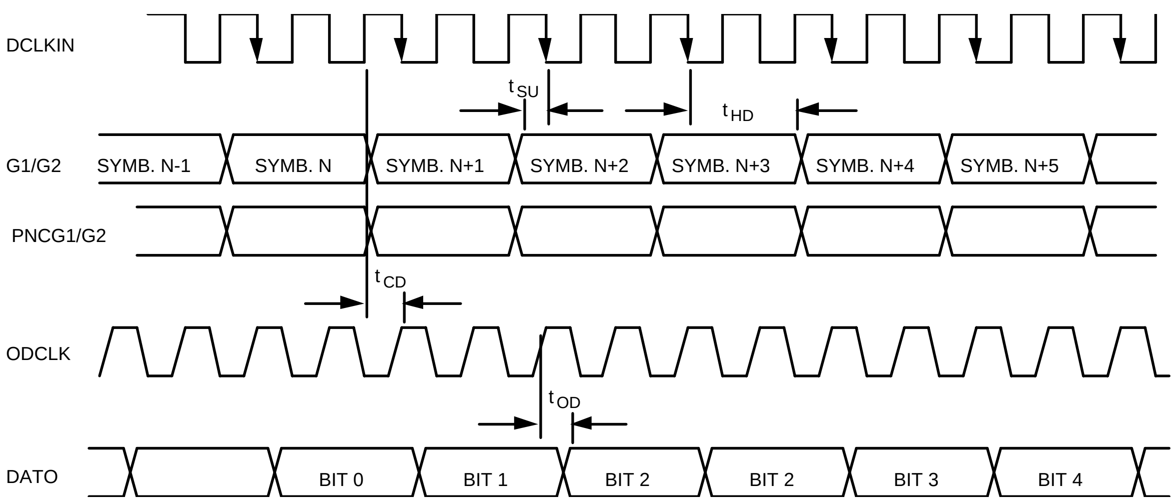
Symbol	Parameter	Min.	Max.	Units	Conditions
f_{DAT}	Data speed		17	Mbps	
t_{SU}	**G1**, **G2**, **PNCG1** or **PCNG2** to **DCLKIN** Setup	10		nsecs.	
t_{HD}	**G1**, **G2**, **PNCG1** or **PCNG2** to **DCLKIN** Hold	5		nsecs.	
t_{CD}	**DCLKIN** to **ODCLK** stable delay		20	nsecs.	
t_{OD}	**ODCLK** to any other output stable delay		12	nsecs.	

DECODER TIMING (a) PARALLEL INPUT MODE (PARL = 1)

1. CLKSEL = 1



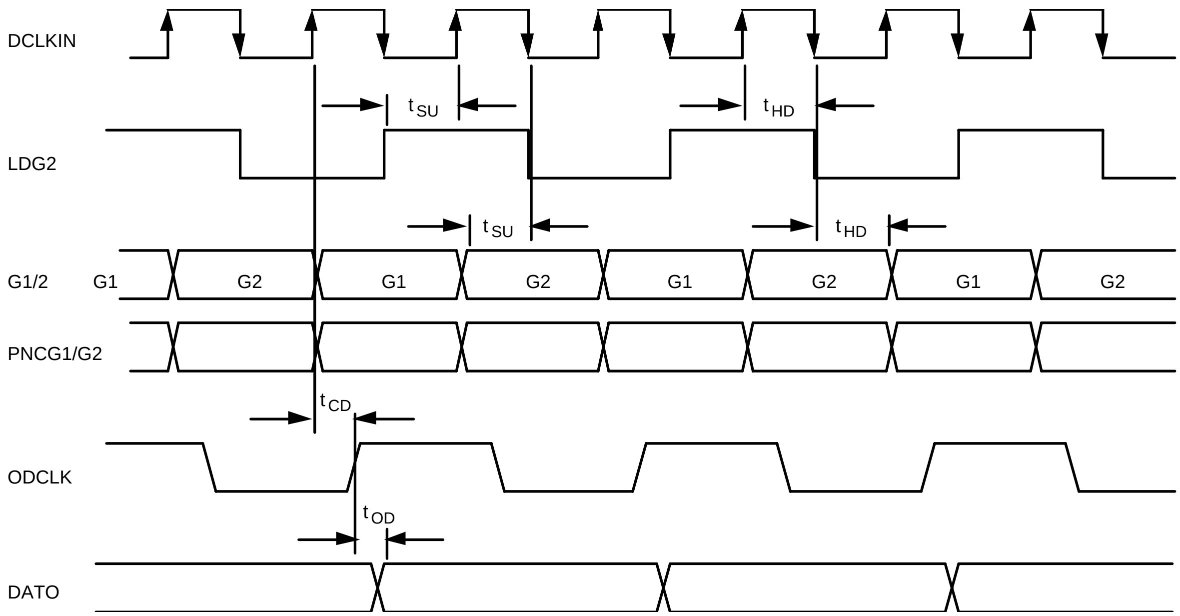
2. CLKSEL = 0



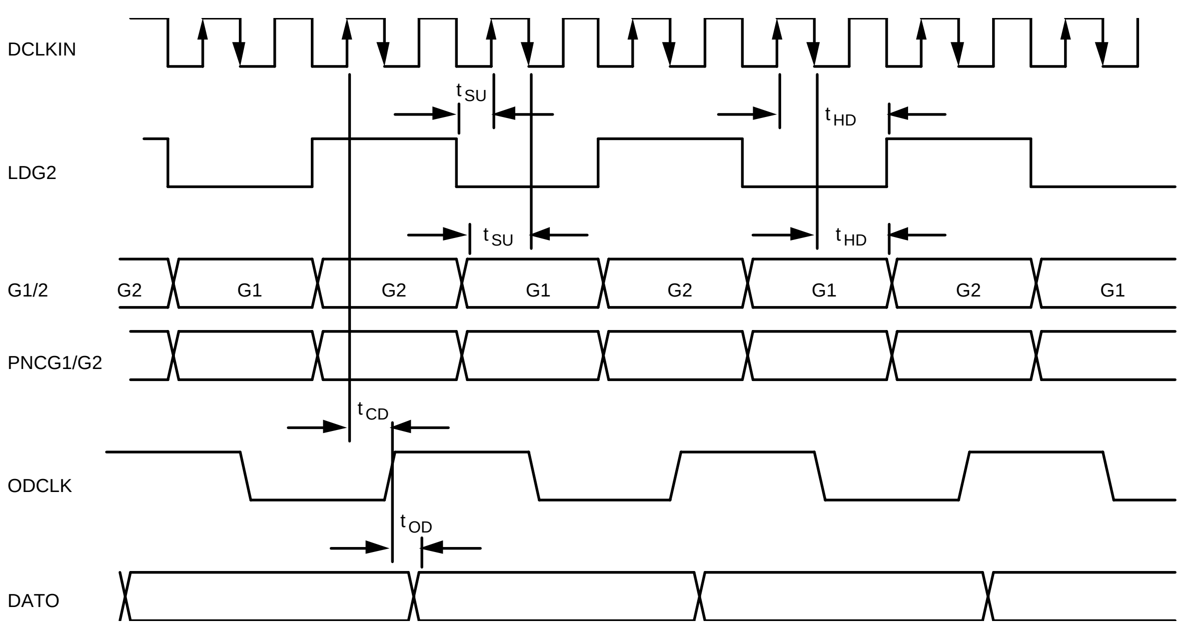
Notes:
1. N = 163 when **TBD** = 1, N = 291 when **TBD** = 0
2. When **CLKSEL** = 1 an internal double speed clock is generated whose rising edges are generated on the edges of **DCLKIN**.

DECODER TIMING (b) SEQUENTIAL INPUT MODE (PARL = 0)

1. CLKSEL = 1



2. CLKSEL = 0



Note: When **CLKSEL** = 1 an internal double speed clock is generated whose rising edges are generated on the edges of **DCLKIN**.

DECODER A.C. CHARACTERISTICS (Operating Conditions: V_{DD} = 5.0 ±5% volts, T_a = 0° to 70° C)

Symbol	Parameter	Min.	Max.	Units	Conditions
f_{DAT}	Data speed		17	Mbps	
t_{SU}	**G1**, **G2**, **PNCG1** or **PCNG2** to **DCLKIN** Setup	10		nsecs.	
t_{HD}	**G1**, **G2**, **PNCG1** or **PCNG2** to **DCLKIN** Hold	5		nsecs.	
t_{CD}	**DCLKIN** to **ODCLK** stable delay		20	nsecs.	
t_{OD}	**ODCLK** to any other output stable delay		12	nsecs.	

NODE SYNCHRONIZATION

In a communication system using Viterbi decoding the decoder will only operate correctly when the symbols G1 and G2 are loaded into the decoder in the correct order. Identifying which symbol is which is referred to as node synchronization. The STEL-2030C contains a circuit designed to carry out the node synchronization function automatically. It uses the internally generated metrics of the received sequence to do this. These parameters are constantly changing and are periodically renormalized to keep them within bounds. If renormalization is required too frequently it is a good indication that the system is not converging, and the most likely reason is lack of node synchronization. The renormalization rate at which the system will decide to change the node sync is determined by the threshold parameter. This is an 8-bit number which is set by the **THR$_{7-0}$** inputs. When the renormalization count exceeds this value, the **OOS** output will go high and the **AUTO** output will pulse high for one clock cycle. The counter is reset after a number of bits determined by the number set by the **COUNT$_{7-0}$** inputs, so that the threshold must be exceeded somewhere in that period for resynchronization to take place. To use the internal node sync the **AUTO** output must be connected to the **SYNC** input. The synchronization sequence depends on the setting of the **PARL** input. When **PARL** is set low it is assumed that the data was modulated using BPSK, and when it is set high it is assumed that the data was modulated using QPSK, the appropriate synchronization sequences will be invoked, as shown in the table:

		Symbol entered into decoder during symbol period N	
PARL	Sync State	**G1$_{2-0}$**	**G2$_{2-0}$**
0	0	$G1_N$	$G2_N$
0	1	$G2_{N-1}$	$G1_N$
1	0	$G1_N$	$G2_N$
1	1	$\overline{G2_N}$	$G1_N$

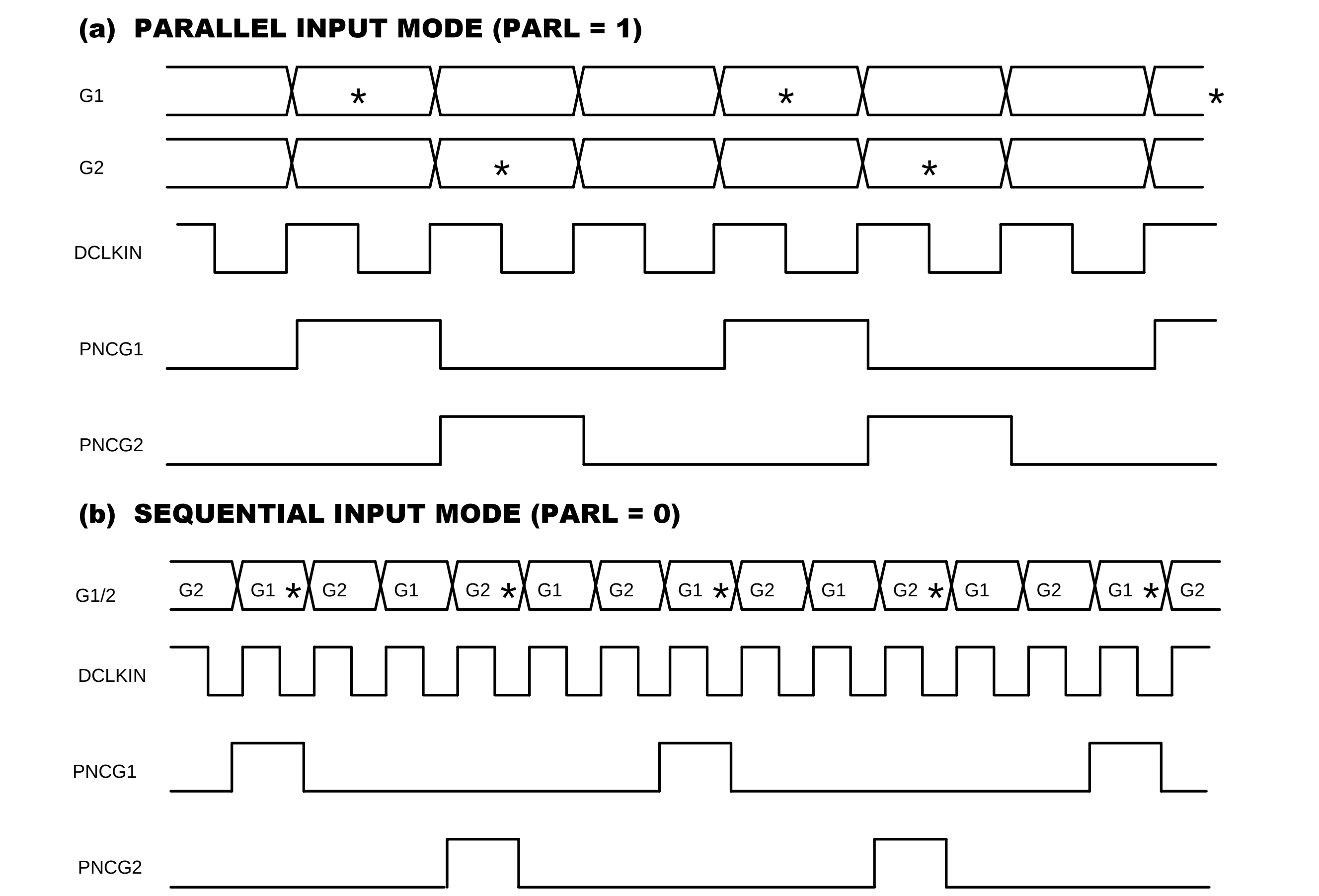
Sync state 0 is the state into which the device will be set after a reset sequence. Note that whenever the sync state is changed there will be a delay of 163 or 291 bit periods before valid data starts appearing at **DOUT**, according to the state of the **TBD** input.

The most suitable threshold setting will depend on both the value of E_b/N_0 and the signal level at the G1 and G2 inputs. For full scale inputs, i.e., the peak signal values almost saturate the digital inputs, a suitable starting value for the threshold will be 10%. e.g. if the number of bits over which the measure is made is set to 256 (**COUNT$_{7-0}$** = 0) the threshold should be set to 26 (**THR$_{7-0}$** = 3). More reliable results will be obtained by counting over a longer period to improve the averaging process, but this increases the time taken to make a decision and hence to acquire node sync. Thus starting with a low count period and then increasing it (and adjusting the threshold accordingly to maintain a value of 10%) will result in a faster acquisition of correct node sync followed by a better chance of recorrecting if an error was made.

PUNCTURED CODE OPERATION

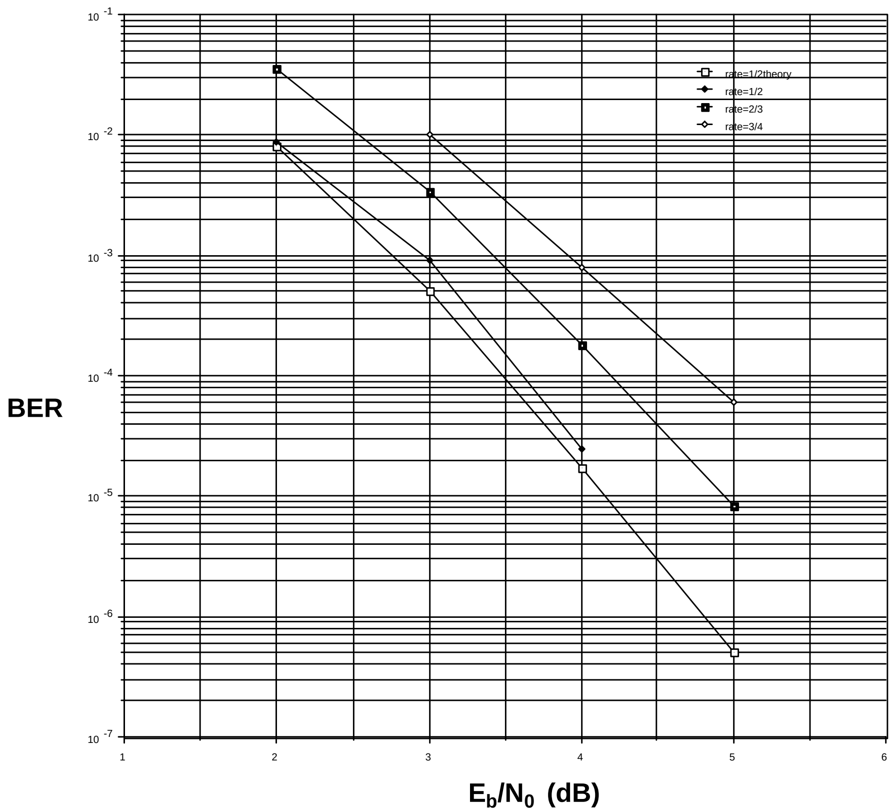
In punctured codes some of the symbols generated by the convolutional encoder are deleted, or punctured, from the transmitted sequence. For example, in an unpunctured Rate $^1/_2$ sequence, four bits would be transmitted for every two data bits. If every fourth bit was punctured from the sequence then only three bits would be transmitted for every two data bits. This would result in a Rate $^2/_3$ code. The STEL-2030C decoder is designed to operate in punctured mode as well as normal, Rate $^1/_2$, mode. This is easily accomplished by means of the **PNCG1** and **PNCG2** signals, which delete the symbol which would normally have been loaded into the device at the time when either of these signals is set high. The punctured symbols are replaced by zero metric values. Zero weight is given to these values in the computations relative to the other symbols. The coding gain is significantly less than that for unpunctured operation, as shown in the BER plot, but this is the trade-off for the reduced bandwidth required to transmit the symbols. The puncturing sequences for the various $^{(N-1)}/_N$ rates of punctured operation are shown in the table. The sequence shown in boldface is the basic sequence, which is then repeated. The use of the **PNCG1** and **PNCG2** signals is shown below for Rate $^3/_4$. The sequence is G1 G2 P G2 G1 P. The punctured symbols are marked with asterisks. Rates higher than $^3/_4$ are not recommended with the STEL-2030C.

Rate	Symbol sequence
$^2/_3$	**G1 G2 G1 P** G1 G2 G1 P G1 G2 G1 P G1 G2 G1 P G1 G2
$^3/_4$	**G1 G2 P G2 G1 P** G1 G2 P G2 G1 P G1 G2 P G2 G1 G2



Note: Timing shown for case where **CLKSEL** = 1. **DCLKIN** runs at double the speed when **CLKSEL** = 0.

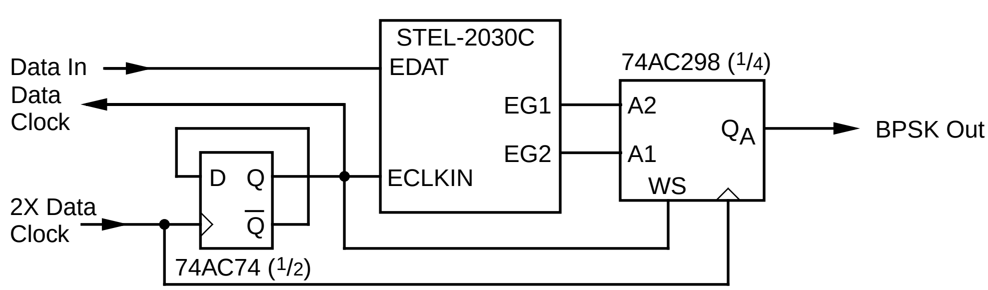
BER PERFORMANCE WITH RATE 1/2 AND PUNCTURED CODES



APPLICATIONS INFORMATION

BPSK OPERATION OF ENCODER

The STEL-2030C encoder generates output symbols as parallel pairs, suitable for QPSK modulation. For BPSK modulation it is normally necessary to serialize the symbol pairs using a clock at twice the data rate. A suitable circuit is shown below in which the input clock is divided by two to produce the data clock itself. The encoder produces parallel symbol pairs and the multiplexer serializes them for BPSK modulation.

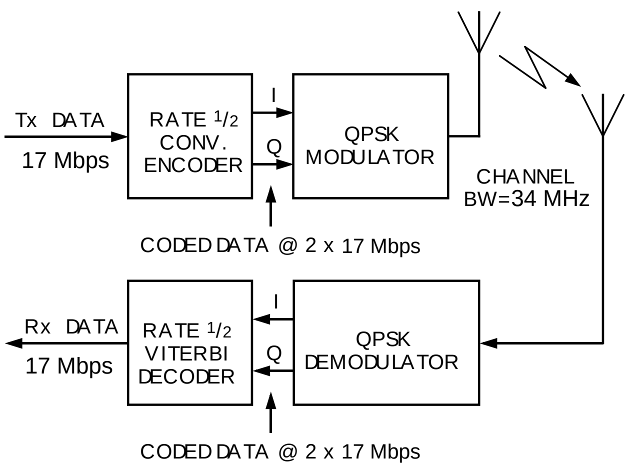


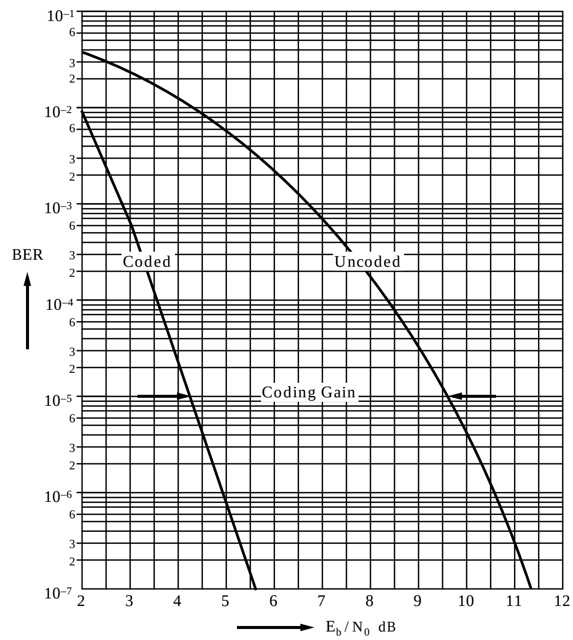
APPLICATION INFORMATION

The STEL-2030C can be used in a variety of different environments. One example of a system using the convolutional coder and Viterbi decoder is illustrated here. It cannot be used as a common encoder or decoder in multi-channel applications because of the memory incorporated on the chip which is dedicated to a single channel.

The system modulates a data stream of rate 17 Mbps using binary PSK (BPSK) or quaternary PSK (QPSK). To be able to use convolutional coding/decoding, the system must have available the additional bandwidth needed to transmit symbols at twice the data rate (for rate $^1/_2$ encoding) or make use of two parallel channels (QPSK) to transmit two streams of symbols at the data rate. The performance improvement that can be expected is shown in the graph below.

The convolutional encoder is functionally independent from the decoder. A single data bit is clocked into the 7 bit shift register on the rising edge of **ECLKIN**. The decoder portion of the STEL-2030C is designed to accept symbols synchronously. **DCLKIN** is supplied by the user to clock in the symbols. The maximum data rate is 17 Mbps, using a clock frequency of 34 MHz. This corresponds to 34 MSymbols per sec at Rate $^1/_2$.





QPSK Communication System Using Convolutional Encoding and Viterbi Decoding. Rate = $^1/_2$

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