

BUK962R8-60E

N-channel TrenchMOS logic level FET

13 July 2012

Product data sheet

1. Product profile

1.1 General description

Logic level N-channel MOSFET in a SOT404 package using TrenchMOS technology. This product has been designed and qualified to AEC Q101 standard for use in high performance automotive applications.

1.2 Features and benefits

- AEC Q101 compliant
- Repetitive avalanche rated
- Suitable for thermally demanding environments due to 175 °C rating
- True logic level gate with V_{GS(th)} rating of greater than 0.5V at 175 °C

1.3 Applications

- 12 V Automotive systems
- Motors, lamps and solenoid control
- Start-Stop micro-hybrid applications
- Transmission control
- Ultra high performance power switching

1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V _{DS}	drain-source voltage	T _j ≥ 25 °C; T _j ≤ 175 °C		-	-	60	V
I _D	drain current	V _{GS} = 5 V; T _{mb} = 25 °C; Fig. 1	[1]	-	-	120	A
P _{tot}	total power dissipation	T _{mb} = 25 °C; Fig. 2		-	-	324	W
Static characteristics							
R _{DS(on)}	drain-source on-state resistance	V _{GS} = 5 V; I _D = 25 A; T _j = 25 °C; Fig. 11		-	2.29	2.8	mΩ
Dynamic characteristics							
Q _{GD}	gate-drain charge	V _{GS} = 5 V; I _D = 25 A; V _{DS} = 48 V; Fig. 13 ; Fig. 14		-	28.6	-	nC

[1] Continuous current is limited by package.



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2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 D2PAK (SOT404)	 mbb076
2	D	drain		
3	S	source		
mb	D	mounting base; connected to drain		

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK962R8-60E	D2PAK	plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)	SOT404

4. Limiting values

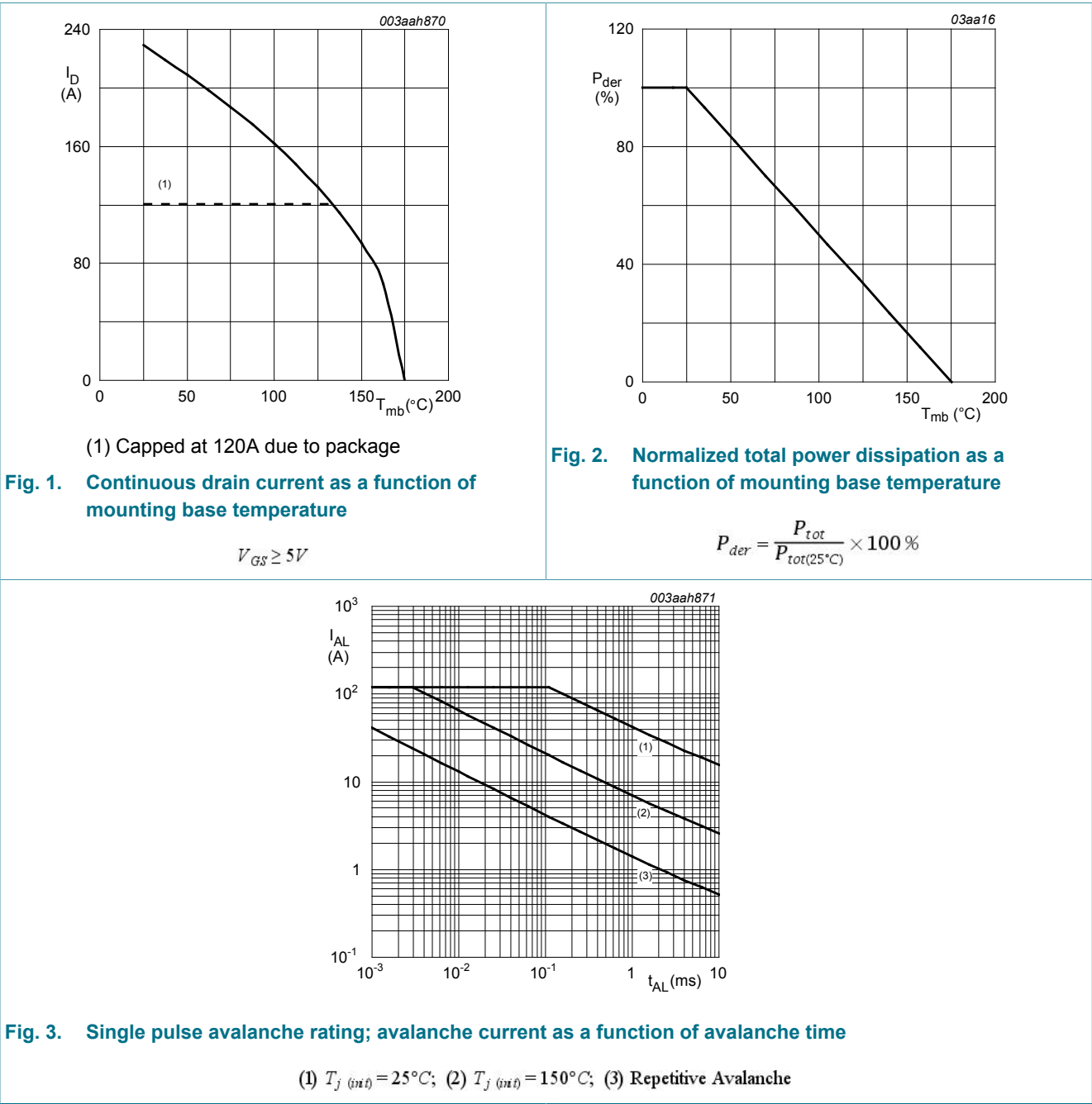
Table 4. Limiting values

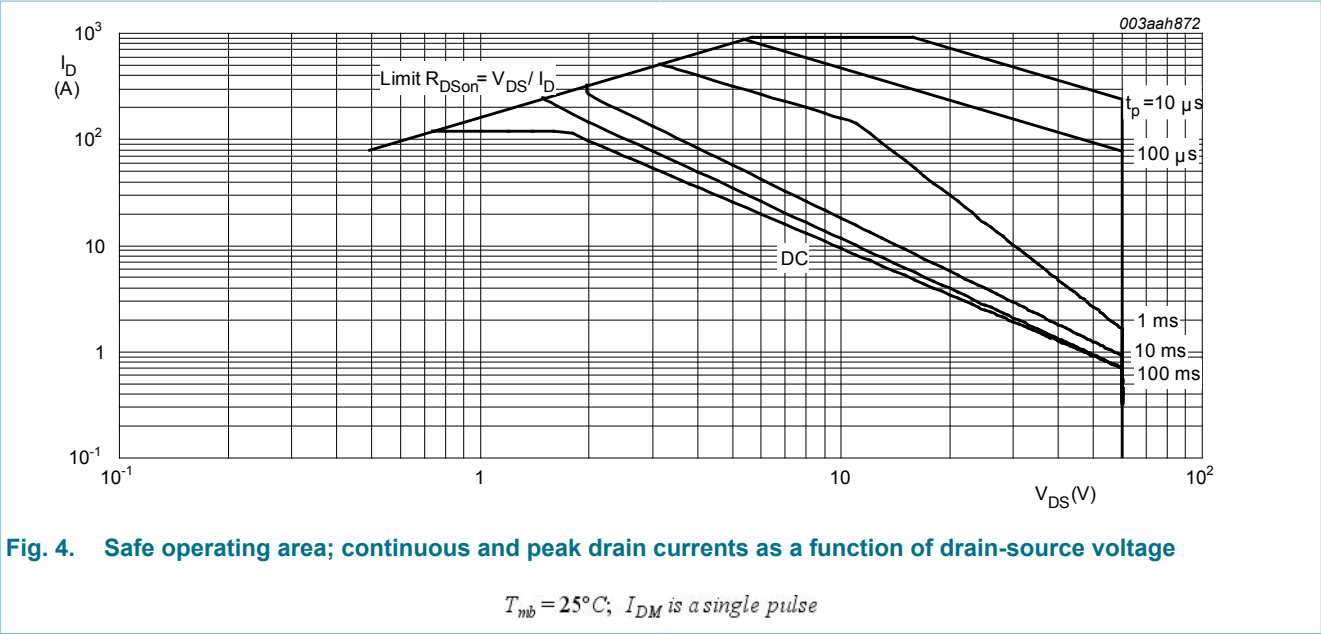
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ }^{\circ}\text{C}$; $T_j \leq 175\text{ }^{\circ}\text{C}$		-	60	V
V_{DGR}	drain-gate voltage	$R_{GS} = 20\text{ k}\Omega$		-	60	V
V_{GS}	gate-source voltage	$T_j = 25\text{ }^{\circ}\text{C}$; lifetime = 100 hours		-15	15	V
		$T_j = 25\text{ }^{\circ}\text{C}$		-10	10	V
I_D	drain current	$T_{mb} = 25\text{ }^{\circ}\text{C}$; $V_{GS} = 5\text{ V}$; Fig. 1	[1]	-	120	A
		$T_{mb} = 100\text{ }^{\circ}\text{C}$; $V_{GS} = 5\text{ V}$; Fig. 1	[1]	-	120	A
I_{DM}	peak drain current	$T_{mb} = 25\text{ }^{\circ}\text{C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$; Fig. 4		-	917	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ }^{\circ}\text{C}$; Fig. 2		-	324	W
T_{stg}	storage temperature			-55	175	$^{\circ}\text{C}$
T_j	junction temperature			-55	175	$^{\circ}\text{C}$
Source-drain diode						
I_S	source current	$T_{mb} = 25\text{ }^{\circ}\text{C}$	[1]	-	120	A
I_{SM}	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ }^{\circ}\text{C}$		-	917	A

Symbol	Parameter	Conditions		Min	Max	Unit
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 120\text{ A}$; $V_{sup} \leq 60\text{ V}$; $R_{GS} = 50\text{ }\Omega$; $V_{GS} = 5\text{ V}$; $T_{j(init)} = 25\text{ }^\circ\text{C}$; unclamped; Fig. 3	[2] [3]	-	519	mJ

- [1] Continuous current is limited by package.
- [2] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.
- [3] Refer to application note AN10273 for further information.

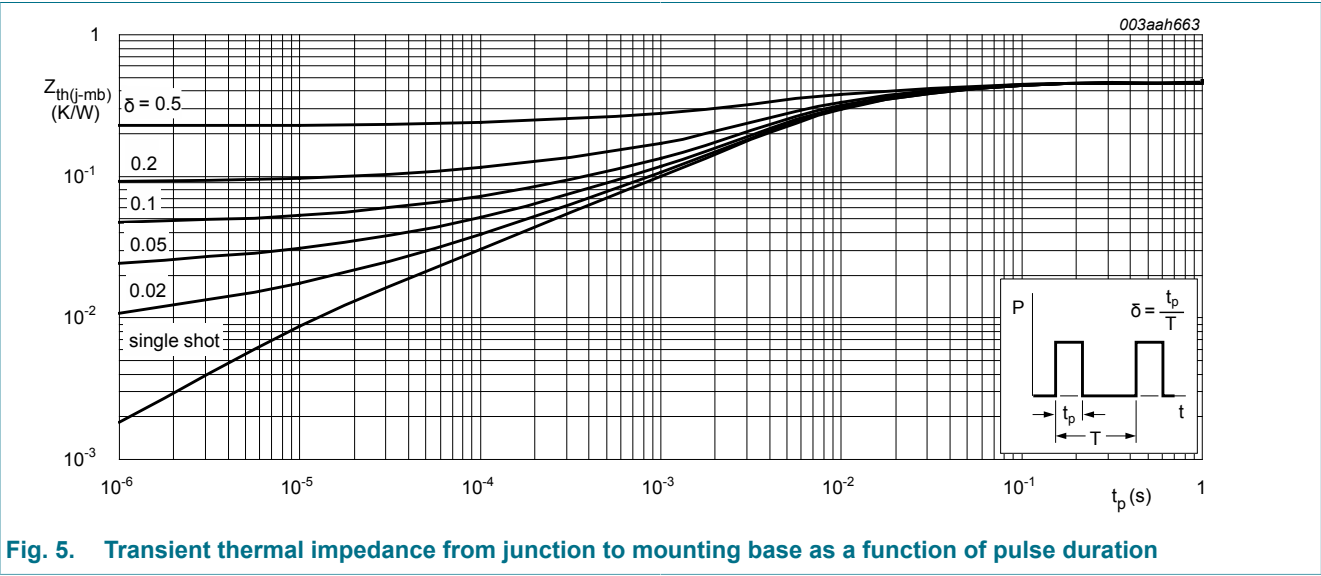




5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5	-	-	0.46	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	minimum footprint ; mounted on a printed-circuit board	-	50	-	K/W



6. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
V _{(BR)DSS}	drain-source breakdown voltage	I _D = 250 μA; V _{GS} = 0 V; T _j = 25 °C		60	-	-	V
		I _D = 250 μA; V _{GS} = 0 V; T _j = -55 °C		54	-	-	V
V _{GS(th)}	gate-source threshold voltage	I _D = 1 mA; V _{DS} = V _{GS} ; T _j = 25 °C; Fig. 9 ; Fig. 10		1.4	1.7	2.1	V
		I _D = 1 mA; V _{DS} = V _{GS} ; T _j = -55 °C; Fig. 9		-	-	2.45	V
		I _D = 1 mA; V _{DS} = V _{GS} ; T _j = 175 °C; Fig. 9		0.5	-	-	V
I _{DSS}	drain leakage current	V _{DS} = 60 V; V _{GS} = 0 V; T _j = 25 °C		-	0.08	1	μA
		V _{DS} = 60 V; V _{GS} = 0 V; T _j = 175 °C		-	-	500	μA
I _{GSS}	gate leakage current	V _{GS} = 10 V; V _{DS} = 0 V; T _j = 25 °C		-	2	100	nA
		V _{GS} = -10 V; V _{DS} = 0 V; T _j = 25 °C		-	2	100	nA
R _{DSon}	drain-source on-state resistance	V _{GS} = 5 V; I _D = 25 A; T _j = 25 °C; Fig. 11		-	2.29	2.8	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _j = 25 °C; Fig. 11		-	2.08	2.5	mΩ
		V _{GS} = 5 V; I _D = 25 A; T _j = 175 °C; Fig. 12 ; Fig. 11		-	-	6.2	mΩ
Dynamic characteristics							
Q _{G(tot)}	total gate charge	I _D = 25 A; V _{DS} = 48 V; V _{GS} = 5 V; Fig. 13 ; Fig. 14		-	96	-	nC
Q _{GS}	gate-source charge			-	27.8	-	nC
Q _{GD}	gate-drain charge			-	28.6	-	nC
C _{iss}	input capacitance	V _{GS} = 0 V; V _{DS} = 25 V; f = 1 MHz; T _j = 25 °C; Fig. 15		-	11701	15600	pF
C _{oss}	output capacitance			-	925	1110	pF
C _{rss}	reverse transfer capacitance			-	444	610	pF
t _{d(on)}	turn-on delay time	V _{DS} = 45 V; R _L = 1.8 Ω; V _{GS} = 5 V; R _{G(ext)} = 5 Ω		-	53	-	ns
t _r	rise time			-	88	-	ns
t _{d(off)}	turn-off delay time			-	115	-	ns
t _f	fall time			-	81	-	ns
L _D	internal drain inductance	from upper edge of drain mounting base to center of die		-	2.5	-	nH
L _S	internal source inductance	from source lead to source bonding pad		-	7.5	-	nH

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 25\text{ A}$; $V_{GS} = 0\text{ V}$; $T_j = 25\text{ }^{\circ}\text{C}$; Fig. 16	-	0.77	1.2	V
t_{rr}	reverse recovery time	$I_S = 20\text{ A}$; $di_S/dt = -100\text{ A}/\mu\text{s}$; $V_{GS} = 0\text{ V}$;	-	45	-	ns
Q_r	recovered charge	$V_{DS} = 25\text{ V}$	-	74	-	nC

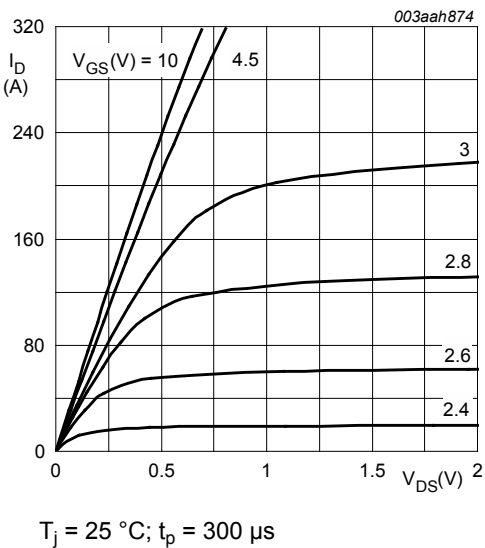


Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values

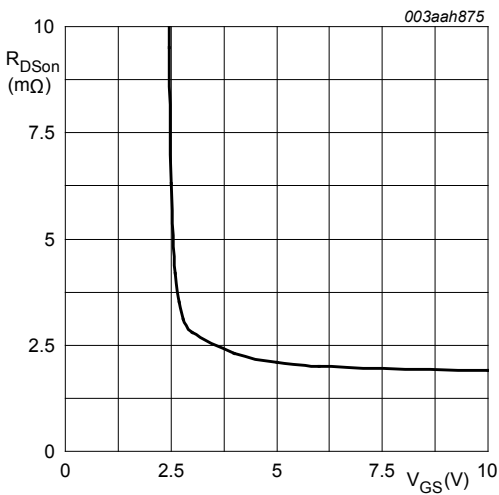


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

$T_j = 25^{\circ}\text{C}$; $I_D = 25\text{ A}$

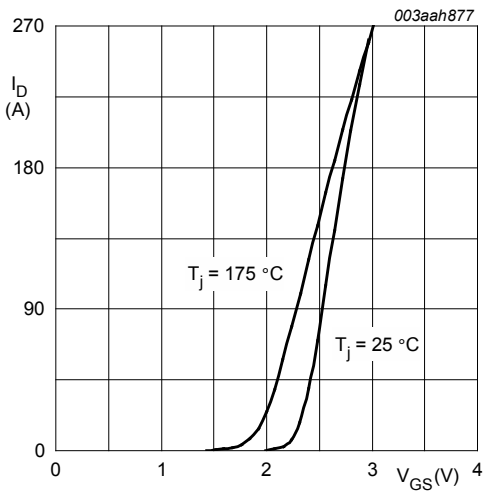


Fig. 8. Transfer characteristics; drain current as a function of gate-source voltage; typical values

$V_{DS} = 10\text{ V}$

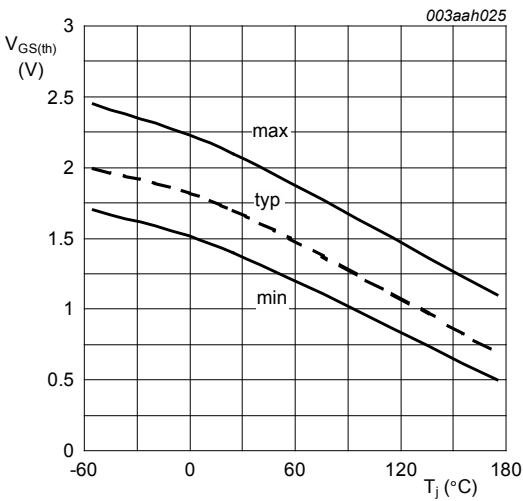


Fig. 9. Gate-source threshold voltage as a function of junction temperature

$I_D = 1\text{ mA}$; $V_{DS} = V_{GS}$

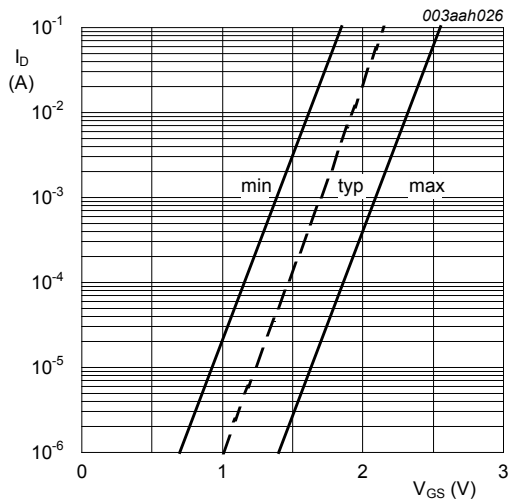


Fig. 10. Sub-threshold drain current as a function of gate-source voltage

$T_j = 25^{\circ}\text{C}; V_{DS} = 5\text{V}$

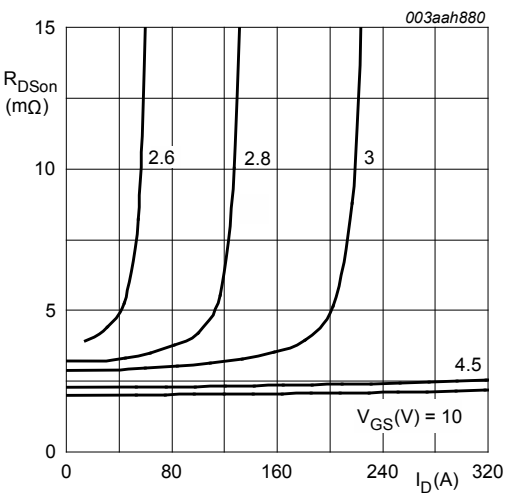


Fig. 11. Drain-source on-state resistance as a function of drain current; typical values

$T_j = 25^{\circ}\text{C}; t_p = 300\text{ }\mu\text{s}$

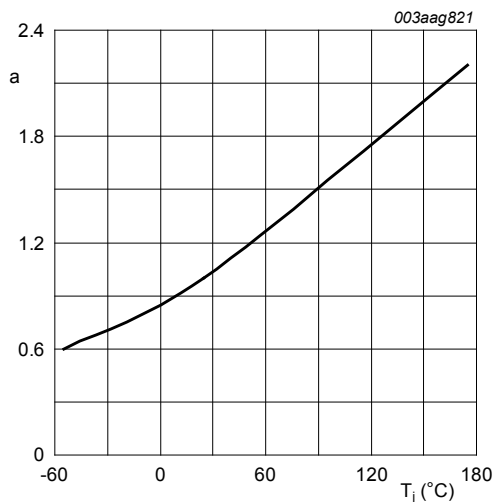


Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DSon}}{R_{DSon(25^{\circ}\text{C})}}$$

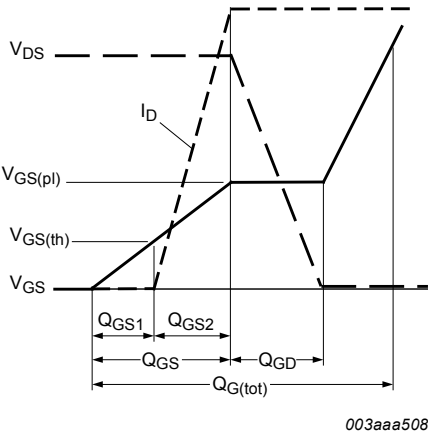


Fig. 13. Gate charge waveform definitions

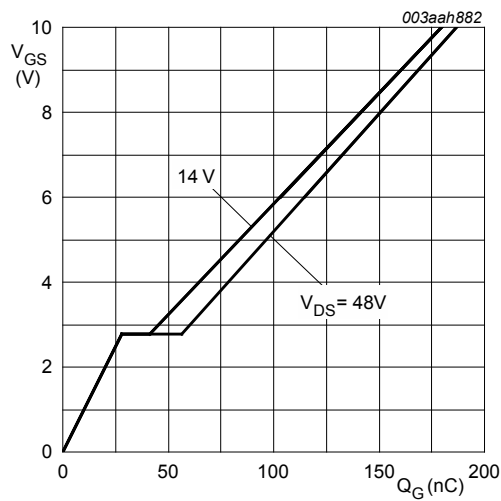


Fig. 14. Gate-source voltage as a function of gate charge; typical values

$T_j = 25^{\circ}C; I_D = 25A$

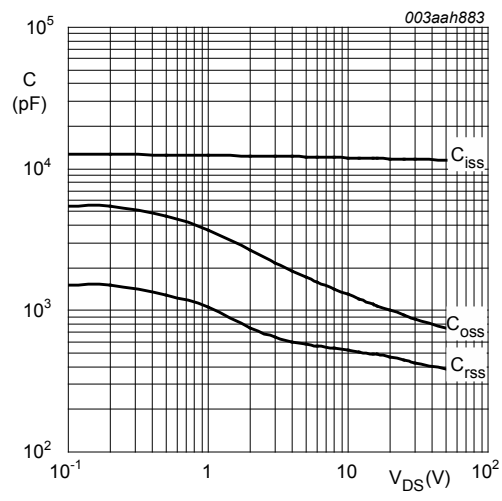


Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

$V_{GS} = 0V; f = 1MHz$

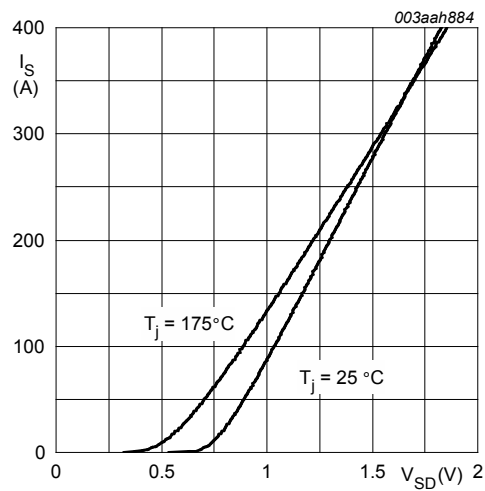


Fig. 16. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values

$V_{GS} = 0V$

7. Package outline

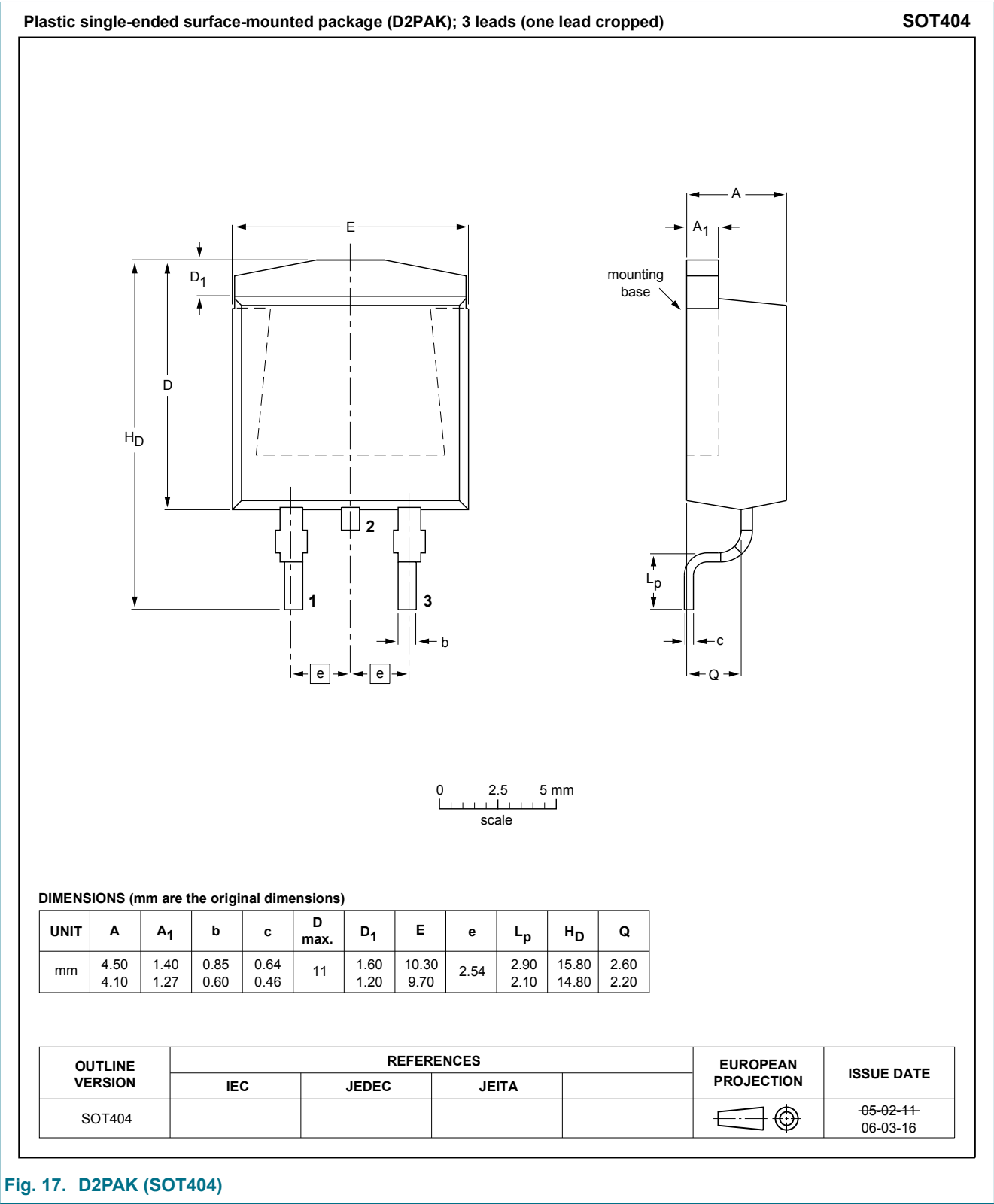


Fig. 17. D2PAK (SOT404)

8. Legal information

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9. Contents

1 Product profile 1

1.1 General description 1

1.2 Features and benefits1

1.3 Applications 1

1.4 Quick reference data 1

2 Pinning information2

3 Ordering information2

4 Limiting values2

5 Thermal characteristics4

6 Characteristics5

7 Package outline 9

8 Legal information10

8.1 Data sheet status 10

8.2 Definitions10

8.3 Disclaimers10

8.4 Trademarks 11

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