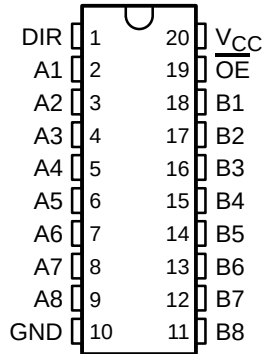


# SN54HC645, SN74HC645 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

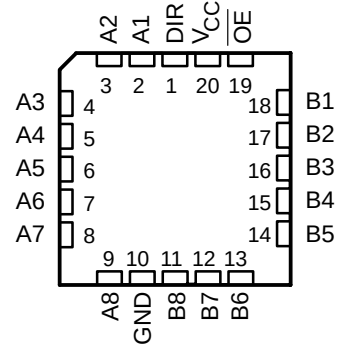
SCLS304B – JANUARY 1996 – REVISED DECEMBER 2002

- Wide Operating Voltage Range of 2 V to 6 V
- High-Current 3-State Outputs Can Drive Up To 15 LSTTL Loads
- Low Power Consumption, 80- $\mu$ A Max  $I_{CC}$
- Typical  $t_{pd} = 12$  ns
- $\pm 6$ -mA Output Drive at 5 V
- Low Input Current of 1  $\mu$ A Max
- True Logic

SN54HC645 . . . J OR W PACKAGE  
SN74HC645 . . . DW, N, OR NS PACKAGE  
(TOP VIEW)



SN54HC645 . . . FK PACKAGE  
(TOP VIEW)



## description/ordering information

These octal bus transceivers are designed for asynchronous two-way communication between data buses. These devices transmit data from the A bus to the B bus or from the B bus to the A bus, depending upon the level at the direction-control (DIR) input. The output-enable ( $\overline{OE}$ ) input can be used to disable the device so the buses are effectively isolated.

## ORDERING INFORMATION

| $T_A$          | PACKAGE <sup>†</sup> |               | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|----------------------|---------------|-----------------------|------------------|
| –40°C to 85°C  | PDIP – N             | Tube          | SN74HC645N            | SN74HC645N       |
|                | SOIC – DW            | Tube          | SN74HC645DW           |                  |
|                |                      | Tape and reel | SN74HC645DWR          | HC645            |
|                | SOP – NS             | Tape and reel | SN74HC645NSR          | HC645            |
| –55°C to 125°C | CDIP – J             | Tube          | SNJ54HC645J           | SNJ54HC645J      |
|                | CFP – W              | Tube          | SNJ54HC645W           | SNJ54HC645W      |
|                | LCCC – FK            | Tube          | SNJ54HC645FK          | SNJ54HC645FK     |

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

## FUNCTION TABLE

| INPUTS          |     | OPERATION       |
|-----------------|-----|-----------------|
| $\overline{OE}$ | DIR |                 |
| L               | L   | B data to A bus |
| L               | H   | A data to B bus |
| H               | X   | Isolation       |



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2002, Texas Instruments Incorporated  
On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

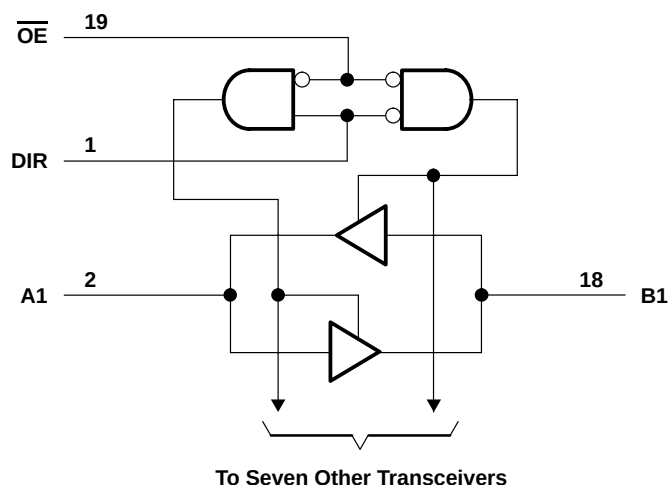
# SN54HC645, SN74HC645

## OCTAL BUS TRANSCEIVERS

### WITH 3-STATE OUTPUTS

SCLS304B – JANUARY 1996 – REVISED DECEMBER 2002

#### logic diagram (positive logic)



#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

|                                                                             |                |
|-----------------------------------------------------------------------------|----------------|
| Supply voltage range, $V_{CC}$                                              | –0.5 V to 7 V  |
| Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ ) (see Note 1)  | $\pm 20$ mA    |
| Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) (see Note 1) | $\pm 20$ mA    |
| Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )                  | $\pm 35$ mA    |
| Continuous current through $V_{CC}$ or GND                                  | $\pm 70$ mA    |
| Package thermal impedance, $\theta_{JA}$ (see Note 2): DW package           | 58°C/W         |
| N package                                                                   | 69°C/W         |
| NS package                                                                  | 60°C/W         |
| Storage temperature range, $T_{stg}$                                        | –65°C to 150°C |

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JESD 51-7.

#### recommended operating conditions (see Note 3)

|                 |                                 |                         | SN54HC645 |                 |     | SN74HC645 |                 |     | UNIT |
|-----------------|---------------------------------|-------------------------|-----------|-----------------|-----|-----------|-----------------|-----|------|
|                 |                                 |                         | MIN       | NOM             | MAX | MIN       | NOM             | MAX |      |
| V <sub>CC</sub> | Supply voltage                  |                         | 2         | 5               | 6   | 2         | 5               | 6   | V    |
| V <sub>IH</sub> | High-level input voltage        | V <sub>CC</sub> = 2 V   | 1.5       |                 |     | 1.5       |                 |     | V    |
|                 |                                 | V <sub>CC</sub> = 4.5 V | 3.15      |                 |     | 3.15      |                 |     |      |
|                 |                                 | V <sub>CC</sub> = 6 V   | 4.2       |                 |     | 4.2       |                 |     |      |
| V <sub>IL</sub> | Low-level input voltage         | V <sub>CC</sub> = 2 V   | 0.5       |                 |     | 0.5       |                 |     | V    |
|                 |                                 | V <sub>CC</sub> = 4.5 V | 1.35      |                 |     | 1.35      |                 |     |      |
|                 |                                 | V <sub>CC</sub> = 6 V   | 1.8       |                 |     | 1.8       |                 |     |      |
| V <sub>I</sub>  | Input voltage                   |                         | 0         | V <sub>CC</sub> |     | 0         | V <sub>CC</sub> |     | V    |
| V <sub>O</sub>  | Output voltage                  |                         | 0         | V <sub>CC</sub> |     | 0         | V <sub>CC</sub> |     | V    |
| Δt/Δv           | Input transition rise/fall time | V <sub>CC</sub> = 2 V   | 1000      |                 |     | 1000      |                 |     | ns   |
|                 |                                 | V <sub>CC</sub> = 4.5 V | 500       |                 |     | 500       |                 |     |      |
|                 |                                 | V <sub>CC</sub> = 6 V   | 400       |                 |     | 400       |                 |     |      |
| T <sub>A</sub>  | Operating free-air temperature  |                         | −55       | 125             |     | −40       | 85              |     | °C   |



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

# SN54HC645, SN74HC645 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCLS304B – JANUARY 1996 – REVISED DECEMBER 2002

NOTE 3: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS            |                                | $V_{CC}$   | $T_A = 25^\circ\text{C}$ |            |           | SN54HC645 |            | SN74HC645 |            | UNIT          |
|-----------|----------------------------|--------------------------------|------------|--------------------------|------------|-----------|-----------|------------|-----------|------------|---------------|
|           |                            |                                |            | MIN                      | TYP        | MAX       | MIN       | MAX        | MIN       | MAX        |               |
| $V_{OH}$  | $V_I = V_{IH}$ or $V_{IL}$ | $I_{OH} = -20\ \mu\text{A}$    | 2 V        | 1.9                      | 1.998      |           | 1.9       |            | 1.9       |            | V             |
|           |                            |                                | 4.5 V      | 4.4                      | 4.499      |           | 4.4       |            | 4.4       |            |               |
|           |                            |                                | 6 V        | 5.9                      | 5.999      |           | 5.9       |            | 5.9       |            |               |
|           |                            | $I_{OH} = -6\ \text{mA}$       | 4.5 V      | 3.98                     | 4.3        |           | 3.7       |            | 3.84      |            |               |
|           |                            | $I_{OH} = -7.8\ \text{mA}$     | 6 V        | 5.48                     | 5.8        |           | 5.2       |            | 5.34      |            |               |
| $V_{OL}$  | $V_I = V_{IH}$ or $V_{IL}$ | $I_{OL} = 20\ \mu\text{A}$     | 2 V        |                          | 0.002      | 0.1       |           | 0.1        |           | 0.1        | V             |
|           |                            |                                | 4.5 V      |                          | 0.001      | 0.1       |           | 0.1        |           | 0.1        |               |
|           |                            |                                | 6 V        |                          | 0.001      | 0.1       |           | 0.1        |           | 0.1        |               |
|           |                            | $I_{OL} = 6\ \text{mA}$        | 4.5 V      |                          | 0.17       | 0.26      |           | 0.4        |           | 0.33       |               |
|           |                            | $I_{OL} = 7.8\ \text{mA}$      | 6 V        |                          | 0.15       | 0.26      |           | 0.4        |           | 0.33       |               |
| $I_I$     | DIR or $\overline{OE}$     | $V_I = V_{CC}$ or 0            | 6 V        |                          | $\pm 0.1$  | $\pm 100$ |           | $\pm 1000$ |           | $\pm 1000$ | nA            |
| $I_{OZ}$  | A or B                     | $V_O = V_{CC}$ or 0            | 6 V        |                          | $\pm 0.01$ | $\pm 0.5$ |           | $\pm 10$   |           | $\pm 5$    | $\mu\text{A}$ |
| $I_{CC}$  |                            | $V_I = V_{CC}$ or 0, $I_O = 0$ | 6 V        |                          |            | 8         |           | 160        |           | 80         | $\mu\text{A}$ |
| $C_i$     | DIR or $\overline{OE}$     |                                | 2 V to 6 V |                          | 3          | 10        |           | 10         |           | 10         | pF            |

## switching characteristics over recommended operating free-air temperature range, $C_L = 50\ \text{pF}$ (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT)    | TO (OUTPUT) | $V_{CC}$ | $T_A = 25^\circ\text{C}$ |     |     | SN54HC645 |     | SN74HC645 |     | UNIT |
|-----------|-----------------|-------------|----------|--------------------------|-----|-----|-----------|-----|-----------|-----|------|
|           |                 |             |          | MIN                      | TYP | MAX | MIN       | MAX | MIN       | MAX |      |
| $t_{pd}$  | A or B          | B or A      | 2 V      |                          | 40  | 105 |           | 160 |           | 130 | ns   |
|           |                 |             | 4.5 V    |                          | 15  | 21  |           | 32  |           | 26  |      |
|           |                 |             | 6 V      |                          | 12  | 18  |           | 27  |           | 22  |      |
| $t_{en}$  | $\overline{OE}$ | A or B      | 2 V      |                          | 125 | 230 |           | 340 |           | 290 | ns   |
|           |                 |             | 4.5 V    |                          | 23  | 46  |           | 68  |           | 58  |      |
|           |                 |             | 6 V      |                          | 20  | 39  |           | 58  |           | 49  |      |
| $t_{dis}$ | $\overline{OE}$ | A or B      | 2 V      |                          | 74  | 200 |           | 300 |           | 250 | ns   |
|           |                 |             | 4.5 V    |                          | 25  | 40  |           | 60  |           | 50  |      |
|           |                 |             | 6 V      |                          | 21  | 34  |           | 51  |           | 43  |      |
| $t_t$     |                 | A or B      | 2 V      |                          | 20  | 60  |           | 90  |           | 75  | ns   |
|           |                 |             | 4.5 V    |                          | 8   | 12  |           | 18  |           | 15  |      |
|           |                 |             | 6 V      |                          | 6   | 10  |           | 15  |           | 13  |      |



# SN54HC645, SN74HC645

## OCTAL BUS TRANSCEIVERS

### WITH 3-STATE OUTPUTS

SCLS304B – JANUARY 1996 – REVISED DECEMBER 2002

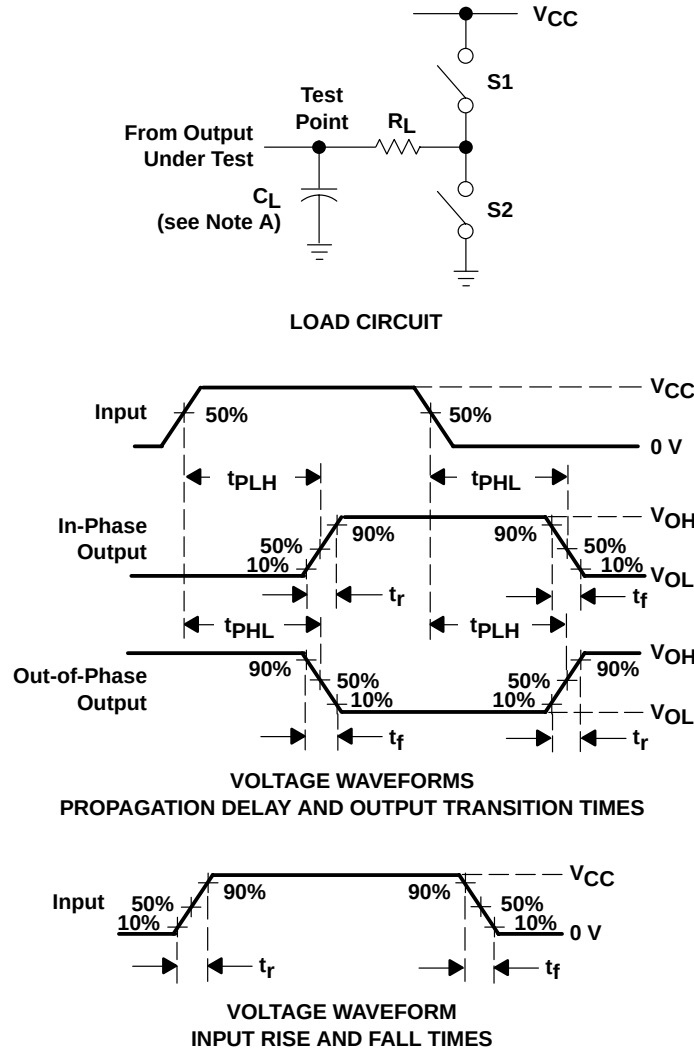
switching characteristics over recommended operating free-air temperature range,  $C_L = 150$  pF (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM<br>(INPUT) | TO<br>(OUTPUT) | $V_{CC}$ | $T_A = 25^\circ\text{C}$ |     |     | SN54HC645 |     | SN74HC645 |     | UNIT |
|-----------|-----------------|----------------|----------|--------------------------|-----|-----|-----------|-----|-----------|-----|------|
|           |                 |                |          | MIN                      | TYP | MAX | MIN       | MAX | MIN       | MAX |      |
| $t_{pd}$  | A or B          | B or A         | 2 V      |                          | 54  | 135 |           | 200 |           | 170 | ns   |
|           |                 |                | 4.5 V    |                          | 18  | 27  |           | 40  |           | 34  |      |
|           |                 |                | 6 V      |                          | 15  | 23  |           | 34  |           | 29  |      |
| $t_{en}$  | $\overline{OE}$ | A or B         | 2 V      |                          | 150 | 270 |           | 405 |           | 335 | ns   |
|           |                 |                | 4.5 V    |                          | 31  | 54  |           | 81  |           | 67  |      |
|           |                 |                | 6 V      |                          | 25  | 46  |           | 69  |           | 56  |      |
| $t_t$     |                 | A or B         | 2 V      |                          | 45  | 210 |           | 315 |           | 265 | ns   |
|           |                 |                | 4.5 V    |                          | 17  | 42  |           | 63  |           | 53  |      |
|           |                 |                | 6 V      |                          | 13  | 36  |           | 53  |           | 45  |      |

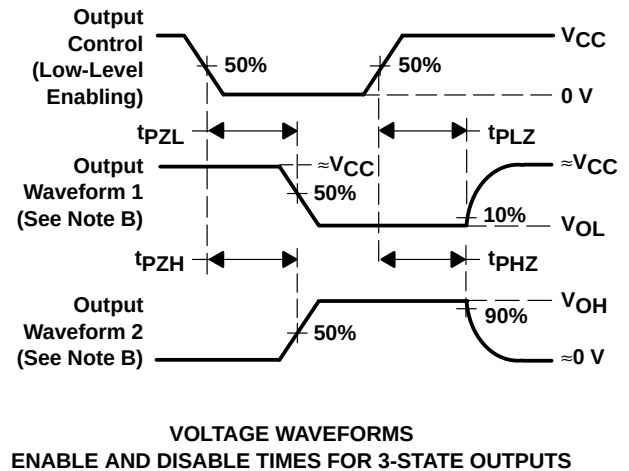
operating characteristics,  $T_A = 25^\circ\text{C}$

| PARAMETER |                                               | TEST CONDITIONS | TYP | UNIT |
|-----------|-----------------------------------------------|-----------------|-----|------|
| $C_{pd}$  | Power dissipation capacitance per transceiver | No load         | 40  | pF   |

**PARAMETER MEASUREMENT INFORMATION**



| PARAMETER         | $R_L$        | $C_L$           | S1     | S2     |
|-------------------|--------------|-----------------|--------|--------|
| $t_{en}$          | 1 k $\Omega$ | 50 pF or 150 pF | Open   | Closed |
|                   |              |                 | Closed | Open   |
| $t_{dis}$         | 1 k $\Omega$ | 50 pF           | Open   | Closed |
|                   |              |                 | Closed | Open   |
| $t_{pd}$ or $t_t$ | --           | 50 pF or 150 pF | Open   | Open   |



- NOTES:
- A.  $C_L$  includes probe and test-fixture capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1$  MHz,  $Z_O = 50 \Omega$ ,  $t_r = 6$  ns,  $t_f = 6$  ns.
  - D. The outputs are measured one at a time with one input transition per measurement.
  - E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

**Figure 1. Load Circuit and Voltage Waveforms**

## PACKAGING INFORMATION

| Orderable part number        | Status<br>(1) | Material type<br>(2) | Package   Pins | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|------------------------------|---------------|----------------------|----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">SN54HC645J</a>   | Active        | Production           | CDIP (J)   20  | 20   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | SN54HC645J          |
| SN54HC645J.A                 | Active        | Production           | CDIP (J)   20  | 20   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | SN54HC645J          |
| <a href="#">SN74HC645DW</a>  | Obsolete      | Production           | SOIC (DW)   20 | -                     | -           | Call TI                              | Call TI                           | -40 to 85    | HC645               |
| <a href="#">SN74HC645DWR</a> | Active        | Production           | SOIC (DW)   20 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | HC645               |
| SN74HC645DWR.A               | Active        | Production           | SOIC (DW)   20 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | HC645               |
| <a href="#">SN74HC645N</a>   | Active        | Production           | PDIP (N)   20  | 20   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -40 to 85    | SN74HC645N          |
| SN74HC645N.A                 | Active        | Production           | PDIP (N)   20  | 20   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -40 to 85    | SN74HC645N          |
| <a href="#">SNJ54HC645FK</a> | Active        | Production           | LCCC (FK)   20 | 55   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | SNJ54HC<br>645FK    |
| SNJ54HC645FK.A               | Active        | Production           | LCCC (FK)   20 | 55   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | SNJ54HC<br>645FK    |
| <a href="#">SNJ54HC645J</a>  | Active        | Production           | CDIP (J)   20  | 20   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | SNJ54HC645J         |
| SNJ54HC645J.A                | Active        | Production           | CDIP (J)   20  | 20   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | SNJ54HC645J         |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

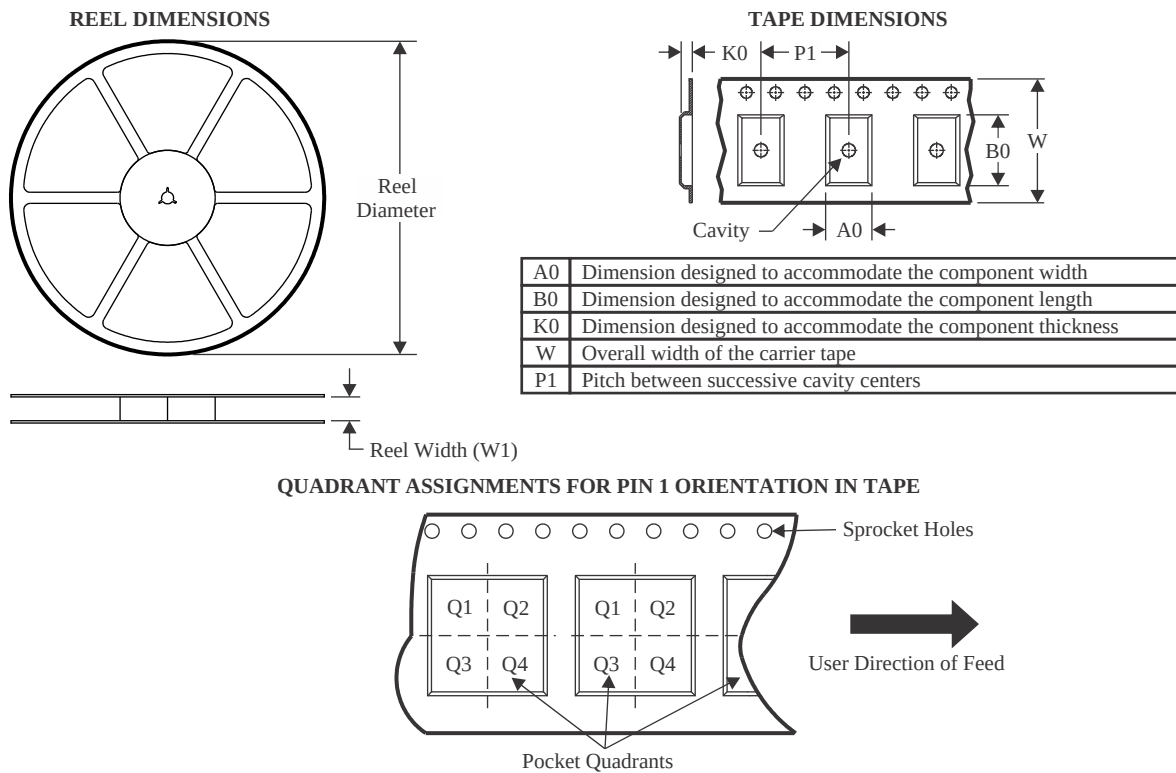
**OTHER QUALIFIED VERSIONS OF SN54HC645, SN74HC645 :**

- Catalog : [SN74HC645](#)
- Military : [SN54HC645](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION

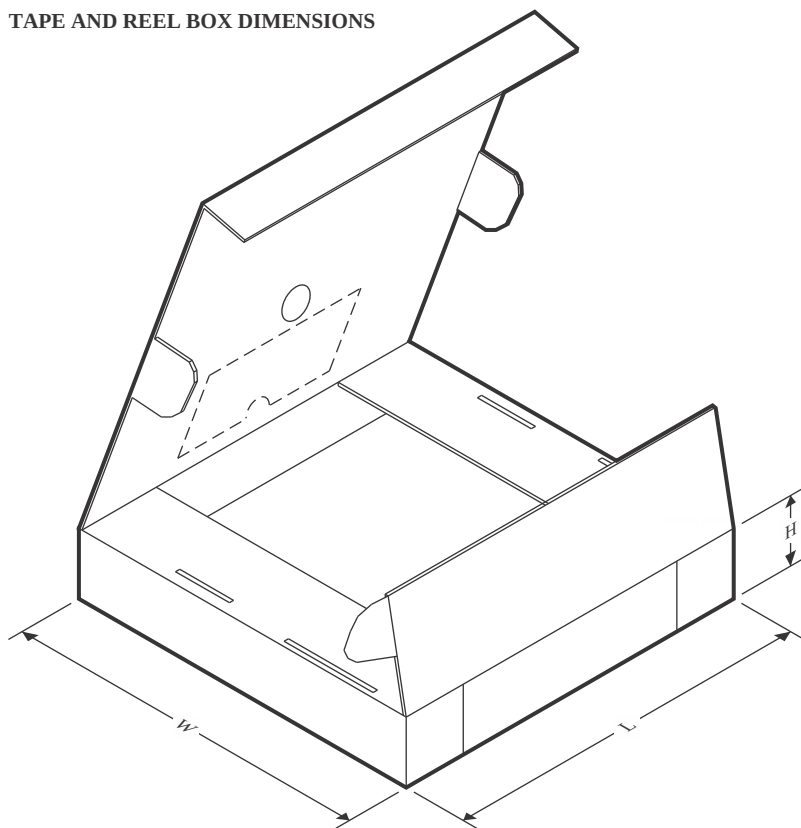


\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74HC645DWR | SOIC         | DW              | 20   | 2000 | 330.0              | 24.4               | 10.8    | 13.3    | 2.7     | 12.0    | 24.0   | Q1            |



## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74HC645DWR | SOIC         | DW              | 20   | 2000 | 356.0       | 356.0      | 45.0        |

**TUBE**

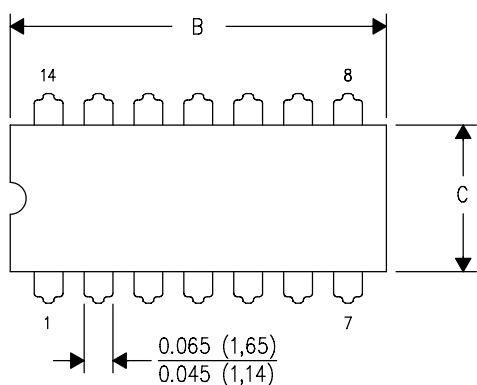

\*All dimensions are nominal

| Device         | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|----------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| SN74HC645N     | N            | PDIP         | 20   | 20  | 506    | 13.97  | 11230  | 4.32   |
| SN74HC645N.A   | N            | PDIP         | 20   | 20  | 506    | 13.97  | 11230  | 4.32   |
| SNJ54HC645FK   | FK           | LCCC         | 20   | 55  | 506.98 | 12.06  | 2030   | NA     |
| SNJ54HC645FK.A | FK           | LCCC         | 20   | 55  | 506.98 | 12.06  | 2030   | NA     |

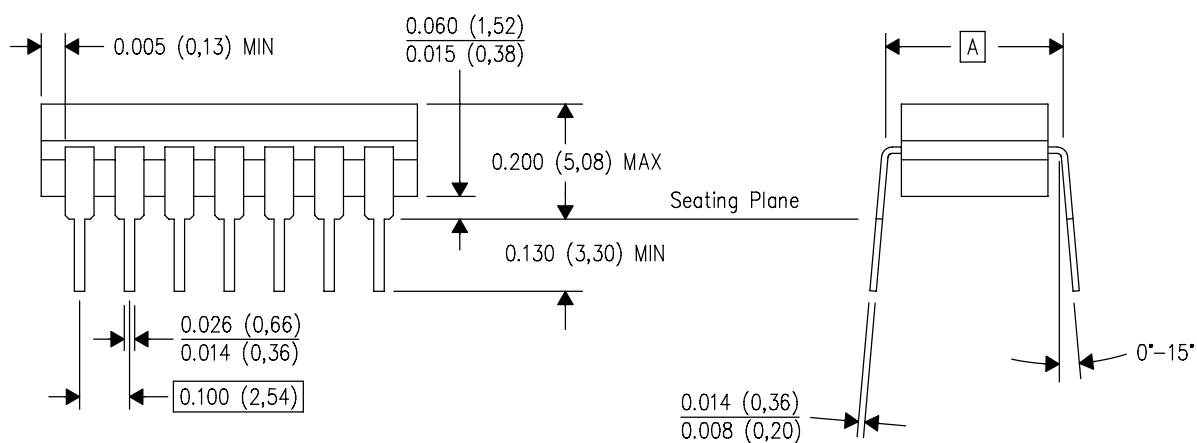
J (R-GDIP-T\*\*)

14 LEADS SHOWN

# CERAMIC DUAL IN-LINE PACKAGE



| PINS **<br>DIM | 14                     | 16                     | 18                     | 20                     |
|----------------|------------------------|------------------------|------------------------|------------------------|
| A              | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC |
| B MAX          | 0.785<br>(19,94)       | .840<br>(21,34)        | 0.960<br>(24,38)       | 1.060<br>(26,92)       |
| B MIN          | —                      | —                      | —                      | —                      |
| C MAX          | 0.300<br>(7,62)        | 0.300<br>(7,62)        | 0.310<br>(7,87)        | 0.300<br>(7,62)        |
| C MIN          | 0.245<br>(6,22)        | 0.245<br>(6,22)        | 0.220<br>(5,59)        | 0.245<br>(6,22)        |



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

## GENERIC PACKAGE VIEW

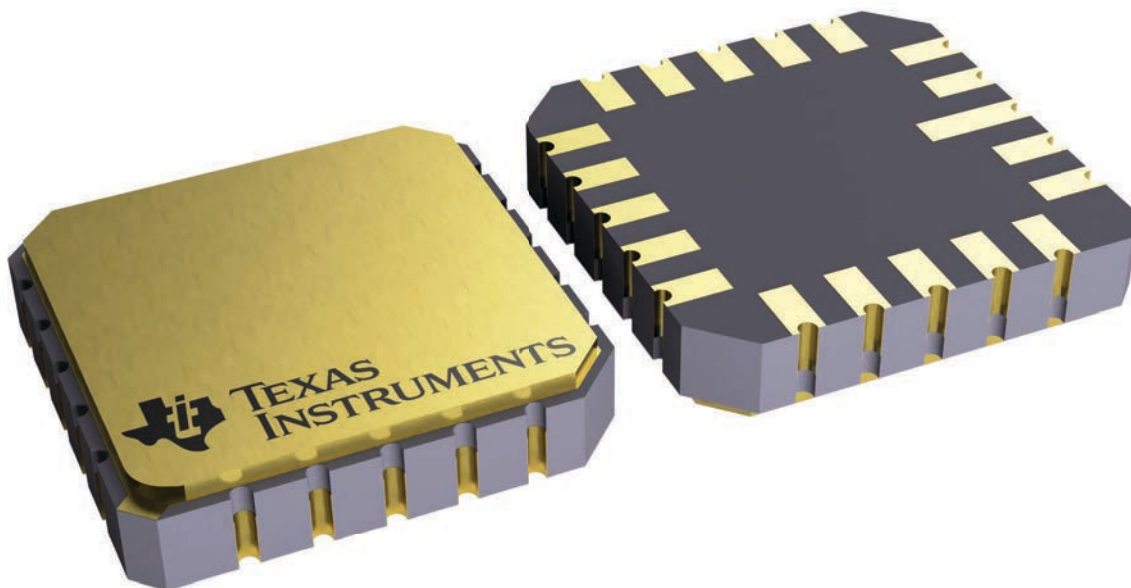
**FK 20**

**LCCC - 2.03 mm max height**

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

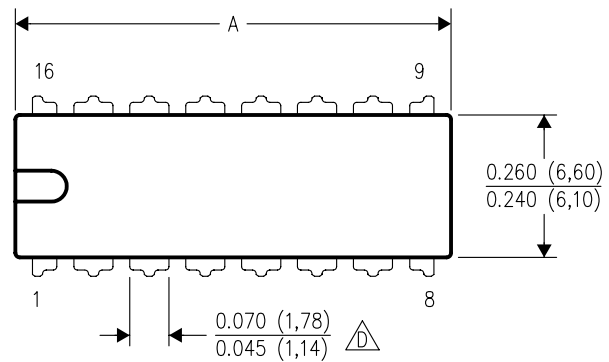


4229370VA\

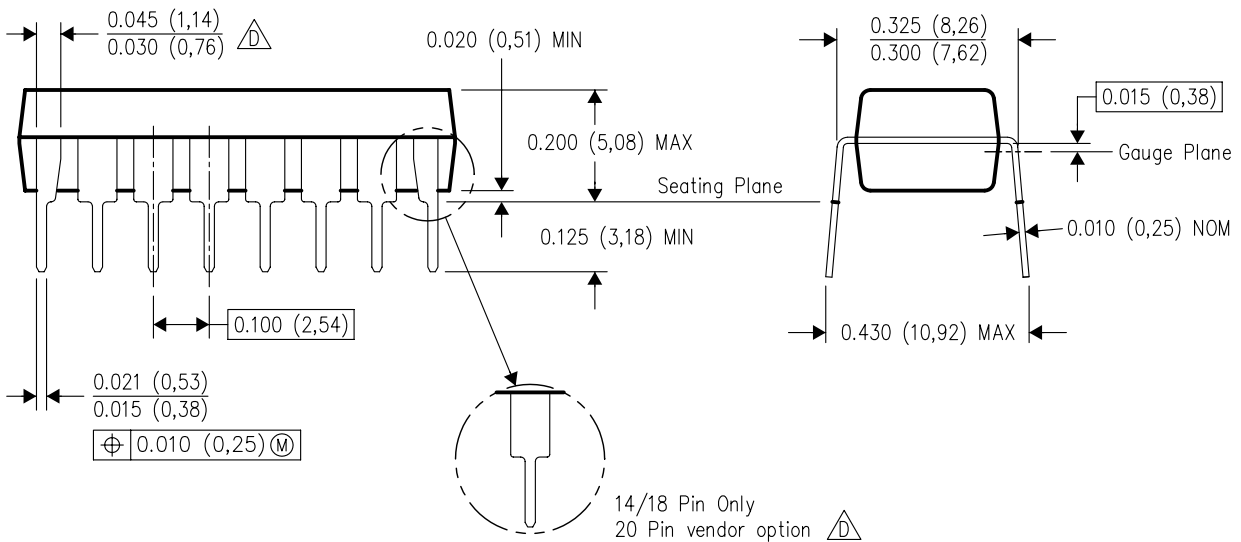
## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



| PINS **             | 14               | 16               | 18               | 20               |
|---------------------|------------------|------------------|------------------|------------------|
| DIM                 |                  |                  |                  |                  |
| A MAX               | 0.775<br>(19,69) | 0.775<br>(19,69) | 0.920<br>(23,37) | 1.060<br>(26,92) |
| A MIN               | 0.745<br>(18,92) | 0.745<br>(18,92) | 0.850<br>(21,59) | 0.940<br>(23,88) |
| MS-001<br>VARIATION | AA               | BB               | AC               | AD               |



14/18 Pin Only  
20 Pin vendor option

4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

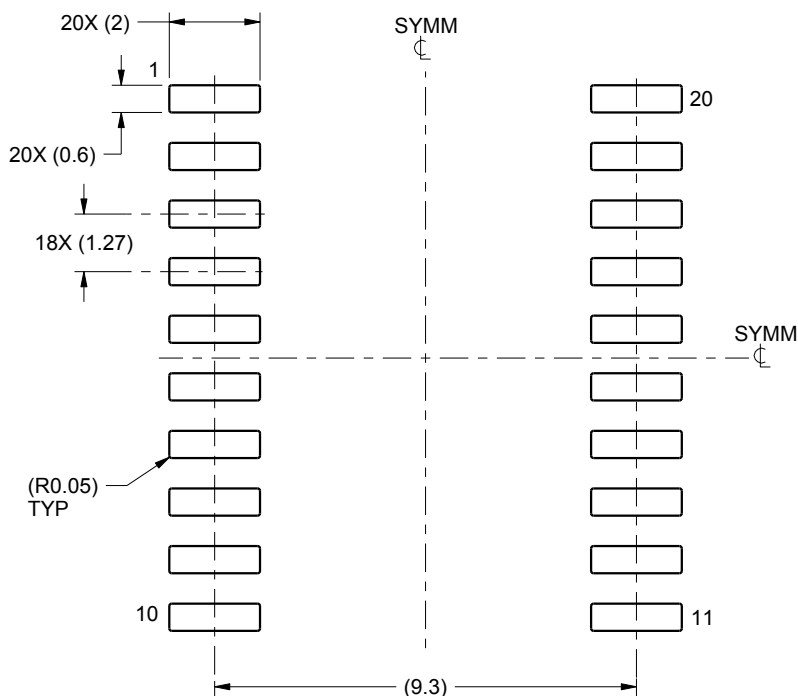


# EXAMPLE BOARD LAYOUT

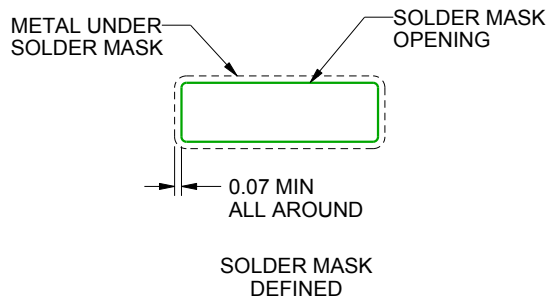
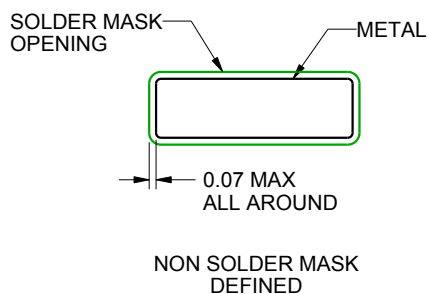
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

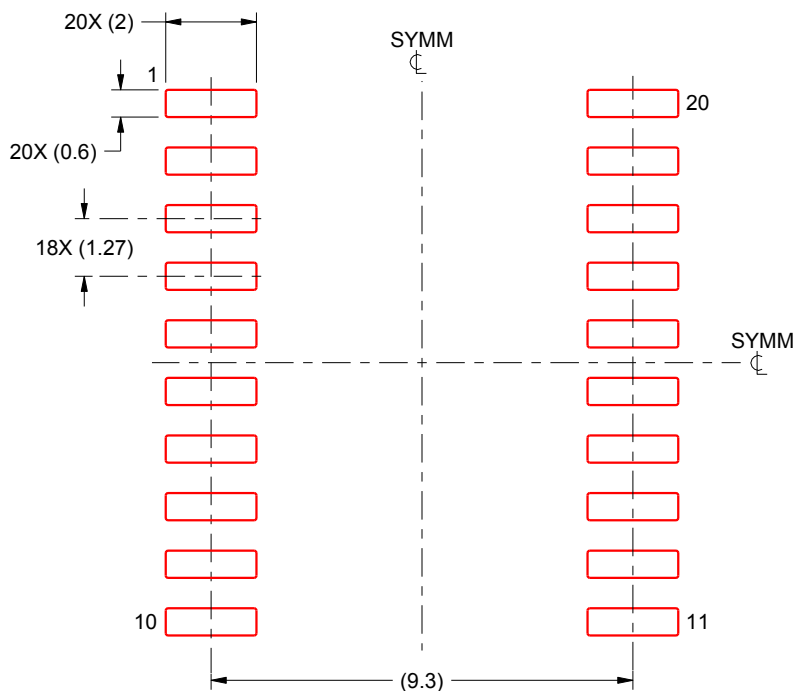
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2025, Texas Instruments Incorporated