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April 1, 2003

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HA16116FP/FPJ, HA16121FP/FPJ

Switching Regulator for Chopper Type DC/DC Converter

ADE-204-019A (Z)

Rev.1
Dec. 2000

Description

HA16116FP/FPJ and HA16121FP/FPJ are dual-channel PWM switching regulator controller ICs for use in chopper-type DC/DC converters.

This IC series incorporates totem pole gate drive circuits to allow direct driving of a power MOS FET. The output logic is preset for booster, step-down, or inverting control in a DC/DC converter. This logic assumes use of an N-channel power MOS FET for booster control, and a P-channel power MOS FET for step-down or inverting control.

HA16116 includes a built-in logic circuit for step-down control only, and one for use in both step-down and inverting control. HA16121 has a logic circuit for booster control only and one for both step-down and inverting control.

Both ICs have a pulse-by-pulse current limiter, which limits PWM pulse width per pulse as a means of protecting against overcurrent, and which uses an on/off timer for intermittent operation. Unlike conventional methods that use a latch timer for shutdown, when the pulse-by-pulse current limiter continues operation beyond the time set in the timer, the IC is made to operate intermittently (flickering operation), resulting in sharp vertical setting characteristics. When the overcurrent condition subsides, the output is automatically restored to normal.

The dual control circuits in the IC output identical triangle waveforms, for completely synchronous configuring a compact, high efficiency dual-channel DC/DC converter, with fewer external components than were necessary previously.

Functions

- 2.5 V reference voltage (Vref) regulator
- Triangle wave form oscillator
- Dual overcurrent detector
- Dual totem pole output driver
- UVL (under voltage lock out) system
- Dual error amplifier
- Vref overvoltage detector
- Dual PWM comparator

Features

- Wide operating supply voltage range* (3.9 V to 40.0 V)
- Wide operating frequency range (600 kHz maximum operation)
- Direct power MOS FET driving (output current ±1 A peak in maximum rating)
- Pulse-by-pulse overcurrent protection circuit with intermittent operation function (When overcurrent state continues beyond time set in timer, the IC operates intermittently to prevent excessive output current.)
- Grounding the ON/$\overline{\text{OFF}}$ pin turns the IC off, saving power dissipation. (HA16116: I_{OFF} = 10 µA max.; HA16121: I_{OFF} = 150 µA max.)
- Built-in UVL circuit (UVL voltage can be varied with external resistance.)
- Built-in soft start and quick shutoff functions

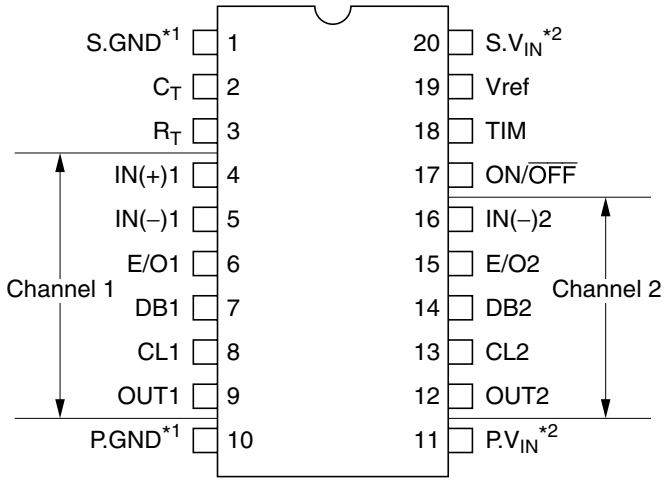
Note: The reference voltage 2.5 V is under the condition of $V_{IN} \geq 4.5$ V.

Ordering Information

Hitachi Control ICs for Chopper-Type DC/DC Converters

Channels	Product Number	Channel No.	Control Functions			Output Circuits	Overcurrent Protection
			Step-Up	Step-Down	Inverting		
Dual	HA17451	Ch 1	❍	❍	❍	Open collector	SCP with timer (latch)
		Ch 2	❍	❍	❍		
Single	HA16114	—	—	❍	❍	Totem pole power MOS FET driver	Pulse-by-pulse current limiter and intermittent operation by on/off timer
	HA16120	—	❍	—	—		
Dual	HA16116	Ch 1	—	❍	❍		
		Ch 2	—	❍	—		
	HA16121	Ch 1	—	❍	❍		
		Ch 2	❍	—	—		

Pin Arrangement



(Top view)

Notes: 1. Pins S.GND (pin 1) and P.GND (pin 10) have no direct internal interconnection. Both pins must be connected to ground.
2. Pins $S.V_{IN}$ (pin 20) and $P.V_{IN}$ (pin 11) have no direct internal interconnection. Both pins must be connected to V_{IN}.

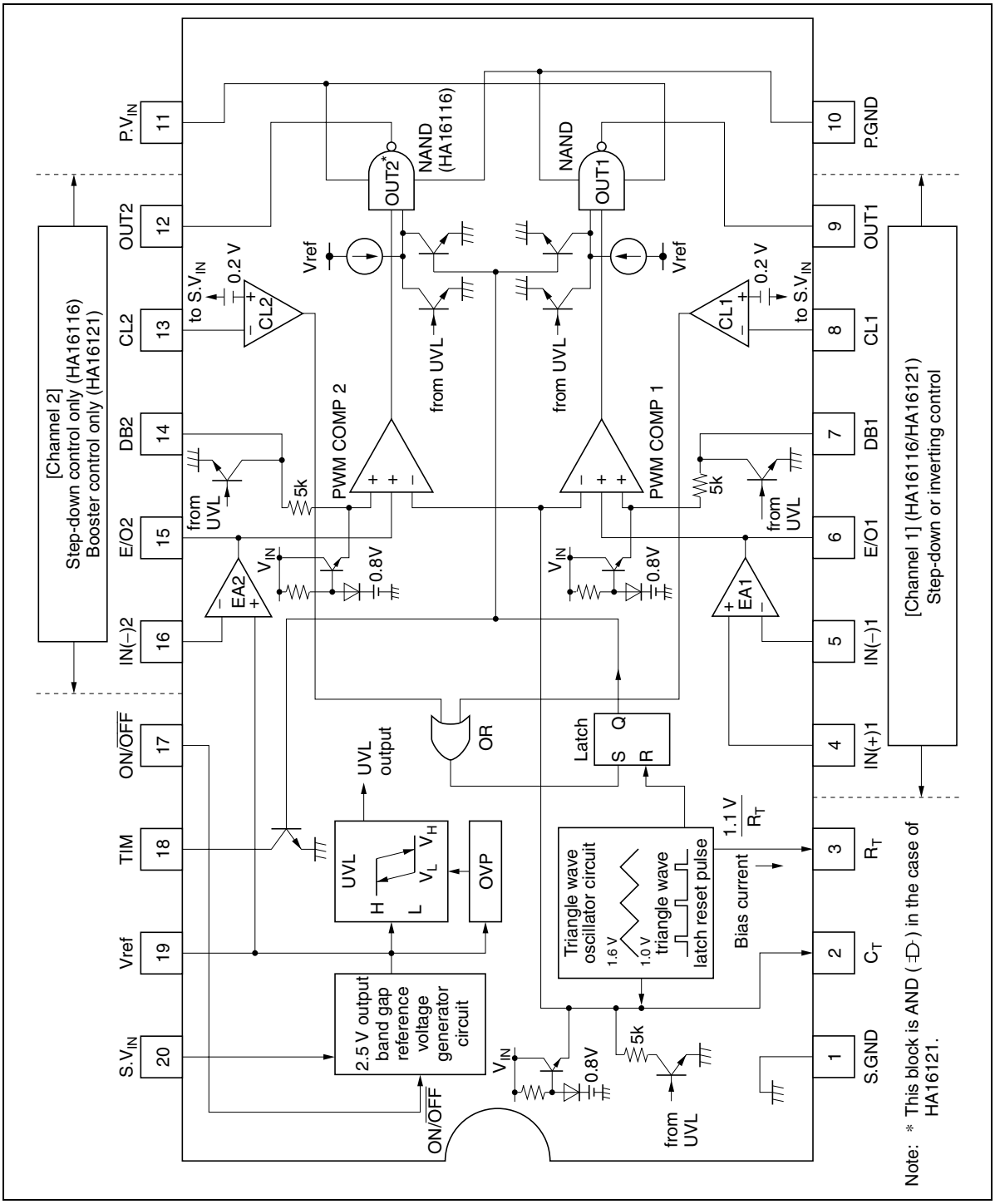
Pin Functions

Pin No.	Symbol	Function	
1	S.GND	Signal circuitry*1 ground	
2	C_T	Timing capacitance (triangle wave oscillator output)	
3	R_T	Timing resistance (for bias current synchronization)	
4	IN(+)1	Error amp. noninverting input (1)	Channel 1
5	IN(–)1	Error amp. inverting input (1)	
6	E/O1	Error amp. output (1)	
7	DB1	Dead band timer off period adjustment input (1)	
8	CL1	Overcurrent detection input (1)	
9	OUT1	PWM pulse output (1)	
10	P.GND	Output stage*1 ground	
11	$P.V_{IN}$	Output stage*1 power supply input	
12	OUT2	PWM pulse output (2)	Channel 2
13	CL2	Overcurrent detection input (2)	
14	DB2	Dead band timer off period adjustment input (2)	
15	E/O2	Error amp. output (2)	
16	IN(–)2	Error amp. inverting input (2)*2	
17	ON/$\overline{\text{OFF}}$	IC on/off switch input (off when grounded)	
18	TIM	Setting of intermittent operation timing when overcurrent is detected (collector input of timer transistor)	
19	Vref	2.5 V reference voltage output	
20	$S.V_{IN}$	Signal circuitry*1 power supply input	

Notes: 1. Here “output stage” refers to the power MOS FET driver circuits, and “signal circuitry” refers to all other circuits on the IC. Note that this IC is not protected against reverse insertion, which can cause breakdown of the IC between V_{IN} and GND. Be careful to insert the IC correctly.

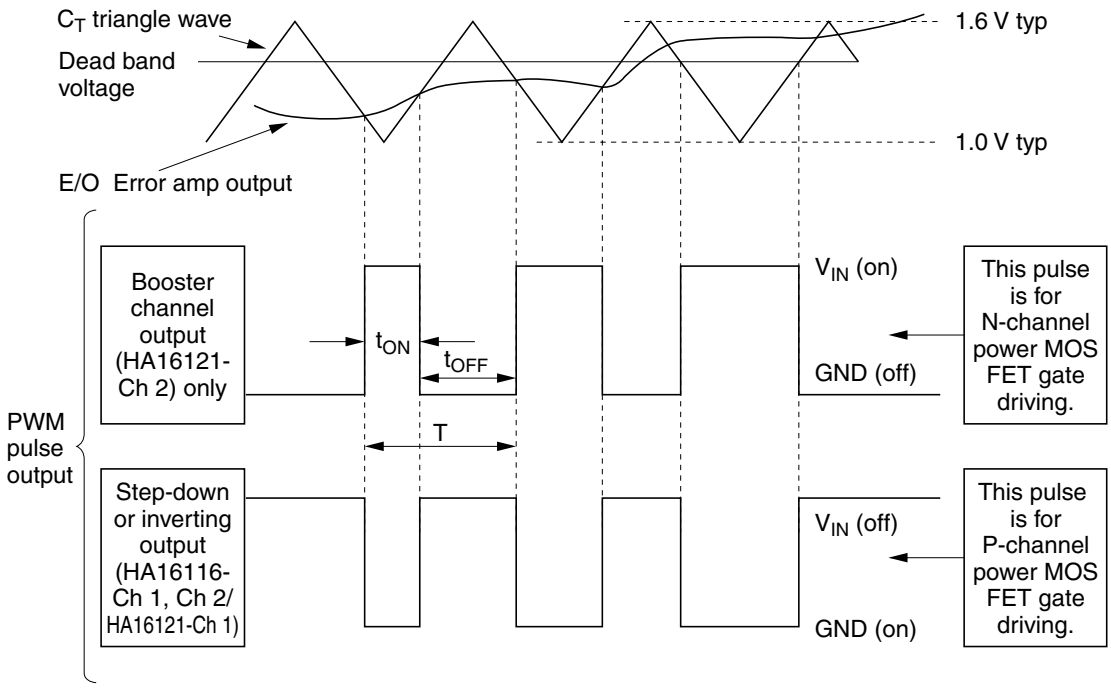
2. Noninverting input of the channel 2 error amp is connected internally to Vref.

Block Diagram



Function and Timing Chart

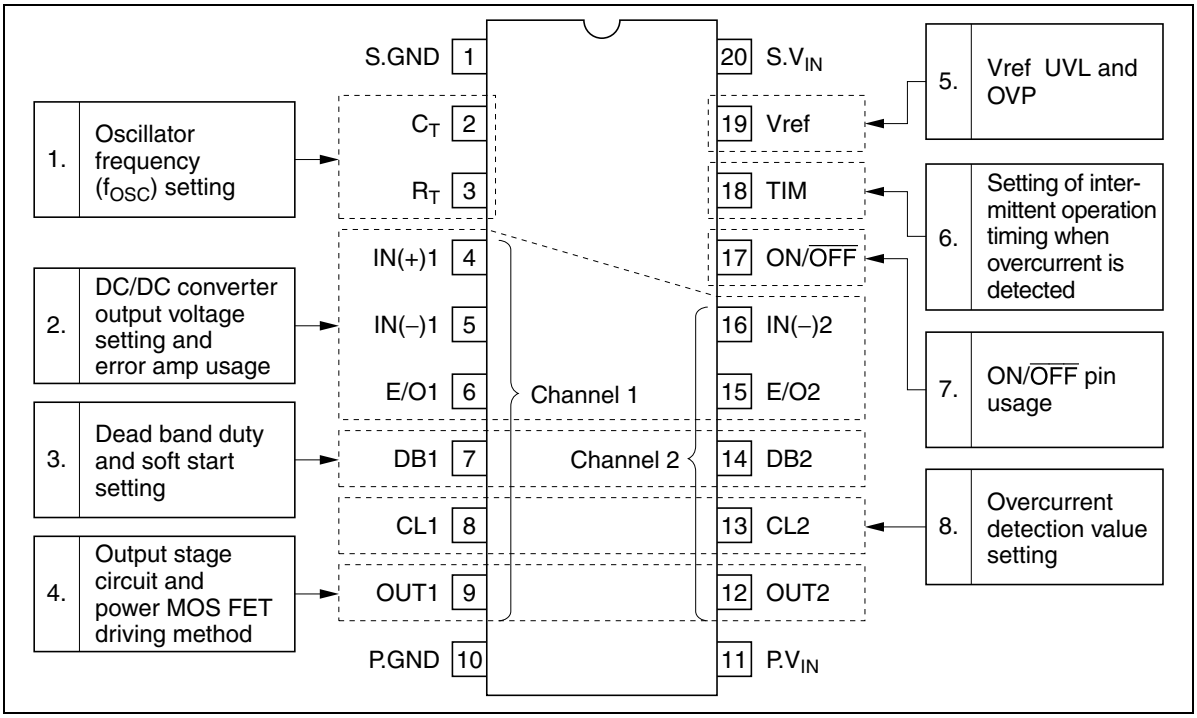
Relation between triangle wave and PWM output (in steady-state operation)



Note: On duty = t_{ON}/T, where $T = 1/f_{OSC}$.

Determining External Component Constants (pin usage)

Constant settings are explained for the following items.



1. Oscillator Frequency (f_{osc}) Setting

Figure 1.1 shows an equivalent circuit for the triangle wave oscillator.

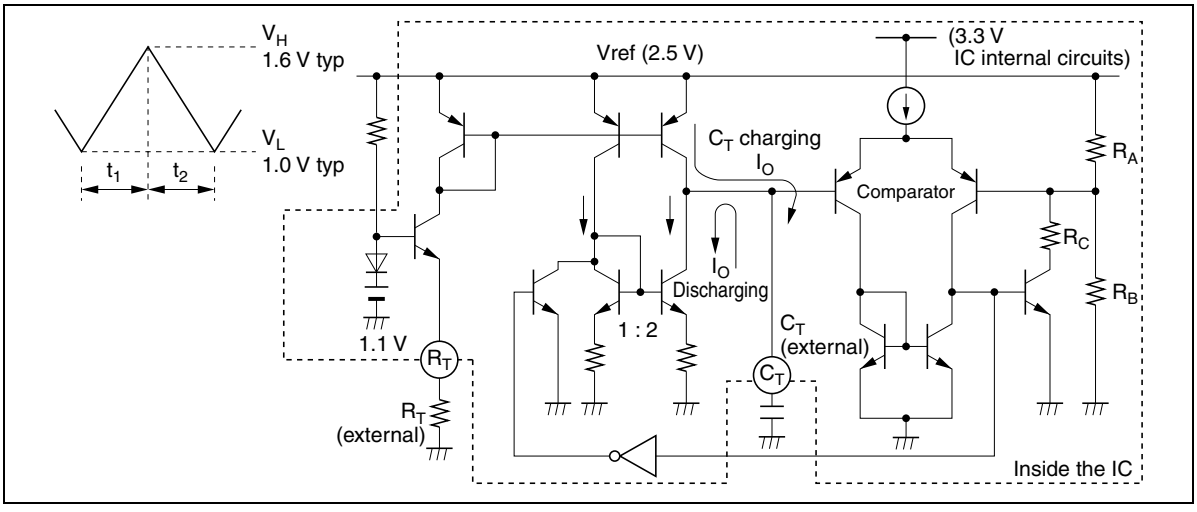


Figure 1.1 Equivalent Circuit for the Triangle Wave Oscillator

The triangle wave is a voltage waveform used as a reference in creating a PWM pulse. This block operates according to the following principles. A constant current I_O, determined by an external timing resistor R_T, is made to flow continuously to external timing capacitor C_T. When the C_T pin voltage exceeds the comparator threshold voltage V_H, the comparator output causes a switch to operate, discharging a current I_O from C_T. Next, when the C_T pin voltage drops below threshold voltage V_L, the comparator output again causes the switch to operate, stopping the I_O discharge. The triangle wave is generated by this repeated operation.

Note that $I_O = 1.1\ V/R_T$. Since the I_O current mirror circuit has a very limited current producing ability, R_T should be set to $\geq 5\ k\Omega$ ($I_O \geq 220\ \mu A$).

With this IC series, V_H and V_L of the triangle wave are fixed internally at about 1.6 V and 1.0 V by the internal resistors R_A, R_B, and R_C. The oscillator frequency can be calculated as follows.

$$f_{OSC} = \frac{1}{t_1 + t_2 + t_3}$$

Here,

$$t_1 = \frac{C_T \cdot (V_H - V_L)}{1.1\ V/R_T} = \frac{C_T R_T \cdot (V_H - V_L)}{1.1\ V}$$

$$t_2 = \frac{C_T \cdot (V_H - V_L)}{(2-1) \times 1.1\ V/R_T} = \frac{C_T R_T \cdot (V_H - V_L)}{1.1\ V} = t_1$$

$$V_H - V_L = 0.6\ V$$

$$t_1 = t_2 = \frac{0.6}{1.1} C_T R_T$$

$t_3 \approx 0.8\ \mu s$ (comparator delay time in the oscillator)

Accordingly,

$$f_{OSC} \approx \frac{1}{2t_1 + t_3} \approx \frac{1}{1.1\ C_T R_T + 0.8\ \mu s}\ [Hz]$$

Note that the value of f_{OSC} may differ slightly from the above calculation depending on the amount of delay in the comparator circuit. Also, at high frequencies this comparator delay can cause triangle wave overshoot or undershoot, skewing the dead band threshold. Confirm the actual value in implementation and adjust the constants accordingly.

2. DC/DC Converter Output Voltage Setting and Error Amp Usage

2.1 Positive Voltage Booster ($V_O > V_{IN}$) or Step-Down ($V_{IN} > V_O >$ Vref)

Use $V_O = \frac{R_1 + R_2}{R_2} \cdot \text{Vref}$ (V)

Booster output is possible only at channel 2 of HA16121. For step-down output, both channels of HA16116 or channel 1 of HA16121 are used.

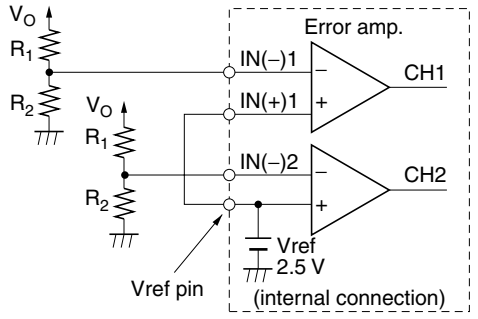


Figure 2.1

2.2 Negative Voltage ($V_o <$ Vref) for Inverting Output

Use $V_O = -\text{Vref} \cdot \left(\frac{R_1}{R_1 + R_2} \cdot \frac{R_3 + R_4}{R_3} - 1 \right)$ (V)

Channel 1 is used for inverting output on both ICs.

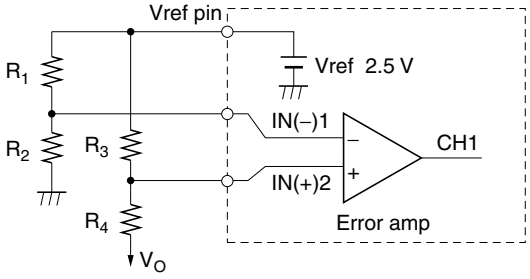


Figure 2.2 Inverting Output

2.3 Error Amplifier

Figure 2.3 shows an equivalent circuit of the error amplifier. The error amplifier on these ICs is configured of a simple NPN transistor differential input amplifier and the output circuit of a constant-current driver.

This amplifier features wide bandwidth (f_T = 4 MHz) with open loop gain kept to 50 dB, allowing stable feedback to be applied when the power supply is designed. Phase compensation is also easy.

Both HA16116 and HA16121 have a noninverting input (IN(+)) pin, in order to allow use of the channel 1 error amplifier for inverting control. The channel 2 error amplifier, on the other hand, is used for step-down control in HA16116 and booster control in HA16121; so the channel 2 noninverting input is connected internally to Vref.

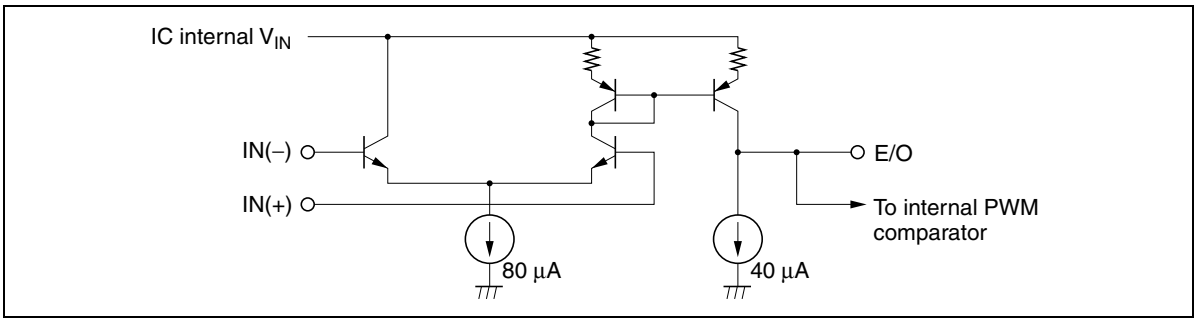


Figure 2.3 Error Amplifier Equivalent Circuit

3. Dead Band (DB) Duty and Soft Start Setting (common to both channels)

3.1 Dead Band Duty Setting

Dead band duty is set by adjusting the DB pin input voltage (V_{DB}). A convenient means of doing this is to connect two external resistors to the Vref of this IC so as to divide V_{DB} (see figure 3.1).

$$V_{DB} = Vref \times \frac{R_2}{R_1 + R_2} \ (V)$$

$$Duty\ (DB) = \frac{V_{TH} - V_{DB}}{V_{TH} - V_{TL}} \times 100\ (\%) \cdots \text{This applies when } V_{DB} > V_{TL}.$$

If $V_{DB} < V_{TL}$, there is no PWM output.

$$Here,\ T = \frac{1}{f_{OSC}}$$

Note: V_{TH}: 1.6 V (Typ)
V_{TL}: 1.0 V (Typ)

Vref is typically 2.5 V. Select R_1 and R_2 so that 1.0 V ≤ V_{DB} ≤ 1.6 V.

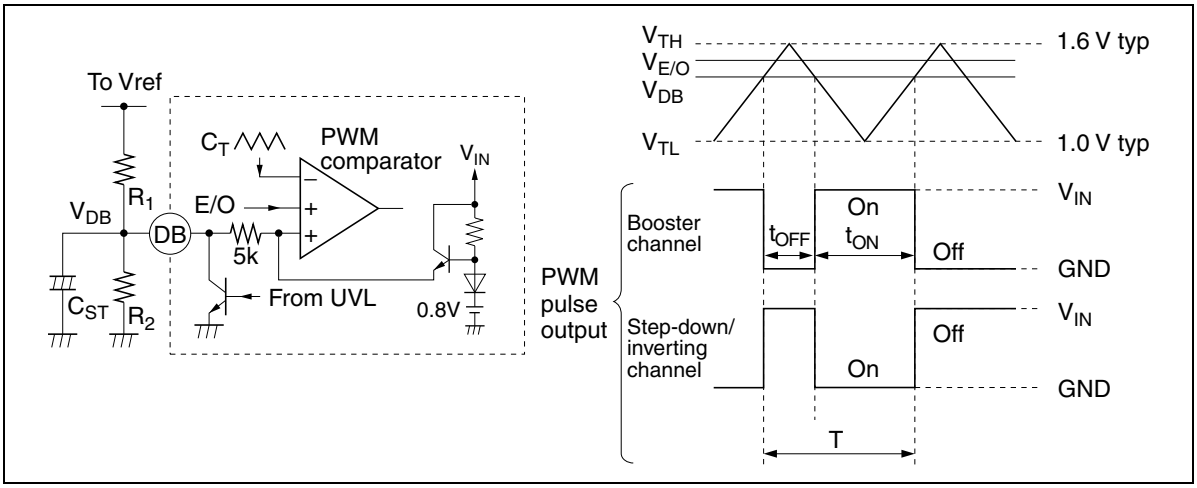


Figure 3.1 Dead Band Duty Setting

3.2 Soft Start (SST) Setting (each channel)

When the power is turned on, the soft start function gradually raises V_{DB} (refer to section 3.1), and the PWM output pulse width gradually widens. This function is realized by adding a capacitor C_{ST} to the DB pin. The function is realized as follows.

In the figure 3.2, the DB pin is clamped internally at approximately 0.8 V, which is 0.2 V lower than the triangle wave V_{TL} = 1.0 V typ.

t_A: Standby time until PWM pulse starts widening.

t_B: Time during which SST is in effect.

During soft start, the DB pin voltage in the figure below is as expressed in the following equation.

$$V_{SST} = V_{DB} \cdot \left(1 - e^{\frac{-t - t_{0.8}}{T}}\right), \quad t_{SST} = t_A + t_B$$

Here,

$$t_{0.8} = -T \ln \left(1 - \frac{0.8}{V_{DB}}\right), \quad T = C_{ST} \cdot (R_1 // R_2)$$

How to select values: If the soft start time t_{SST} is too short, the DC/DC converter output voltage will tend to overshoot. To prevent this, set t_{SST} to a few tens of ms or above.

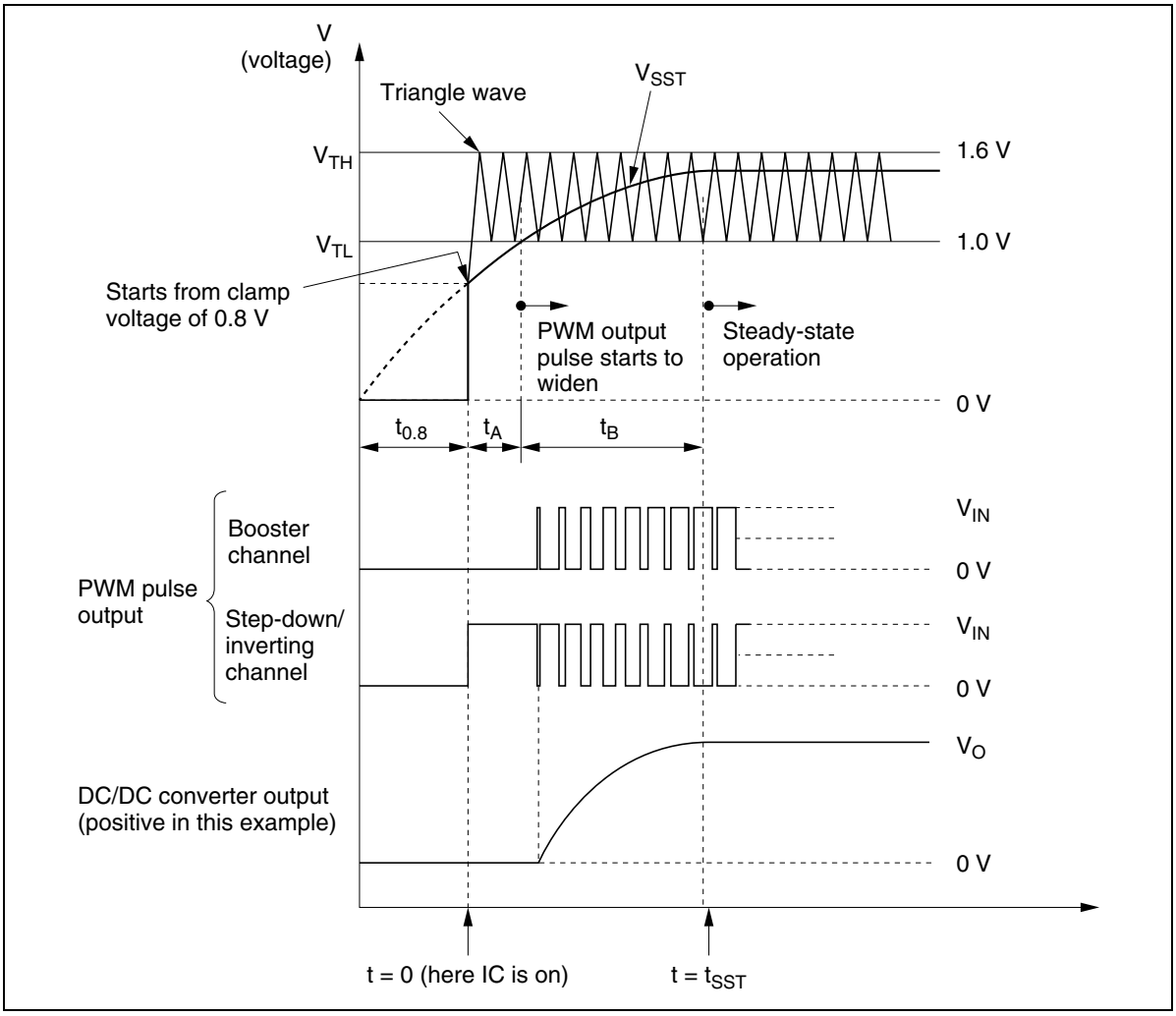


Figure 3.2 Soft Start (SST) Setting

4. Totem Pole Output Stage Circuit and Power MOS FET Driving Method

The output stage of this IC series is configured of totem pole circuits, allowing direct connection to a power MOS FET as an external switching device, so long as V_{IN} is below the gate breakdown voltage.

If there is a possibility that V_{IN} will exceed the gate breakdown voltage of the power MOS FET, a Zener diode circuit like that shown figure 4.1 or other protective measures should be used. The figure 4.1 shows an example using a P-channel power MOS FET.

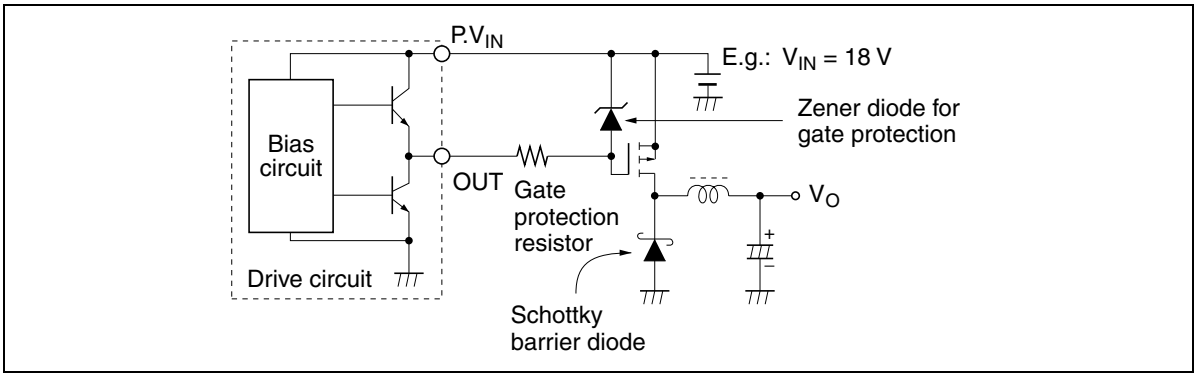


Figure 4.1 P-channel Power MOS FET (example)

5. Vref Undervoltage Error Prevention (UVL) and Overvoltage Protection (OVP) Functions

5.1 Operation Principles

The reference voltage circuit is equipped with UVL and OVP functions.

- UVL

  In normal operation the Vref output voltage is fixed at 2.5 V. If V_{IN} is lower than normal, the UVL circuit detects the Vref output voltage with a hysteresis of 1.7 V and 2.0 V, and shuts off the PWM output if Vref falls below this level, in order to prevent malfunction.

- OVP

  The OVP circuit protects the IC from inadvertent application of a high voltage from outside, such as if V_{IN} is shorted. A Zener diode (5.6 V) and resistor are used between Vref and GND for overvoltage detection. PWM output is shut off if Vref exceeds approximately 7.0 V.

Note that the PWM output pulse logic and the precision of the switching regulator output voltage are not guaranteed at an applied voltage of 2.5 V to 7 V.

5.2 Quick Shutoff

When the UVL circuit goes into operation, a sink transistor is switched on as in the figure below, drawing off the excess current. This transistor also functions when the IC is turned off, drawing off current from the C_T, E/O, and DB pins and enabling quick shutoff.

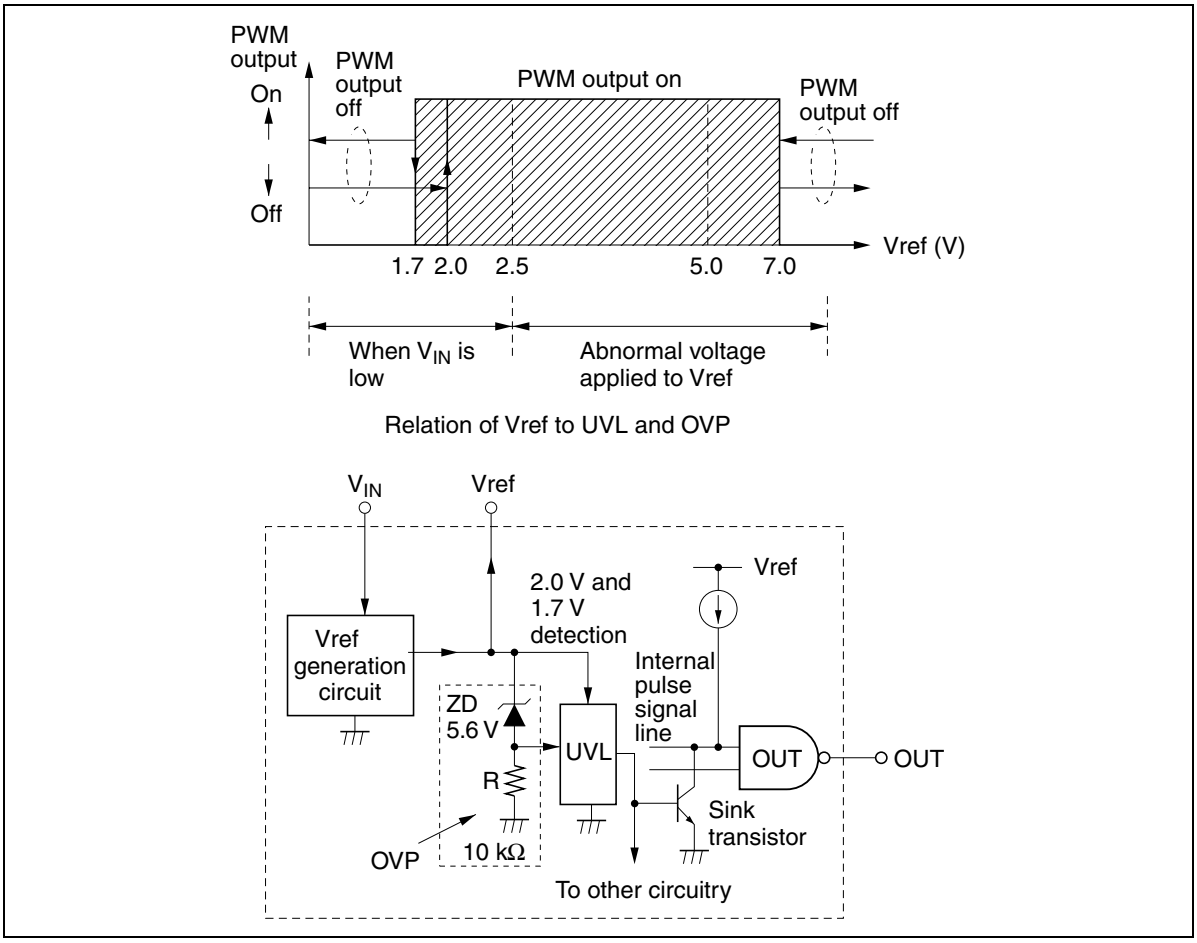


Figure 5.1 Quick Shutoff

6. Setting of Intermittent Operation Timing when Overcurrent is Detected

6.1 Operation Principles

The current limiter on this IC detects overcurrent in each output pulse, providing pulse-by-pulse overcurrent protection by limiting pulse output whenever an overcurrent is detected. If the overcurrent state continues, the TIM pin and ON/$\overline{\text{OFF}}$ pin can be used to operate the IC intermittently. As a result, a power supply with sharp vertical characteristics can be configured.

The ON/$\overline{\text{OFF}}$ timing for intermittent operation makes use of the hysteresis in the ON/$\overline{\text{OFF}}$ pin threshold voltage V_{ON} and V_{OFF}, such that $V_{ON} - V_{OFF} = V_{BE}$. Setting method is performed as described on the following pages. V_{BE} is based-emitter voltage of internal transistor.

Note: When an overcurrent is detected in one channel of this IC but not the other, the pulse-by-pulse current limiter still goes into operation on both channels. Also, when the intermittent operation feature is not used, the TIM pin should be set to open state and the ON/$\overline{\text{OFF}}$ pin pulled up to high level (above V_{ON}).

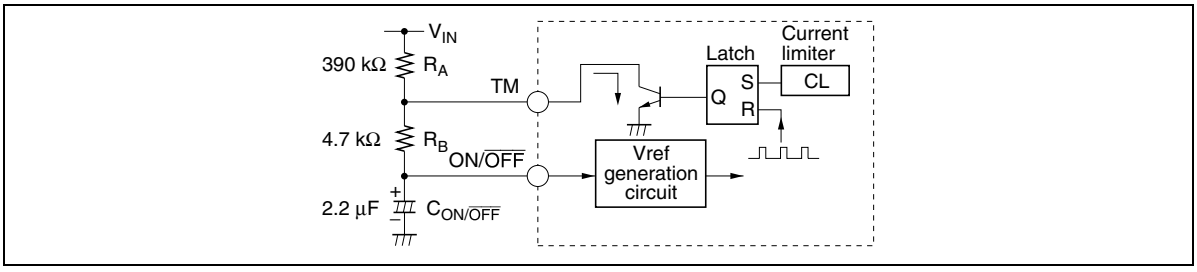
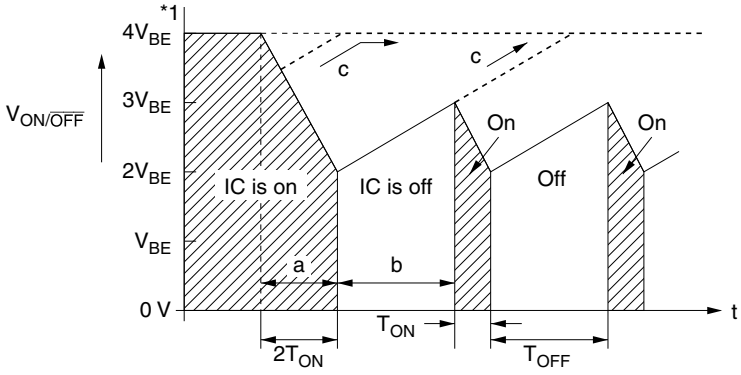


Figure 6.1 Connection Diagram (example)

6.2 Intermittent Operation Timing Chart ($V_{ON/\overline{OFF}}$ only)



a. Continuous overcurrent detected
b. Intermittent operation starts (IC is off)
c. Overcurrent cleared (dotted line)

Note: 1.V_{BE} is the base-emitter voltage in transistors on the IC, and is approximately 0.7 V (see the figure 7.1).
For details, see the overall waveform timing diagram.

Figure 6.2 Intermittent Operation Timing Chart

6.3 Calculating Intermittent Operation Timing

Intermittent operation timing is calculated as follows.

(1) T_{ON} time (the time until the IC is shut off when continuous overcurrent occurs)

$$T_{ON} = C_{ON/\overline{OFF}} \times R_B \times \ln\left(\frac{3V_{BE}}{2V_{BE}}\right) \times \left(\frac{1}{1 - \text{On duty}^*}\right)$$

$$= C_{ON/\overline{OFF}} \times R_B \times \ln 1.5 \times \left(\frac{1}{1 - \text{On duty}^*}\right) \approx 0.4 \times C_{ON/\overline{OFF}} \times R_B \times \left(\frac{1}{1 - \text{On duty}^*}\right)$$

(2) T_{OFF} time (when the IC is off, the time until it next goes on)

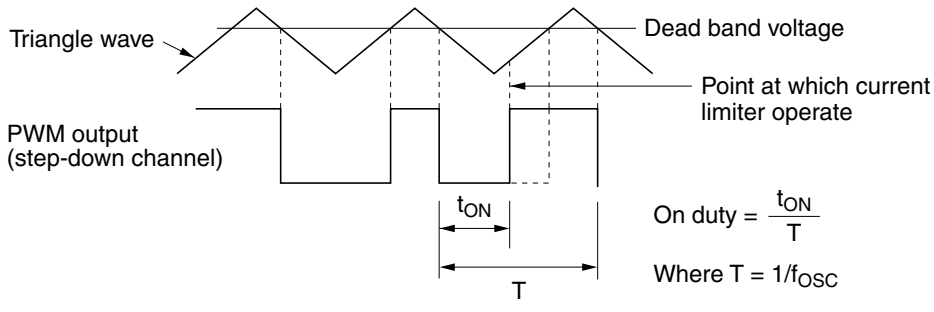
$$T_{OFF} = C_{ON/\overline{OFF}} \times (R_A + R_B) \times \ln\left(\frac{V_{IN} - 2V_{BE}}{V_{IN} - 3V_{BE}}\right)$$

Where, $V_{BE} \approx 0.7$ V

Note: 1. On duty is the percent of time the IC is on during one PWM cycle when the pulse-by-pulse current limiter is operating.

From the first equation (1) above, it is seen that the shorter the time T_{ON} when the pulse-by-pulse current limiter goes into effect (resulting in a larger overload), the smaller the value T_{ON} becomes.

As seen in the second equation (2), T_{OFF} is a function of V_{IN}. Further, according to this setting, when V_{IN} is switched on, the IC goes on only after T_{OFF} has elapsed.



Note: On duty is the percent of time the IC is on during one PWM cycle when the pulse-by-pulse current limiter is operating.

Figure 6.3

6.4 Examples of Intermittent Operation Timing (calculated values)

(1) T_{ON}

$T_{ON} = T_1 \times C_{ON/\overline{OFF}} \times R_B$

Here, coefficient

$T_1 = 0.4 \times \dfrac{1}{1 - \text{On duty}}$

from section 6.3 (1) previously.

Example: If $C_{ON/\overline{OFF}} = 2.2\ \mu F$, $R_B = 4.7\ k\Omega$, and the on duty of the current limiter is 75%, then $T_{ON} = 16$ ms.

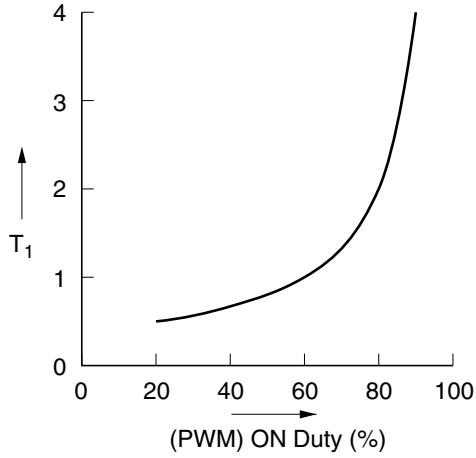


Figure 6.4 Examples of Intermittent Operation Timing (1)

(2) T_{OFF}

$T_{OFF} = T_2 \times C_{ON/\overline{OFF}} \times (R_A + R_B)$

Here, coefficient

$T_2 = \ln \dfrac{V_{IN} - 2V_{BE}}{V_{IN} - 3V_{BE}}$

from section 6.3 (2) previously.

Example: If $C_{ON/\overline{OFF}} = 2.2\ \mu F$, $R_B = 4.7\ k\Omega$, $R_A = 390\ k\Omega$, $V_{IN} = 12$ V, then $T_{OFF} = 60$ ms.

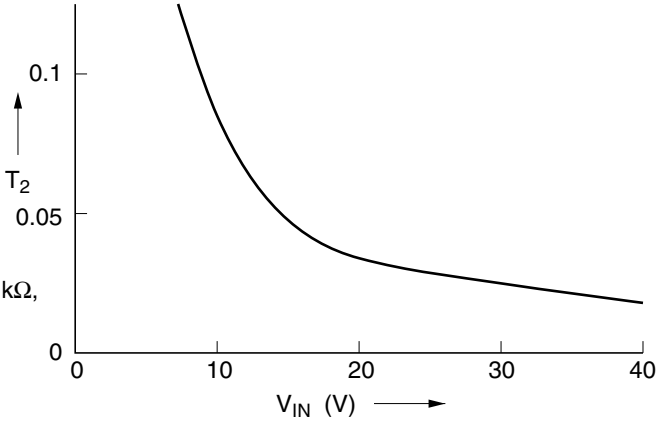


Figure 6.5 Examples of Intermittent Operation Timing (2)

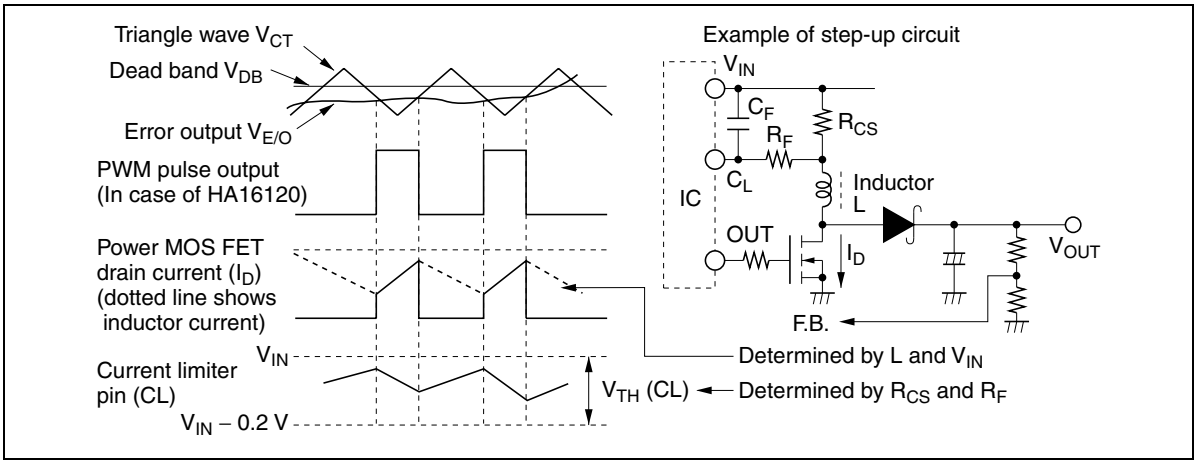


Figure 6.6

7. ON/$\overline{\text{OFF}}$ Pin Usage

7.1 IC Shutoff by the ON/$\overline{\text{OFF}}$ Pin

As shown in the figure 7.1, these ICs can be turned off safely by lowering the voltage at the ON/$\overline{\text{OFF}}$ pin to below $2V_{BE}$. This feature is used to conserve the power in the power supply system. In off state the IC current consumption (I_{OFF}) is 10 µA (Max) for HA16116 and 150 µA (Max) for HA16121.

The ON/$\overline{\text{OFF}}$ pin can also be used to drive logic ICs such as TTL or CMOS with a sink current of 50 µA (Typ) at an applied voltage of 5 V. When it is desired to employ this feature along with intermittent operation, an open collector or open drain logic IC should be used.

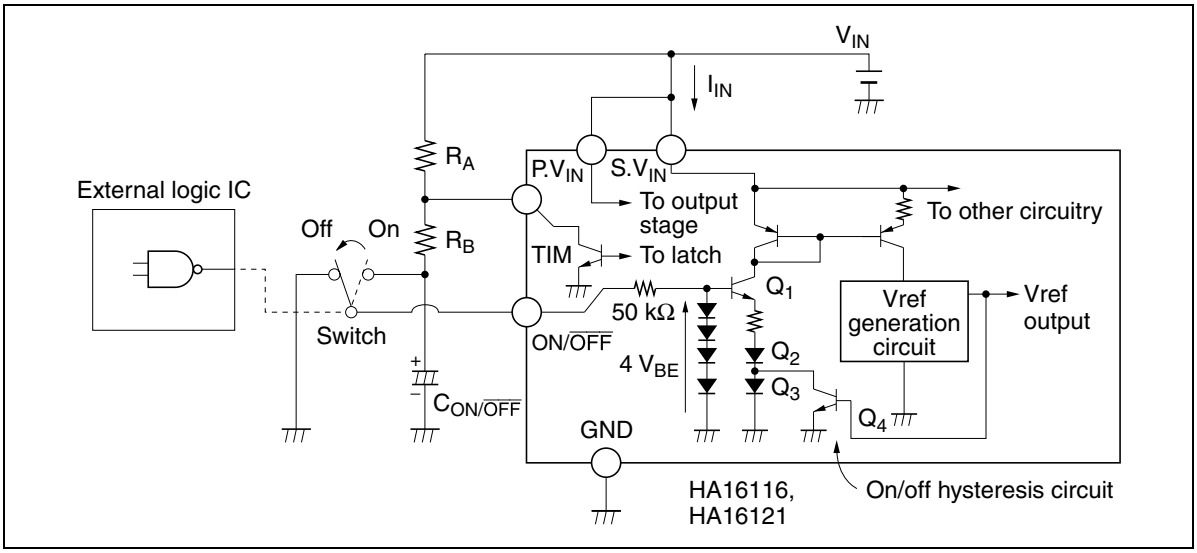


Figure 7.1 IC Shutoff by the ON/$\overline{\text{OFF}}$ Pin

7.2 Adjusting UVL Voltage (when intermittent operation is not used)

The UVL voltage setting in this IC series can be adjusted externally as shown below.

Using the relationships shown in the figure, the UVL voltage in relation to V_{IN} can be adjusted by changing the relative values of V_{TH} and V_{TL}.

When the IC is operating, transistor Q_4 is off, so $V_{ON} = 3V_{BE} \approx 2.1$ V. Accordingly, by connecting resistors R_C and R_D, the voltage at which UVL is cancelled is as follows.

$$V_{IN} = 2.1\ V \times \frac{R_C + R_D}{R_D}$$

This V_{IN} is simply the supply voltage at which the UVL stops functioning, so in this state Vref is still below 2.5 V. In order to restore Vref to 2.5 V, a V_{IN} of approximately 4.3 V should be applied.

With this IC series, $V_{ON/\overline{OFF}}$ makes use of the V_{BE} of internal transistors, so when designing a power supply system it should be noted that V_{ON} has a temperature dependency of around –6 mV/°C.

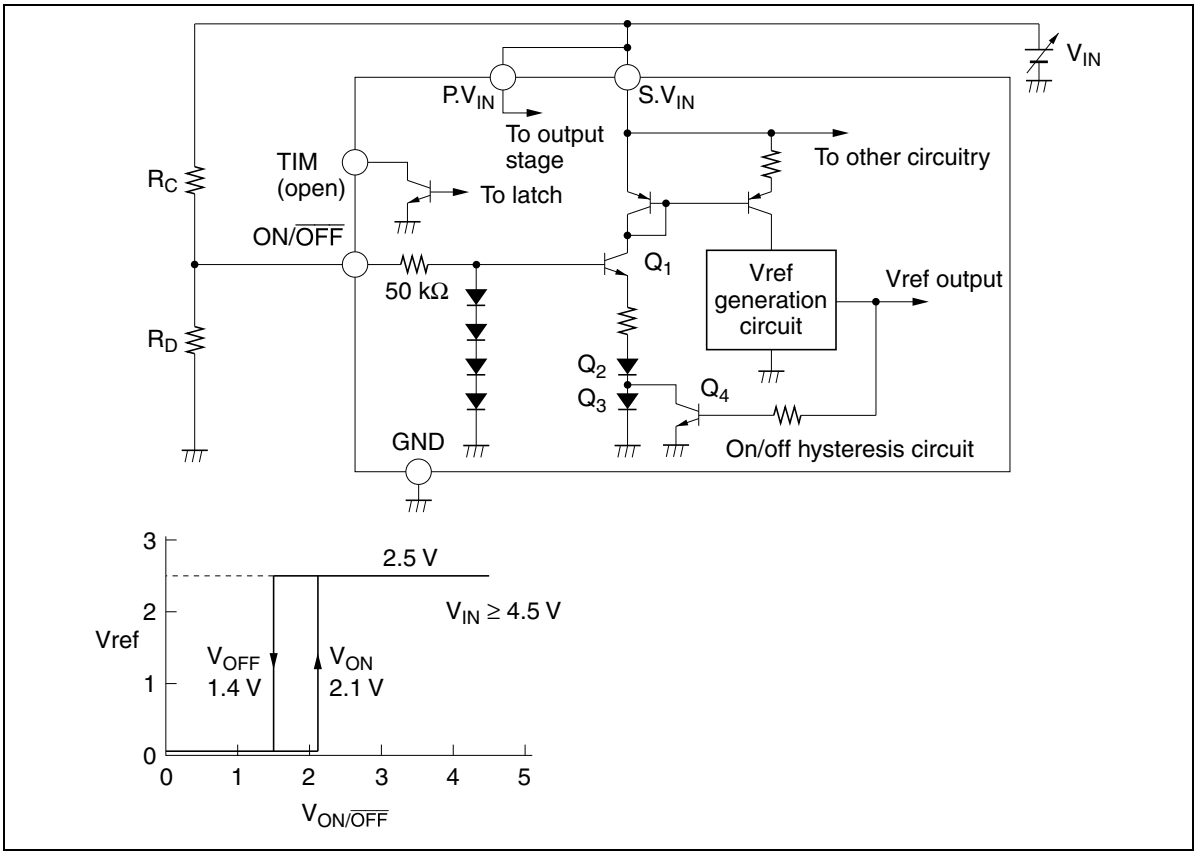


Figure 7.2 Adjusting UVL Voltage

Overcurrent Detection Value Setting

The overcurrent detection value V_{TH} for this IC series is 0.2 V (Typ) and the bias current is 200 µA (Typ) The power MOS FET peak current value before the current limiter goes into operation is derived from the following equation.

$$I_D = \frac{V_{TCL} - (R_F + R_{CS}) \cdot I_{BCL}}{R_{CS}}$$

Here $V_{TH} = V_{IN} - V_{CL} = 0.2$ V, V_{CL} is a voltage referd on GND.

Note that C_F and R_{CS} form a low-pass filter, determined by their time constants, that prevents malfunctions from current spikes when the power MOS FET is turned on or off.

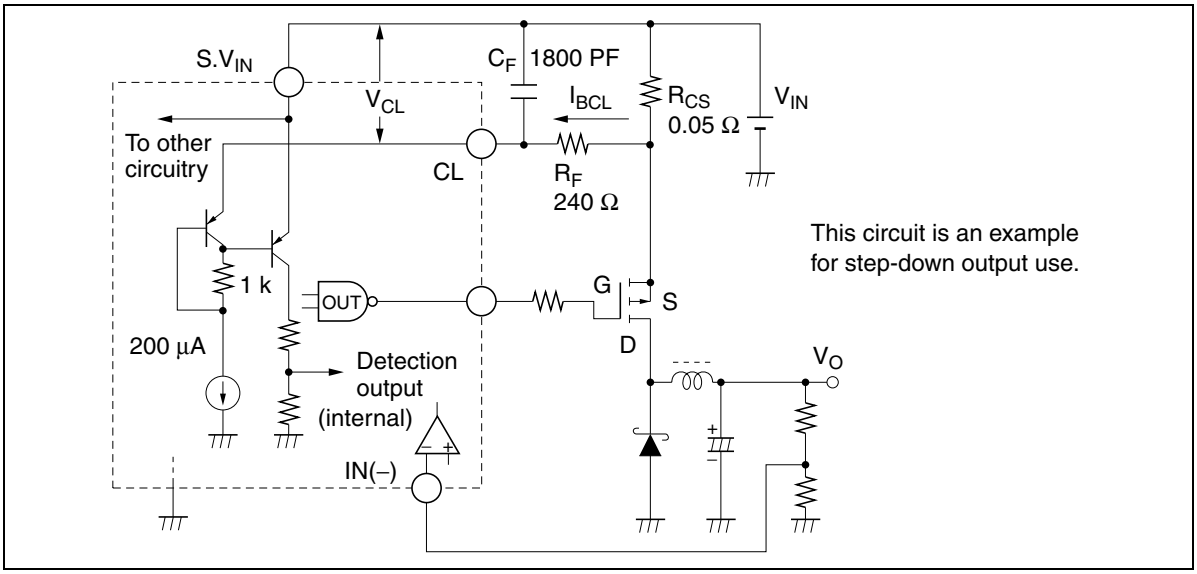


Figure 8.1 Example for Step-Down Use

The sample values given in this figure are calculated from the following equation.

$$I_D = \frac{0.2\ \text{V} - (240\ \Omega + 0.05\ \Omega) \times 200\ \mu\text{A}}{0.05\ \Omega} = 3.04\ [\text{A}]$$

The filter cutoff frequency is calculated as follows.

$$f_C = \frac{1}{2\pi\, C_F\, R_F} = \frac{1}{6.28 \times 1800\ \text{pF} \times 240\ \Omega} = 370\ [\text{kHz}]$$

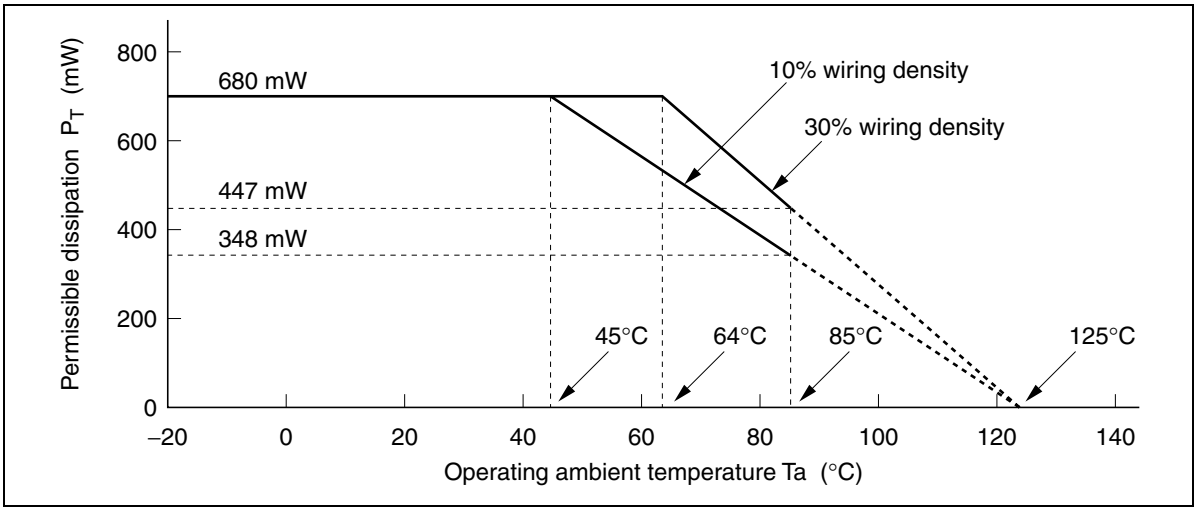
Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Rating		Unit
		HA16116FP, HA16121FP	HA16116FPJ, HA16121FPJ	
Supply voltage	V_{IN}	40	40	V
Output current (DC)	I_O	±0.1	±0.1	A
Output current (peak)	I_O peak	±1.0	±1.0	A
Current limiter pin voltage	V_{CL}	V_{IN}	V_{IN}	V
Error amp input voltage	V_{IEA}	V_{IN}	V_{IN}	V
E/O input voltage	$V_{IE/O}$	Vref	Vref	V
RT pin source current	I_{RT}	500	500	µA
TIM pin sink current	I_{TM}	20	20	mA
Power dissipation*1	P_T	680*1,*2	680*1,*2	mW
Operation temperature range	Topr	–20 to +85	–40 to +85	°C
Junction temperature	TjMax	125	125	°C
Storage temperature range	Tstg	–55 to +125	–55 to +125	°C

Note: 1. This value is based on actual measurements on a 40 × 40 × 1.6 mm glass epoxy circuit board. At a wiring density of 10%, it is the permissible value up to Ta = 45°C, but at higher temperatures this value should be derated by 8.3 mW/°C. At a wiring density of 30% it is the permissible value up to Ta = 64°C, but at higher temperatures it should be derated by 11.1 mW/°C.

2. For the DILP package.
This value applies up to Ta = 45°C; at temperatures above this, 8.3 mW/°C derating should be applied.



Electrical Characteristics

(Ta = 25°C, V_{IN} = 12 V, f_{OSC} = 300 kHz)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Reference voltage block	Output voltage	Vref	2.45	2.50	2.55	V	I_O = 1 mA
	Line regulation	Line	—	30	60	mV	4.5 V ≤ V_{IN} ≤ 40 V
	Load regulation	Load	—	30	60	mV	0 ≤ I_O ≤ 10 mA
	Output shorting current	I_{OS}	10	25	—	mA	Vref = 0 V
	Vref OVP voltage	Vrovp	6.2	6.8	7.0	V	
	Output voltage temperature dependence	ΔVref/ΔTa	—	100	—	ppm/°C	
Triangle wave oscillator block	Maximum oscillator frequency	f_{OSCmax}	600	—	—	kHz	
	Minimum oscillator frequency	f_{OSCmin}	—	—	1	Hz	
	Oscillator frequency input voltage stability	$\Delta f_{OSC}/\Delta V_{IN}$	—	±1	±3	%	4.5 V ≤ V_{IN} ≤ 40 V
	Oscillator frequency temperature stability	$\Delta f_{OSC}/\Delta Ta$	—	±5	—	%	–20°C ≤ Ta ≤ 85°C
	Oscillator frequency	f_{OSC}	270	300	330	kHz	C_T = 220 pF, R_T = 10 kΩ)
Dead band adjust block	Low-level threshold voltage	V_{TLDB}	0.87	0.97	1.07	V	Output on duty 0%
	High-level threshold voltage	V_{THDB}	1.48	1.65	1.82	V	Output on duty 100%
	Threshold differential voltage	ΔV_{TDB}	0.55	0.65	0.75	V	$\Delta V_{TH} = V_{TH} - V_{TL}$
	Output source current	$I_{Osource\ (DB)}$	100	150	200	μA	DB pin = 0 V
PWM comparator block	Low-level threshold voltage	V_{TLCMP}	0.87	0.97	1.07	V	Output on duty = 0%
	High-level threshold oltage	V_{THCMP}	1.48	1.65	1.82	V	Output on duty = 100%
	Threshold differential voltage	ΔV_{TCMP}	0.55	0.65	0.75	V	$\Delta V_{TH} = V_{TH} - V_{TL}$
	Dead band precision	DBdev	–5	0	+5	%	Deviation when $V_{EO} = (V_{TL} + V_{TH})/2$, duty = 50 %

Electrical Characteristics (cont.)

(Ta = 25°C, V_{IN} = 12 V, f_{OSC} = 300 kHz)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Error amp block	Input offset voltage	V_{IOEA}	—	2	10	mV	
	Input bias current	I_{BEA}	—	0.8	2	µA	
	Output sink current	$I_{Osink\ (EA)}$	28	40	52	µA	In open loop, V_I = 3 V, V_O = 2 V
	Output source current	$I_{Osource\ (EA)}$	28	40	52	µA	In open loop, V_I = 2 V, V_O = 1 V
	Voltage gain	A_V	40	50	—	dB	f = 10 kHz
	Unity gain band-width	BW	3	4	—	MHz	
	High-level output voltage	V_{OHEA}	2.2	3.0	—	V	I_O = 10 µA
	Low-level output voltage	V_{OLEA}	—	0.2	0.5	V	I_O = 10 µA
Overcurrent detection block	Threshold voltage	V_{TCL}	V_{IN}–0.22	V_{IN}–0.2	V_{IN}–0.18	V	
	CL bias current	I_{BCL}	150	200	250	µA	C_L = V_{IN}
	Operating time	t_{OFFCL}	—	200	300	ns	C_L = V_{IN} –0.3 V
			—	500	600	ns	Applies only to ch 2 of HA16121
Output stage	Output low voltage	V_{OL1}	—	0.7	2.2	V	I_{Osink} = 10 mA Applies only to HA16116
			—	1.6	1.9	V	I_{Osink} = 10 mA Applies only to HA16121
			—	1.0	1.3	V	I_{Osink} = 0 mA Applies only to HA16121
	Off state low voltage	V_{OL2}	—	1.6	1.9	V	I_{Osink} = 1 mA ON/$\overline{OFF}$ pin = 0 V Applies only to ch 2 of HA16121
			—	1.0	1.3	V	I_{Osink} = 0 mA ON/$\overline{OFF}$ = 0 V Applies only to ch 2 of HA16121
	Output high voltage	V_{OH1}	V_{IN}–1.9	V_{IN}–1.6	—	V	$I_{Osource}$ = 10 mA
			V_{IN}–1.3	V_{IN}–1.0	—	V	$I_{Osource}$ = 0 A
	Off state high voltage	V_{OH2}	V_{IN}–1.9	V_{IN}–1.6	—	V	$I_{Osource}$ = 1 mA ON/$\overline{OFF}$ pin = 0 V
			V_{IN}–1.3	V_{IN}–1.0	—	V	$I_{Osource}$ = 0 A ON/$\overline{OFF}$ pin = 0 V
	Rise time	t_r	—	70	130	ns	C_L = 1000 pF (to V_{IN}) *1, *2
	Fall time	t_f	—	70	130	ns	C_L = 1000 pF (to V_{IN}) *1, *2

Electrical Characteristics (cont.)

(Ta = 25°C, V_{IN} = 12 V, f_{OSC} = 300 kHz)

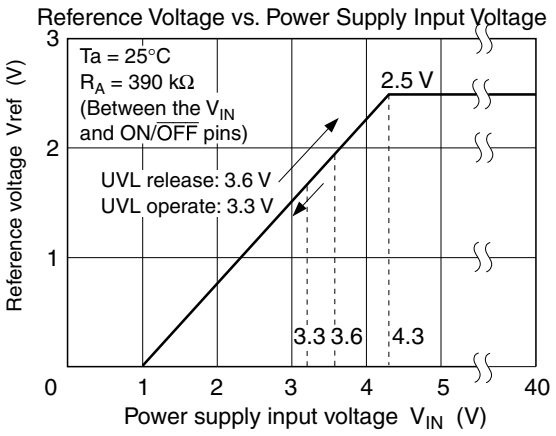
Item		Symbol	Min	Typ	Max	Unit	Test Conditions
UVL block	V_{IN} high-level threshold voltage	V_{TUH1}	3.3	3.6	3.9	V	
	V_{IN} low-level threshold voltage	V_{TUL1}	3.0	3.3	3.6	V	
	V_{IN} threshold differential voltage	ΔV_{TU1}	0.1	0.3	0.5	V	$\Delta V_{TU1} = V_{TUH1} - V_{TUL1}$
	Vref high-level threshold voltage	V_{TUH2}	1.7	2.0	2.3	V	
	Vref low-level threshold voltage	V_{TUL2}	1.4	1.7	2.0	V	
	Vref threshold differential voltage	ΔV_{TU2}	0.1	0.3	0.5	V	$\Delta V_{TU2} = V_{TUH2} - V_{TUL2}$
ON/OFF block	ON/$\overline{OFF}$ pin sink current	$I_{ON/\overline{OFF}}$	—	35	50	µA	ON/$\overline{OFF}$ pin = 5 V
	IC on-state voltage	V_{ON}	1.8	2.1	2.4	V	
	IC off-state voltage	V_{OFF}	1.1	1.4	1.7	V	
	ON/OFF threshold differential voltage	$\Delta V_{ON/\overline{OFF}}$	0.5	0.7	0.9	V	
TIM block	TIM pin sink current in steady state	I_{TIM1}	0	—	10	µA	CL pin = V_{IN}, V_{TIM} = 0.3 V
	TIM pin sink current at overcurrent detection	I_{TIM2}	10	15	20	mA	CL pin = V_{IN} – 0.3 V V_{TIM} = 0.3 V
Common block	Operating current	I_{IN}	6.0	8.5	11.1	mA	C_L = 0 pF (to V_{IN}) *1, *2
			8.5	12.1	15.7	mA	C_L = 500 pF (to V_{IN}) *1, *2
			11.0	15.7	20.5	mA	C_L = 1000 pF (to V_{IN}) *1, *2
	Off current	I_{OFF}	0	—	10	µA	HA16116FP ON/$\overline{OFF}$ pin = 0 V
			0	120	150	µA	HA16121FP

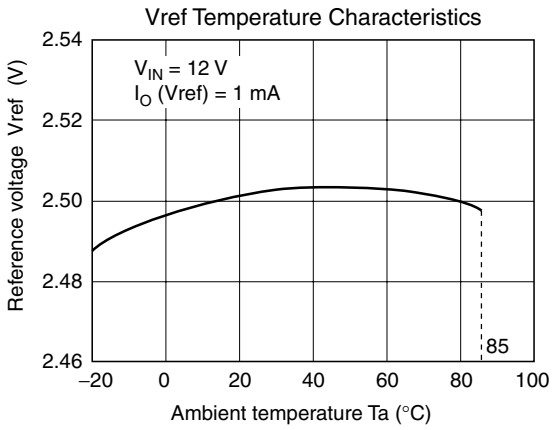
Notes: 1. C_L is load capacitor for Power MOS FET's gate, and C_L = 1000 pF to GND in the case of HA16121 – ch 2.

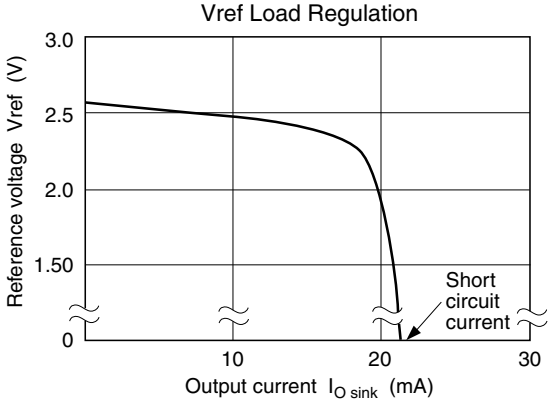
2. C_L in channel 2 of HA16121 is connected to GND.

Characteristic Curves

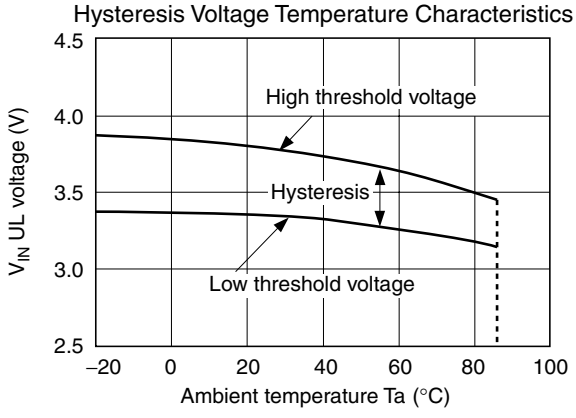
- Reference Voltage Block (Vref)





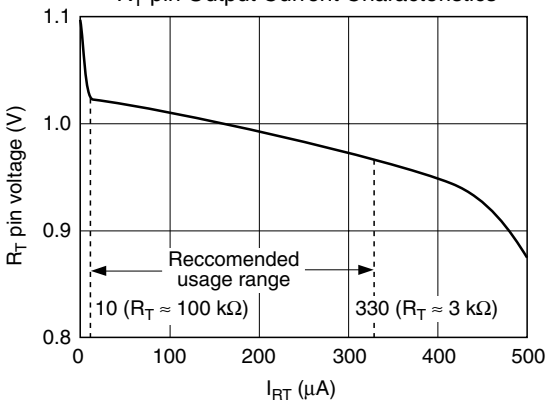


- UVL (Low Input Voltage Malfunction Prevention) Block

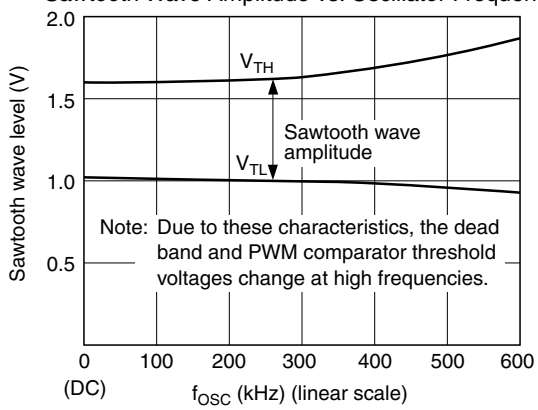


- Triangle Wave Oscillator Block

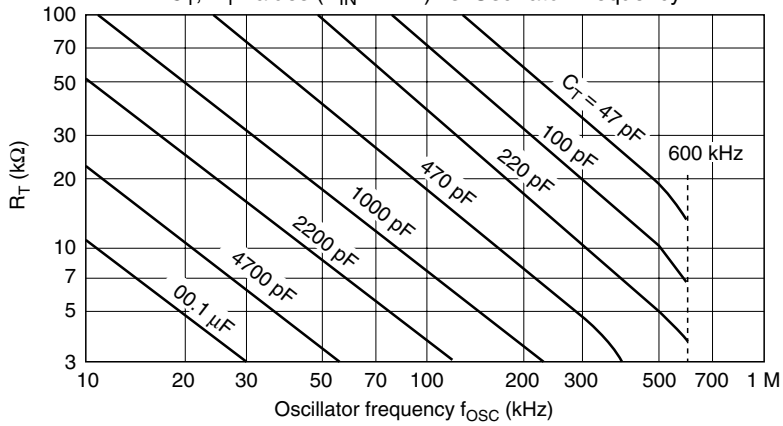
R_T pin Output Current Characteristics



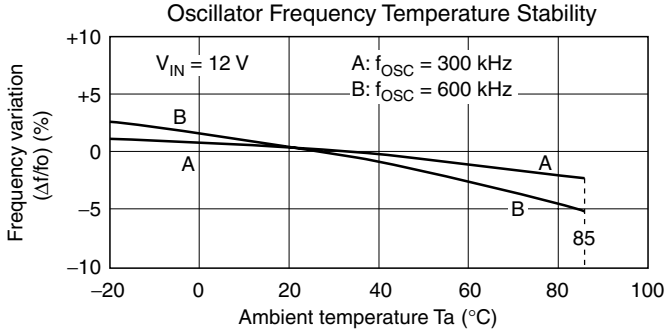
Sawtooth Wave Amplitude vs. Oscillator Frequency



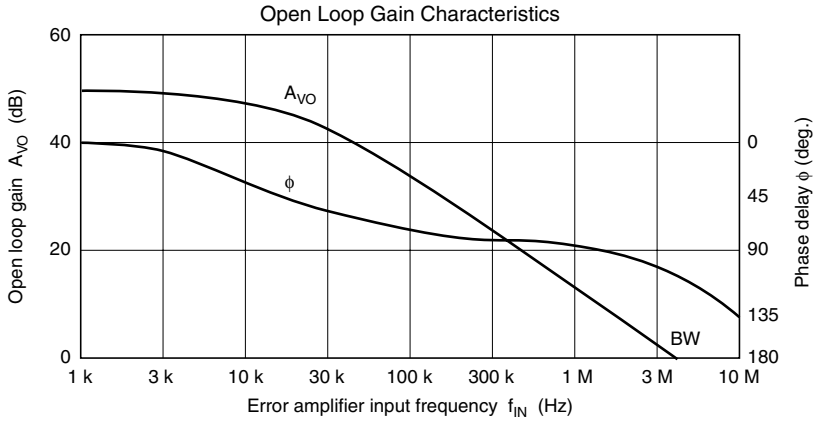
C_T, R_T Values (V_{IN} = 12V) vs. Oscillator Frequency

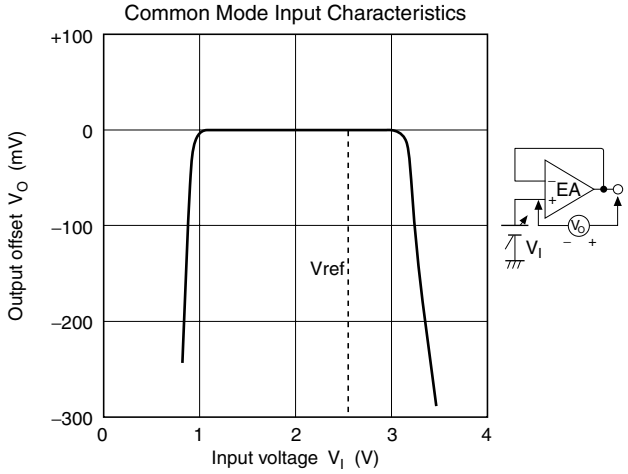


Oscillator Frequency Temperature Stability

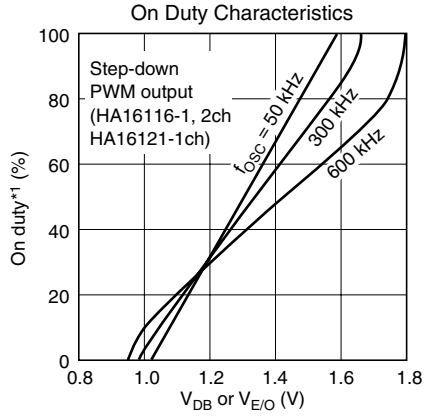


- Error Amplifier Block

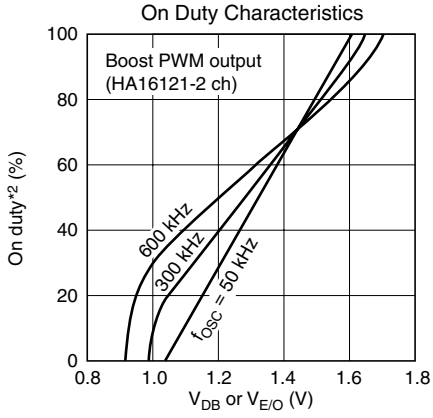




- On Duty Characteristics



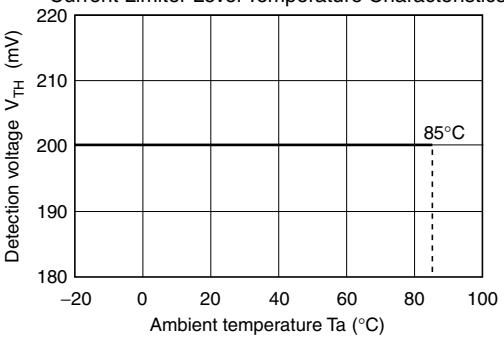
Notes: 1. The percentage of a single timing cycle during which the output is low.



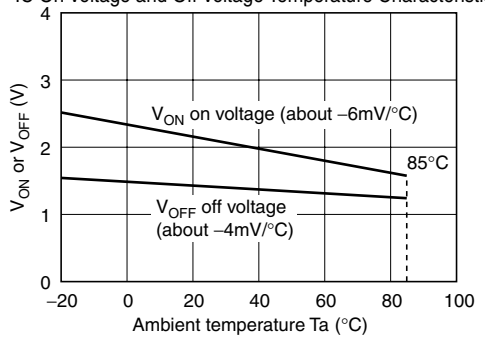
2. The percentage of a single timing cycle during which the output is high.

- Other Characteristics

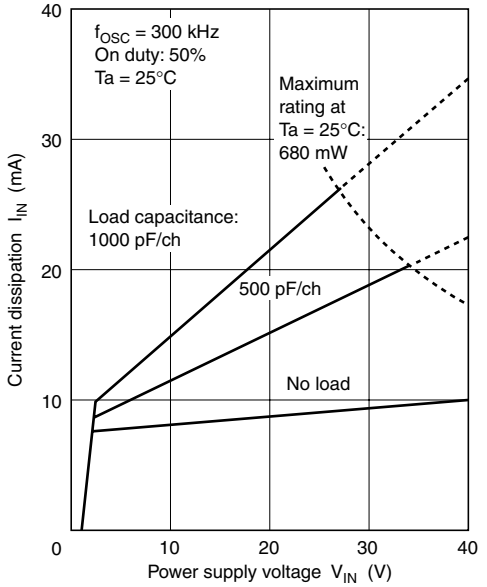
Current Limiter Level Temperature Characteristics



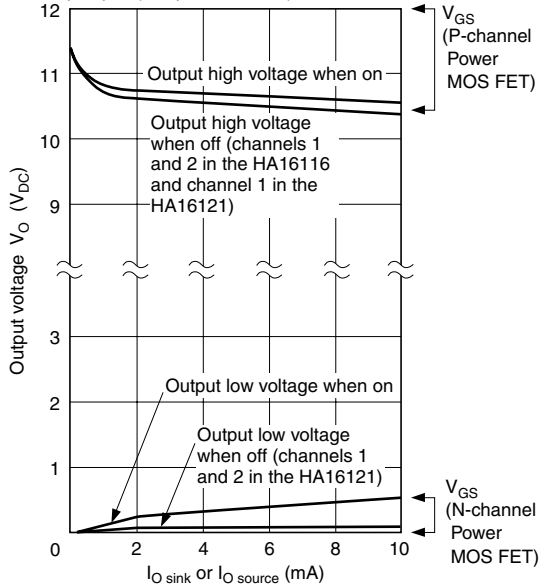
IC On Voltage and Off Voltage Temperature Characteristics



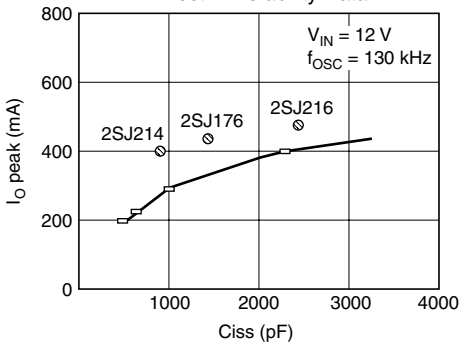
I_{IN} vs. V_{IN} Characteristics



Output pin (Output Resistor) Characteristics

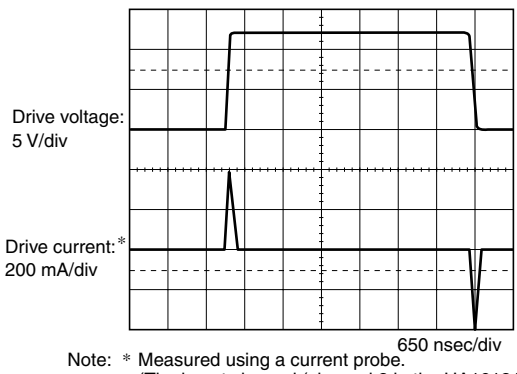


Output Drive Circuit Power MOS FET
Direct Drive ability Data



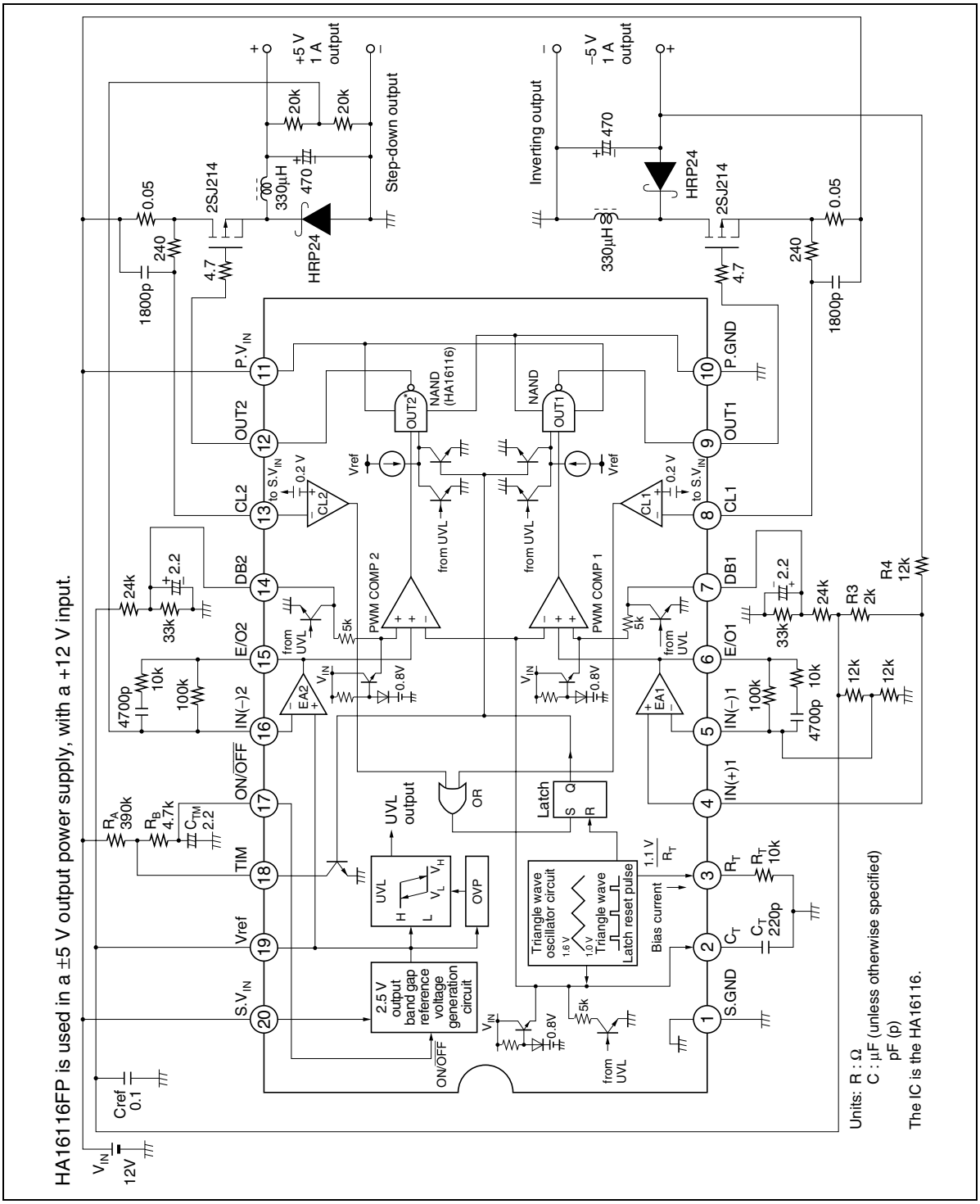
Note: The solid line is data measured with discrete capacitances (for each channel of HA16116).

Gate Drive Waveforms for the 2SJ214

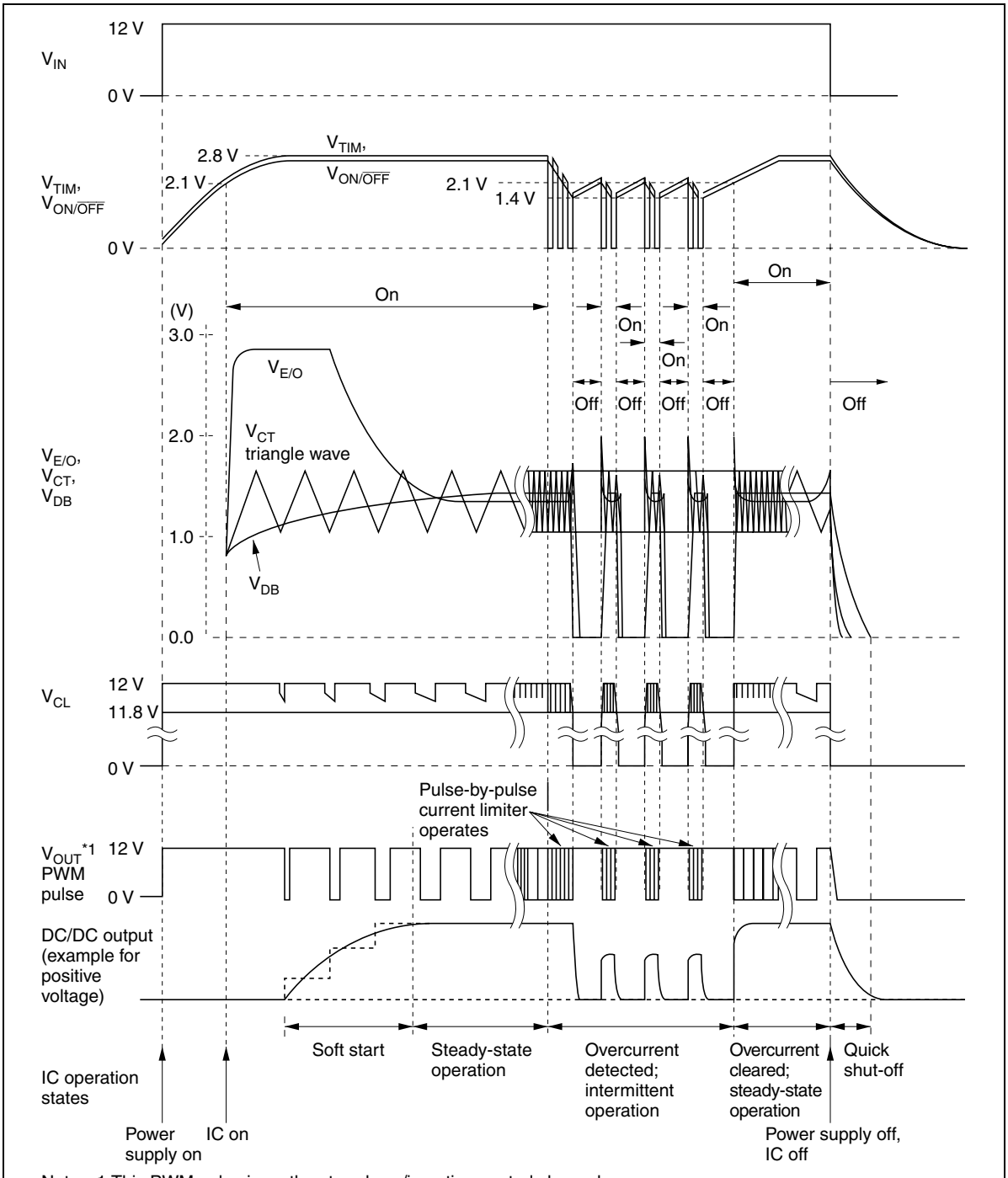


Note: * Measured using a current probe.
(The boost channel (channel 2 in the HA16121) load is with respect to ground, and has almost identical characteristics.)

Application Examples (1)



Overall Waveform Timing Diagram (for Application Examples (1))

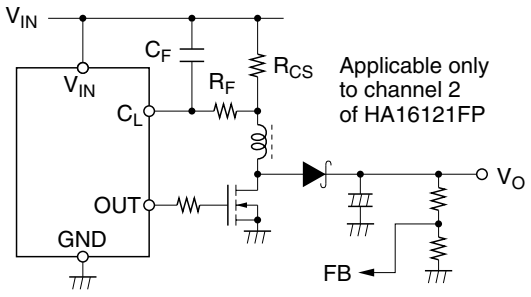


Note: 1.This PWM pulse is on the step-down/inverting control channel.
The booster control channel output consists of alternating L and H of the IC ÒonÓ cycle.

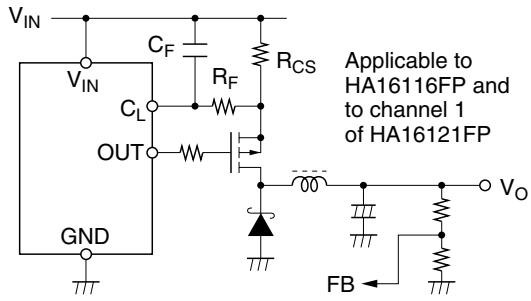
Application Examples (2) (Some Pointers on Use)

1. Inductor, Power MOS FET, and Diode Connections

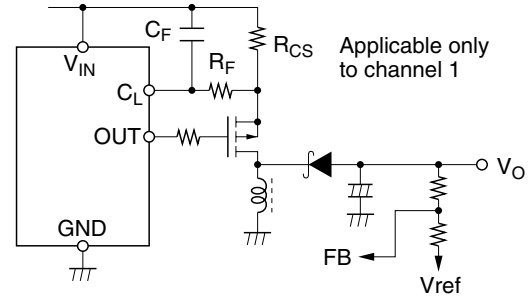
1. Booster specification



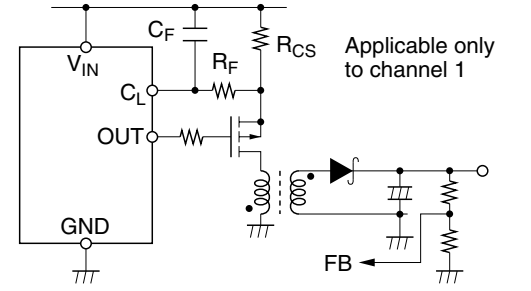
2. Step-down specification



3. Inverting specification

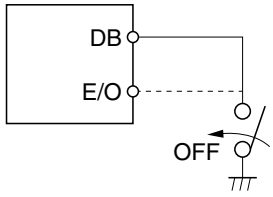


4. Negative booster specification (Flyback transformer)



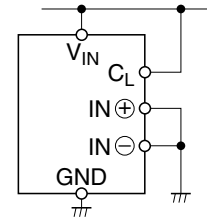
2. Turning Output On and Off while the IC is On

1. To turn only one channel off, ground the DB pin or the E/O pin. In the case of E/O, however, there will be no soft start when the output is turned back on.

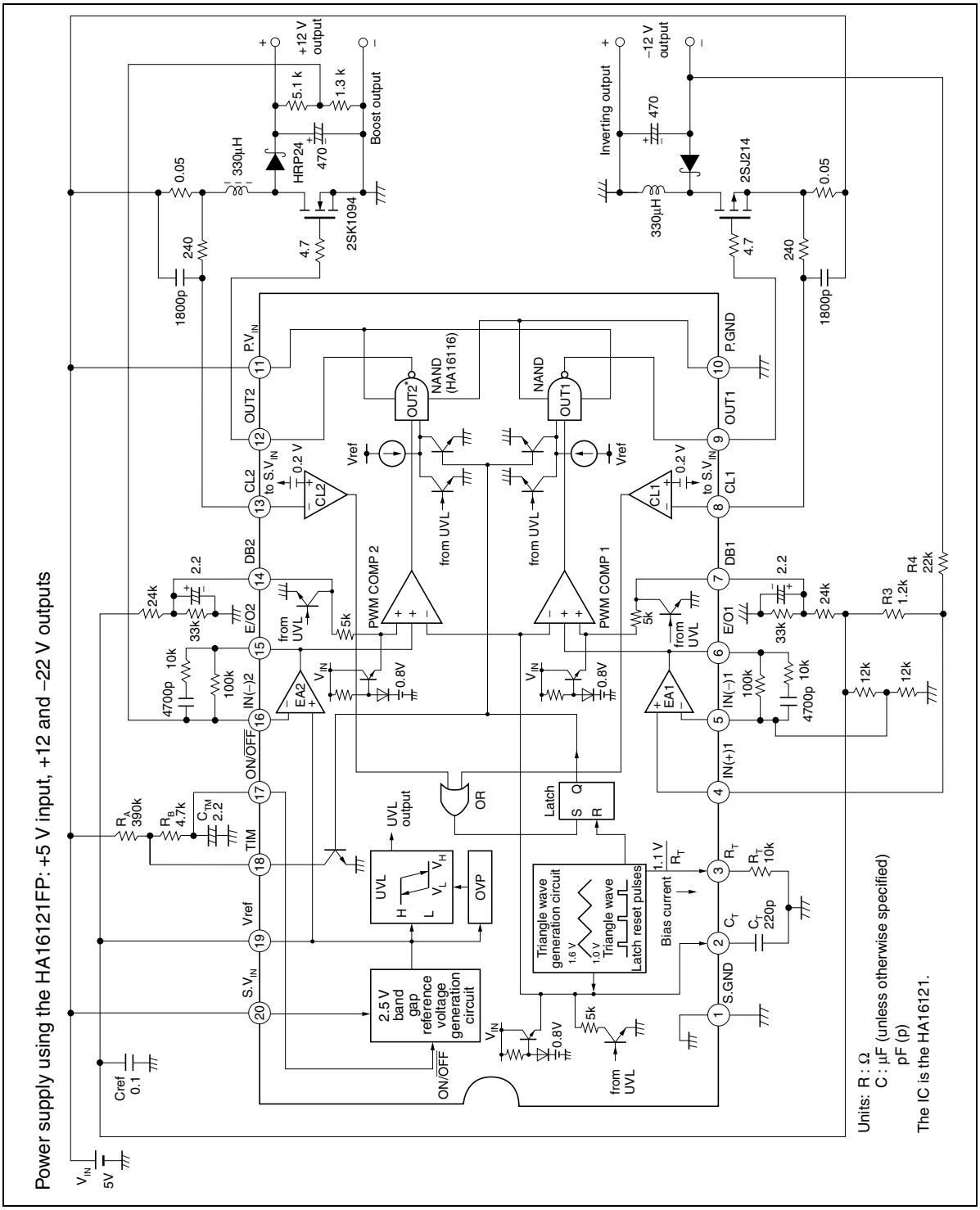


2. When only one channel is to be used, the channel not used should be connected as follows.

Connect C_L to V_{IN}.
Ground IN(+) and IN(–).
Leave other pins open.



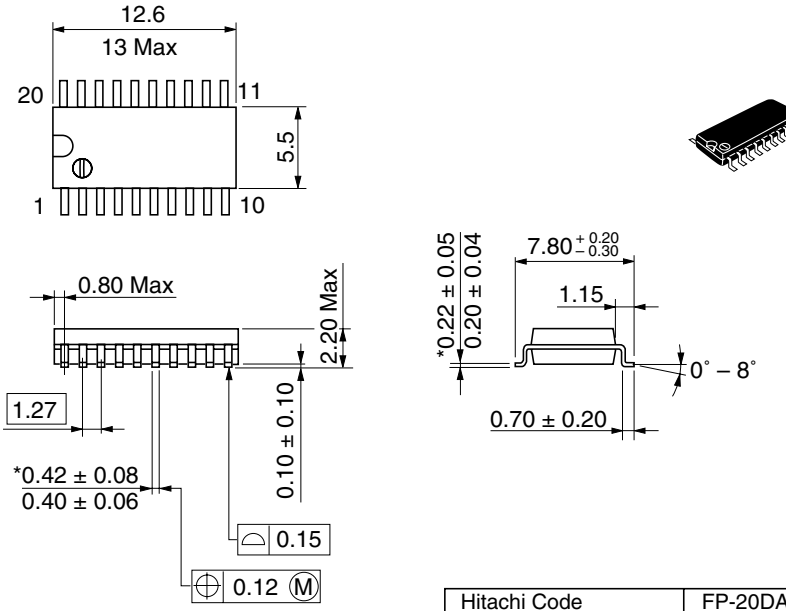
Application Examples (3)



Package Dimensions

As of January, 2002

Unit: mm



*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-20DA
JEDEC	—
JEITA	Conforms
Mass (reference value)	0.31 g

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