512Kx32 SRAM MODULE, SMD 5962-94611

FEATURES

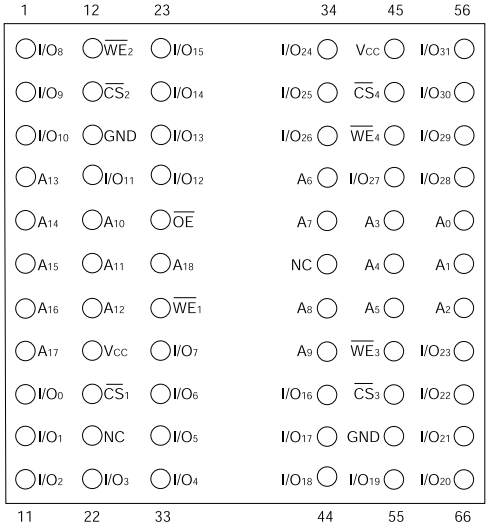
- Access Times of 15*, 17, 20, 25, 35, 45, 55ns
- Packaging
  - 66 pin, PGA Type, 1.075" square, Hermetic Ceramic HIP (Package 400).
  - 68 lead, 40mm Hermetic Low Profile CQFP, 3.5mm (0.140") (Package 502)[1], Package to be developed.
  - 68 lead, Hermetic CQFP (G2T)[1], 22.4mm (0.880") square (Package 509) 4.57mm (0.180") height. Designed to fit JEDEC 68 lead 0.990" CQFJ footprint (Fig. 3).
  - 68 lead, Hermetic CQFP (G1U), 23.9mm (0.940") square (Package 519) 3.57mm (0.140") height. Designed to fit JEDEC 68 lead 0.990" CQFJ footprint (Fig. 3).
  - 68 lead, Hermetic CQFP (G1U), 23.9mm (0.940") square (Package 524) 4.06mm (0.160") height.
- Organized as 512Kx32, User Configurable as 1Mx16 or 2Mx8
- Commercial, Industrial and Military Temperature Ranges
- TTL Compatible Inputs and Outputs
- 5 Volt Power Supply
- Low Power CMOS
- Built-in Decoupling Caps and Multiple Ground Pins for Low Noise Operation
- Weight
  WS512K32-XH1X - 13 grams typical
  WS512K32-XG2TX[1] - 8 grams typical
  WS512K32-XG1UX - 5 grams typical
  WS512K32-XG1TX - 5 grams typical
  WS512K32-XG4TX[1] - 20 grams typical

** 15ns Access Time available only in Commercial and Industrial Temperature. This speed is not fully characterized and is subject to change without notice.*

Note 1: Package Not Recommended For New Design

FIG. 1 PIN CONFIGURATION FOR WS512K32N-XH1X

TOP VIEW



PIN DESCRIPTION

I/O_{0-31}	Data Inputs/Outputs
A_{0-18}	Address Inputs
$\overline{WE}_{1-4}$	Write Enables
$\overline{CS}_{1-4}$	Chip Selects
$\overline{OE}$	Output Enable
V_{CC}	Power Supply
GND	Ground
NC	Not Connected

BLOCK DIAGRAM

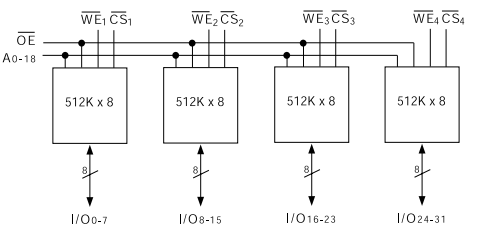
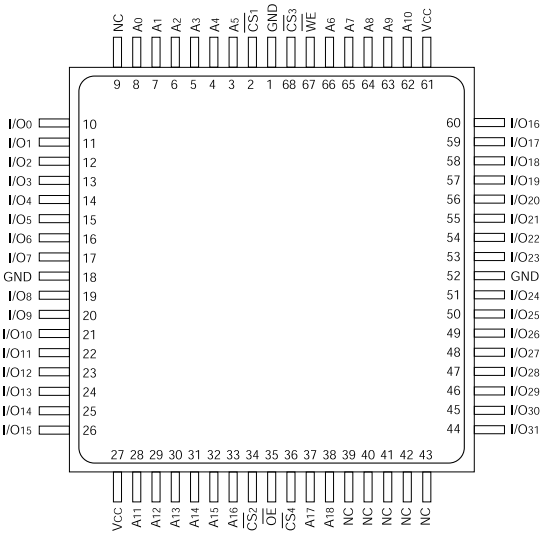


FIG. 2 PIN CONFIGURATION FOR WS512K32-XG4TX[1]

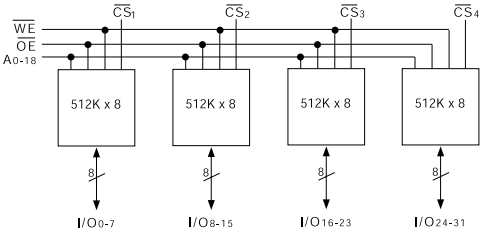
TOP VIEW



PIN DESCRIPTION

I/O0-31	Data Inputs/Outputs
A0-18	Address Inputs
$\overline{WE}$	Write Enables
$\overline{CS}$1-4	Chip Selects
$\overline{OE}$	Output Enable
VCC	Power Supply
GND	Ground
NC	Not Connected

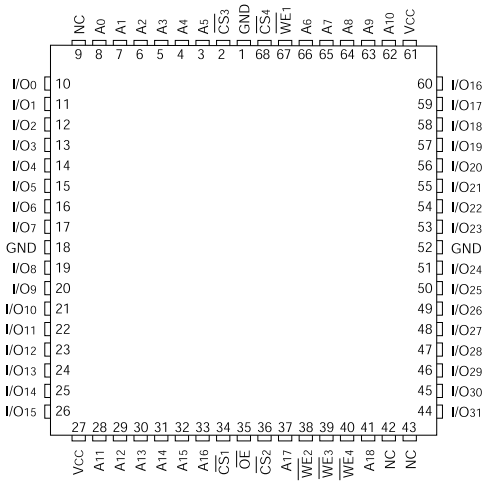
BLOCK DIAGRAM

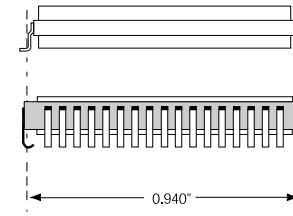


Note 1: Package Not Recommended For New Design

FIG. 3 PIN CONFIGURATION FOR WS512K32-XG2TX[1], WS512K32-XG1TX AND WS512K32-XG1UX

TOP VIEW



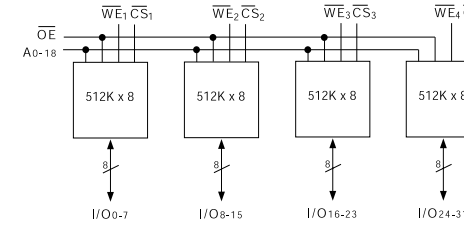


The White 68 lead CQFP fills the same fit and function as the JEDEC 68 lead CQFJ or 68 PLCC. But the CQFJ has the TCE and lead inspection advantage of the CQFP form.

PIN DESCRIPTION

I/O0-31	Data Inputs/Outputs
A0-18	Address Inputs
$\overline{WE}$1-4	Write Enables
$\overline{CS}$1-4	Chip Selects
$\overline{OE}$	Output Enable
VCC	Power Supply
GND	Ground
NC	Not Connected

BLOCK DIAGRAM



Note 1: Package Not Recommended For New Design

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T_A	-55	+125	°C
Storage Temperature	T_{STG}	-65	+150	°C
Signal Voltage Relative to GND	V_G	-0.5	Vcc+0.5	V
Junction Temperature	T_J		150	°C
Supply Voltage	V_{CC}	-0.5	7.0	V

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	4.5	5.5	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	-0.5	+0.8	V
Operating Temp (Mil)	T_A	-55	+125	°C

TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	Data I/O	Power
H	X	X	Standby	High Z	Standby
L	L	H	Read	Data Out	Active
L	H	H	Out Disable	High Z	Active
L	X	L	Write	Data In	Active

CAPACITANCE

(T_A = +25°C)

Parameter	Symbol	Conditions	Max	Unit
$\overline{OE}$ capacitance	C_{OE}	V_{IN} = 0 V, f = 1.0 MHz	50	pF
$\overline{WE}_{1\text{-}4}$ capacitance	C_{WE}	V_{IN} = 0 V, f = 1.0 MHz		pF
HIP (PGA)			20	
CQFP G4T			50	
CQFP G2T/G1U/G1T			20	
$\overline{CS}_{1\text{-}4}$ capacitance	C_{CS}	V_{IN} = 0 V, f = 1.0 MHz	20	pF
Data I/O capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V, f = 1.0 MHz	20	pF
Address input capacitance	C_{AD}	V_{IN} = 0 V, f = 1.0 MHz	50	pF

This parameter is guaranteed by design but not tested.

DC CHARACTERISTICS

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Symbol	Conditions	Min	Max	Units
Input Leakage Current	I_{LI}	V_{CC} = 5.5, V_{IN} = GND to V_{CC}		10	µA
Output Leakage Current	I_{LO}	$\overline{CS}$ = V_{IH}, $\overline{OE}$ = V_{IH}, V_{OUT} = GND to V_{CC}		10	µA
Operating Supply Current x 32 Mode	$I_{CC \times 32}$	$\overline{CS}$ = V_{IL}, $\overline{OE}$ = V_{IH}, f = 5MHz, Vcc = 5.5		660	mA
Standby Current	I_{SB}	$\overline{CS}$ = V_{IH}, $\overline{OE}$ = V_{IH}, f = 5MHz, Vcc = 5.5		80	mA
Output Low Voltage	V_{OL}	I_{OL} = 8mA for 15 - 35ns, I_{OL} = 2.1mA for 45 - 55ns, Vcc = 4.5		0.4	V
Output High Voltage	V_{OH}	I_{OH} = -4.0mA for 15 - 35ns, I_{OH} = -1.0mA for 45 - 55ns, Vcc = 4.5	2.4		V

NOTE: DC test conditions: V_{IH} = V_{CC} -0.3V, V_{IL} = 0.3V

DATA RETENTION CHARACTERISTICS

(T_A = -55°C to +125°C)

Parameter	Symbol	Conditions	Min	Max	Units
Data Retention Supply Voltage	V_{DR}	$\overline{CS} \geq V_{CC}$ -0.2V	2.0	5.5	V
Data Retention Current	I_{CCDR1}	V_{CC} = 3V		28	mA
Low Power Data Retention Current (WS512K32L-XXX)	I_{CCDR2}	V_{CC} = 3V		16	mA

AC CHARACTERISTICS
(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Symbol	-15*		-17		-20		-25		-35		-45		-55		Units
Read Cycle		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	15		17		20		25		35		45		55		ns
Address Access Time	t_{AA}		15		17		20		25		35		45		55	ns
Output Hold from Address Change	t_{OH}	0		0		0		0		0		0		0		ns
Chip Select Access Time	t_{ACS}		15		17		20		25		35		45		55	ns
Output Enable to Output Valid	t_{OE}		8		9		10		12		25		25		25	ns
Chip Select to Output in Low Z	t_{CLZ}[1]	2		2		2		2		4		4		4		ns
Output Enable to Output in Low Z	t_{OLZ}[1]	0		0		0		0		0		0		0		ns
Chip Disable to Output in High Z	t_{CHZ}[1]		12		12		12		12		15		20		20	ns
Output Disable to Output in High Z	t_{OHZ}[1]		12		12		12		12		15		20		20	ns

* 15ns Access Time available only in Commercial and Industrial Temperature. This speed is not fully characterized and is subject to change without notice.

1. This parameter is guaranteed by design but not tested.

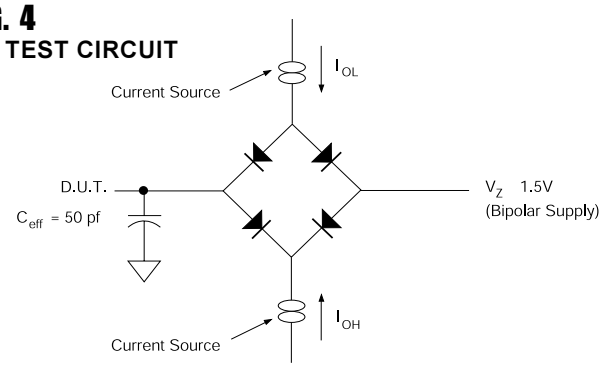
AC CHARACTERISTICS
(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Symbol	-15*		-17		-20		-25		-35		-45		-55		Units
Write Cycle		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	15		17		20		25		35		45		55		ns
Chip Select to End of Write	t_{CW}	13		15		15		17		25		35		50		ns
Address Valid to End of Write	t_{AW}	13		15		15		17		25		35		50		ns
Data Valid to End of Write	t_{DW}	10		11		12		13		20		25		25		ns
Write Pulse Width	t_{WP}	13		15		15		17		25		35		40		ns
Address Setup Time	t_{AS}	2		2		2		2		2		2		2		ns
Address Hold Time	t_{AH}	0		0		0		0		0		5		5		ns
Output Active from End of Write	t_{OW}[1]	2		2		3		4		4		5		5		ns
Write Enable to Output in High Z	t_{WHZ}[1]		8		9		11		13		15		20		20	ns
Data Hold Time	t_{DH}	0		0		0		0		0		0		0		ns

* 15ns Access Time available only in Commercial and Industrial Temperature. This speed is not fully characterized and is subject to change without notice.

1. This parameter is guaranteed by design but not tested.
2. The Address Setup Time of minimum 2ns is for the G2T, G1U and H1 packages. t_{AS} minimum for the G4T package is 0ns.

FIG. 4
AC TEST CIRCUIT

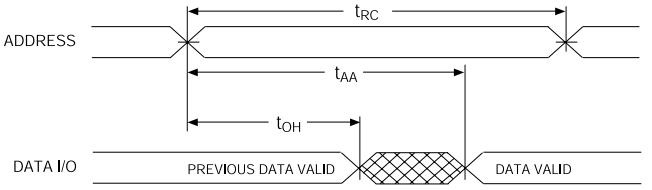


AC TEST CONDITIONS

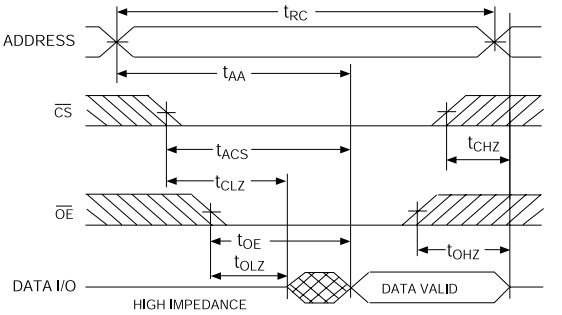
Parameter	Typ	Unit
Input Pulse Levels	V_{IL} = 0, V_{IH} = 3.0	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

NOTES:
V_Z is programmable from -2V to +7V.
I_{OL} & I_{OH} programmable from 0 to 16mA.
Tester Impedance Z_0 = 75 ý.
V_Z is typically the midpoint of V_{OH} and V_{OL}.
I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.
ATE tester includes jig capacitance.

FIG. 5
TIMING WAVEFORM - READ CYCLE

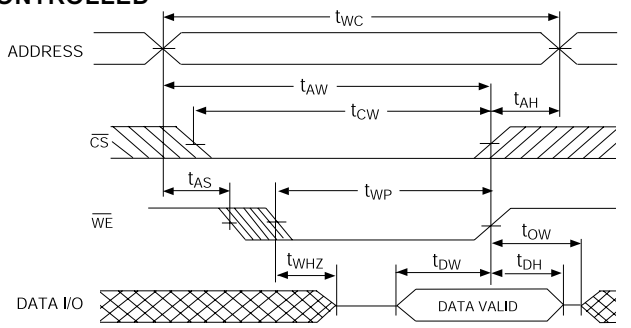


READ CYCLE 1 ($\overline{CS}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH})



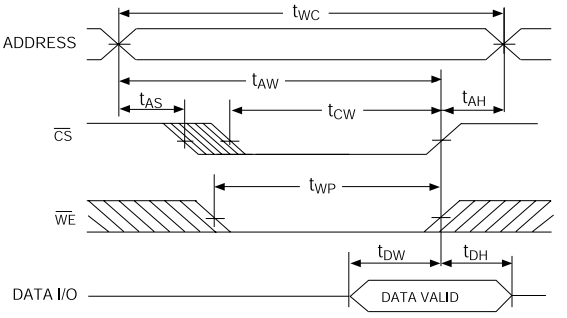
READ CYCLE 2 ($\overline{WE}$ = V_{IH})

FIG. 6
WRITE CYCLE - $\overline{WE}$ CONTROLLED



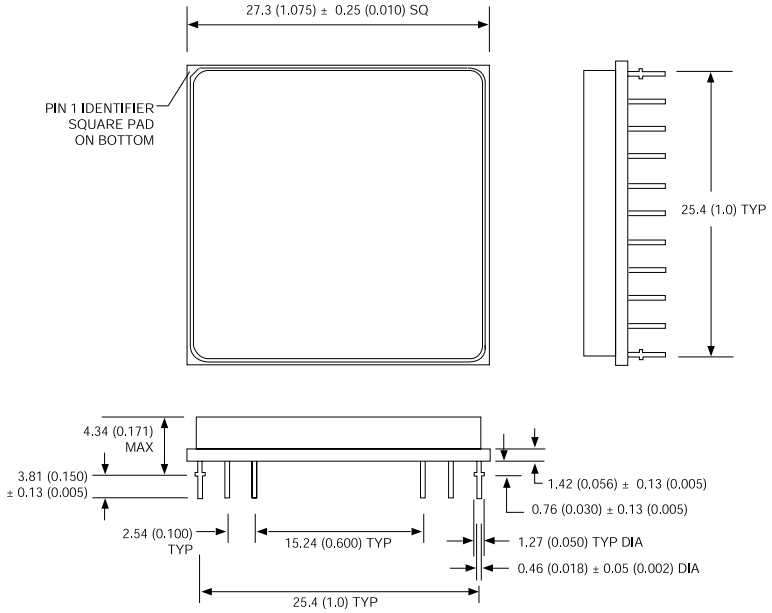
WRITE CYCLE 1, $\overline{WE}$ CONTROLLED

FIG. 7
WRITE CYCLE - $\overline{CS}$ CONTROLLED



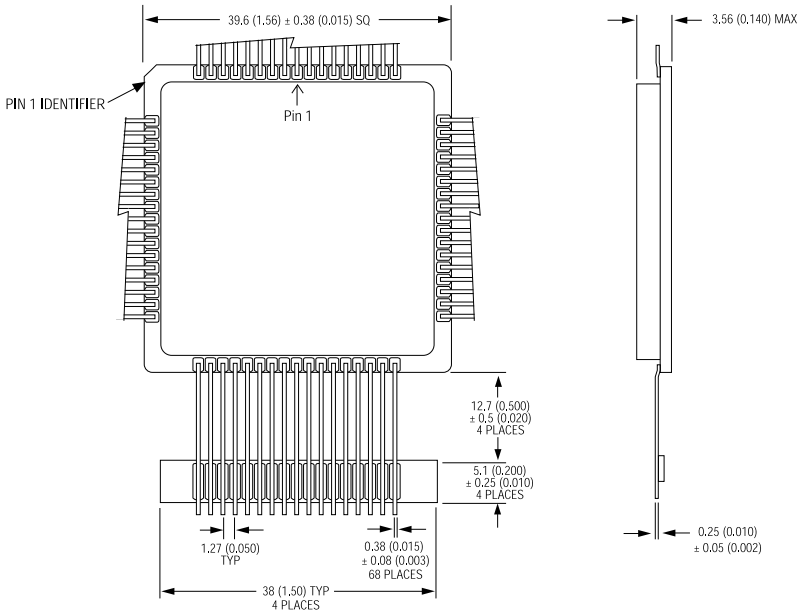
WRITE CYCLE 2, $\overline{CS}$ CONTROLLED

PACKAGE 400: 66 PIN, PGA TYPE, CERAMIC HEX-IN-LINE PACKAGE, HIP (H1)



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

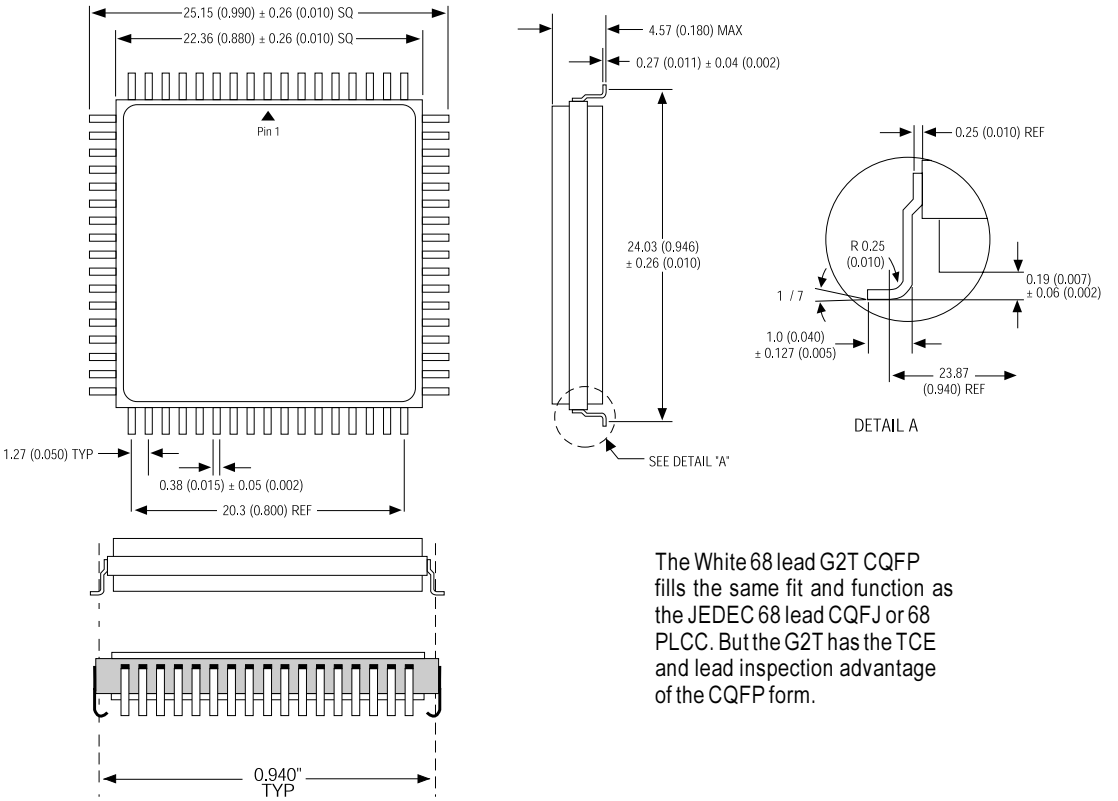
PACKAGE 502: 68 LEAD, CERAMIC QUAD FLAT PACK, LOW PROFILE CQFP (G4T)[1]



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

Note 1: Package Not Recommended For New Design

PACKAGE 509: 68 LEAD, CERAMIC QUAD FLAT PACK, CQFP (G2T)[1]

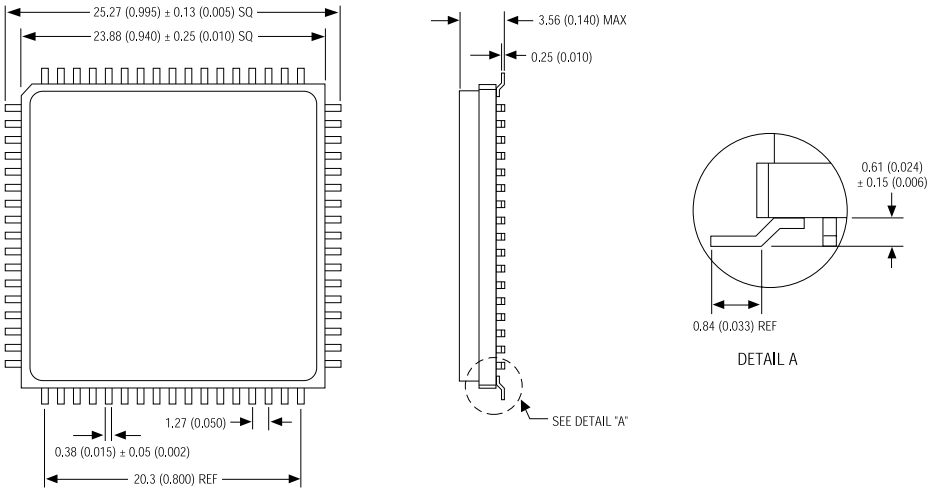


The White 68 lead G2T CQFP fills the same fit and function as the JEDEC 68 lead CQFJ or 68 PLCC. But the G2T has the TCE and lead inspection advantage of the CQFP form.

ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

Note 1: Package Not Recommended For New Design

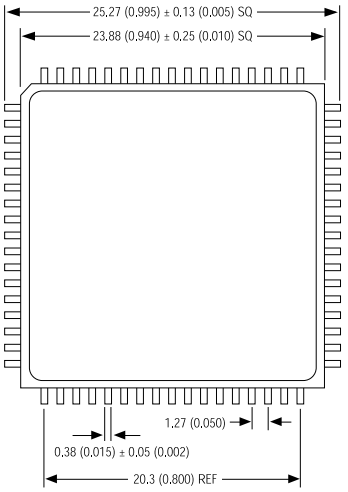
PACKAGE 519: 68 LEAD, CERAMIC QUAD FLAT PACK, LOW PROFILE CQFP (G1U)

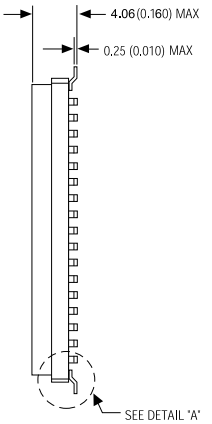


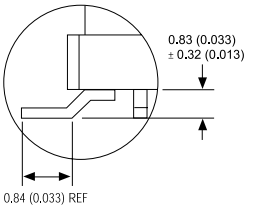
The White 68 lead G1U CQFP fills the same fit and function as the JEDEC 68 lead CQFJ or 68 PLCC. But the G1U has the TCE and lead inspection advantage of the CQFP form.

ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

PACKAGE 524: 68 LEAD, CERAMIC QUAD FLAT PACK, LOW PROFILE CQFP (G1T)



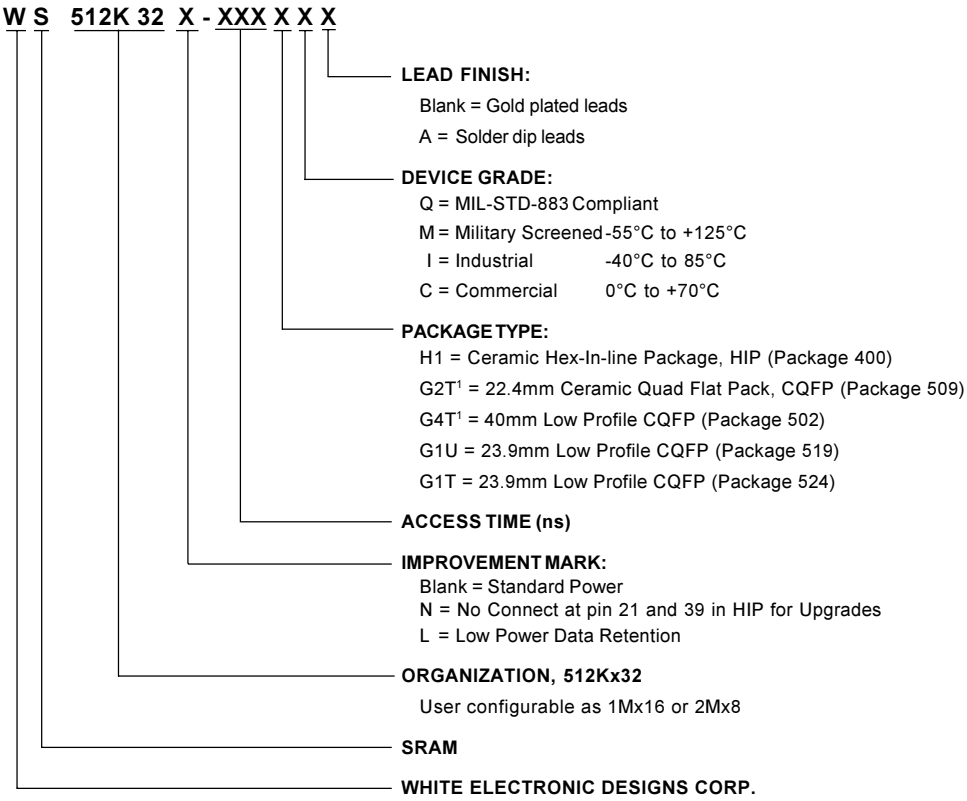




The White 68 lead G1T CQFP fills the same fit and function as the JEDEC 68 lead CQFJ or 68 PLCC. But the G1T has the TCE and lead inspection advantage of the CQFP form.

ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

ORDERING INFORMATION



Note 1: Package Not Recommended For New Design

DEVICE TYPE	SPEED	PACKAGE	SMD NO.
512K x 32 SRAM Module	55ns	66 pin HIP (H1)	5962-94611 05HTX
512K x 32 SRAM Module	45ns	66 pin HIP (H1)	5962-94611 06HTX
512K x 32 SRAM Module	35ns	66 pin HIP (H1)	5962-94611 07HTX
512K x 32 SRAM Module	25ns	66 pin HIP (H1)	5962-94611 08HTX
512K x 32 SRAM Module	20ns	66 pin HIP (H1)	5962-94611 09HTX
512K x 32 SRAM Module	17ns	66 pin HIP (H1)	5962-94611 10HTX
512K x 32 SRAM Module	55ns	68 lead CQFP Low Profile (G4T)[1]	5962-94611 05HYX
512K x 32 SRAM Module	45ns	68 lead CQFP Low Profile (G4T)[1]	5962-94611 06HYX
512K x 32 SRAM Module	35ns	68 lead CQFP Low Profile (G4T)[1]	5962-94611 07HYX
512K x 32 SRAM Module	25ns	68 lead CQFP Low Profile (G4T)[1]	5962-94611 08HYX
512K x 32 SRAM Module	20ns	68 lead CQFP Low Profile (G4T)[1]	5962-94611 09HYX
512K x 32 SRAM Module	17ns	68 lead CQFP Low Profile (G4T)[1]	5962-94611 10HYX
512K x 32 SRAM Module	55ns	68 lead CQFP (G2T)[1]	5962-94611 05HMX
512K x 32 SRAM Module	45ns	68 lead CQFP (G2T)[1]	5962-94611 06HMX
512K x 32 SRAM Module	35ns	68 lead CQFP (G2T)[1]	5962-94611 07HMX
512K x 32 SRAM Module	25ns	68 lead CQFP (G2T)[1]	5962-94611 08HMX
512K x 32 SRAM Module	20ns	68 lead CQFP (G2T)[1]	5962-94611 09HMX
512K x 32 SRAM Module	17ns	68 lead CQFP (G2T)[1]	5962-94611 10HMX
512K x 32 SRAM Module	55ns	68 lead CQFP (G1U)	5962-94611 05H9X
512K x 32 SRAM Module	45ns	68 lead CQFP (G1U)	5962-94611 06H9X
512K x 32 SRAM Module	35ns	68 lead CQFP (G1U)	5962-94611 07H9X
512K x 32 SRAM Module	25ns	68 lead CQFP (G1U)	5962-94611 08H9X
512K x 32 SRAM Module	20ns	68 lead CQFP (G1U)	5962-94611 09H9X
512K x 32 SRAM Module	17ns	68 lead CQFP (G1U)	5962-94611 10H9X

Note 1: Package Not Recommended For New Design