NEC

MOS INTEGRATED CIRCUIT

μPD16772A

480-OUTPUT TFT-LCD SOURCE DRIVER (COMPATIBLE WITH 64-GRAY SCALES)

DESCRIPTION

The μPD16772A is a source driver for TFT-LCDs capable of dealing with displays with 64-gray scales. Data input is based on digital input configured as 6 bits by 6 dots (2 pixels), which can realize a full-color display of 260,000 colors by output of 64 values γ-corrected by an internal D/A converter and 5-by-2 external power modules. Because the output dynamic range is as large as V_{SS2} + 0.1 V to V_{DD2} – 0.1 V, level inversion operation of the LCD's common electrode is rendered unnecessary. Also, to be able to deal with dot-line inversion, n-line inversion and column line inversion when mounted on a single side, this source driver is equipped with a built-in 6-bit D/A converter circuit whose odd output pins and even output pins respectively output gray scale voltages of differing polarity. Assuring a clock frequency of 45 MHz when driving at 2.3 V, this driver is applicable to UXGA-standard TFT-LCD panels.

FEATURES

- CMOS level input (2.3 to 3.6 V)
- 480 outputs
- Input of 6 bits (gradation data) by 6 dots
- Capable of outputting 64 values by means of 5-by-2 external power modules (10 units) and a D/A converter (R-DAC)
- Output dynamic range : V_{SS2} + 0.1 V to V_{DD2} – 0.1 V
- High-speed data transfer : f_{CLK} = 45 MHz (internal data transfer speed when operating at V_{DD1} = 2.3 V)
- Apply for dot-line inversion, n-line inversion and column line inversion
- Output voltage polarity inversion function (POL)
- Display data inversion function (POL21/22)
- Current consumption reduction function (LPC, Bcont)
- Logic power supply voltage (V_{DD1}) : 2.3 to 3.6 V
- Driver power supply voltage (V_{DD2}) : 8.5 V ± 0.5 V

ORDERING INFORMATION

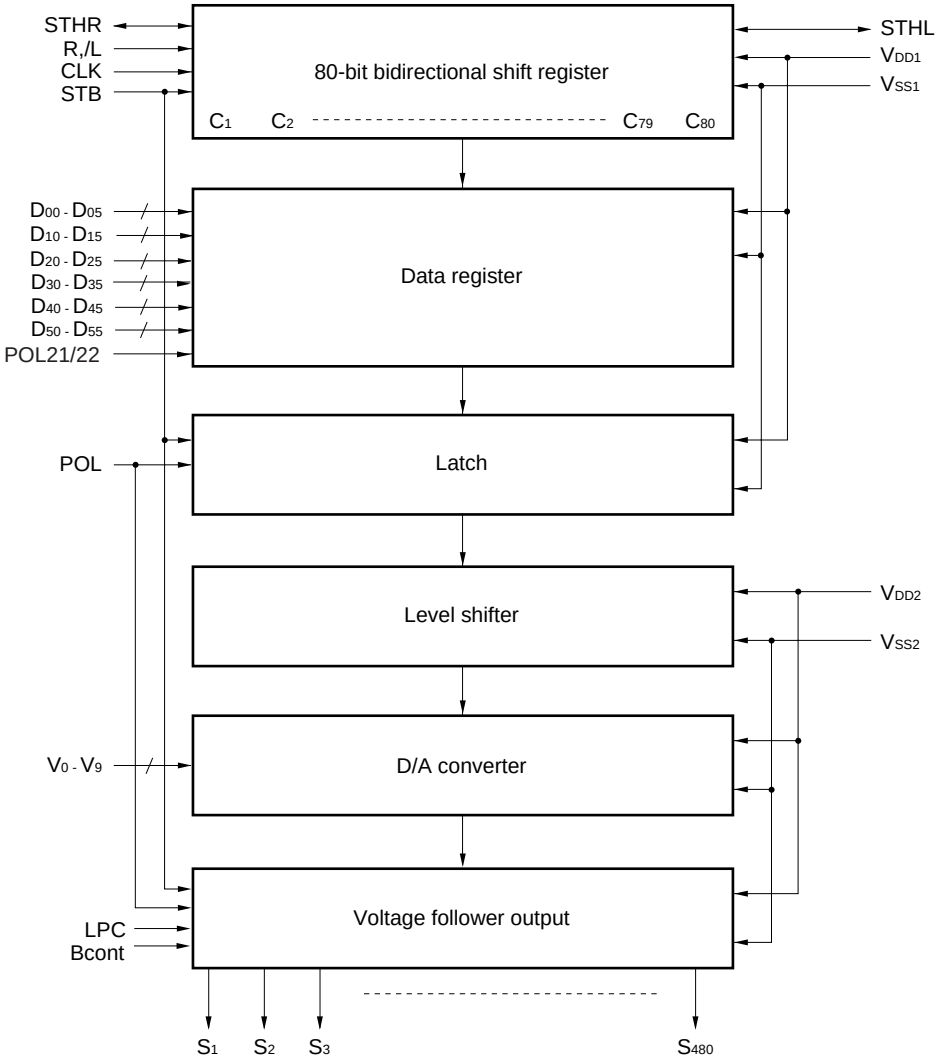
Part Number	Package
μPD16772AN-xxx	TCP (TAB package)

Remark The TCP's external shape is customized. To order the required shape, so please contact one of our sales representatives.

Document No. S14725EJ1V0DS00 (1st edition)
Date Published August 2000 NS CP (K)
Printed in Japan

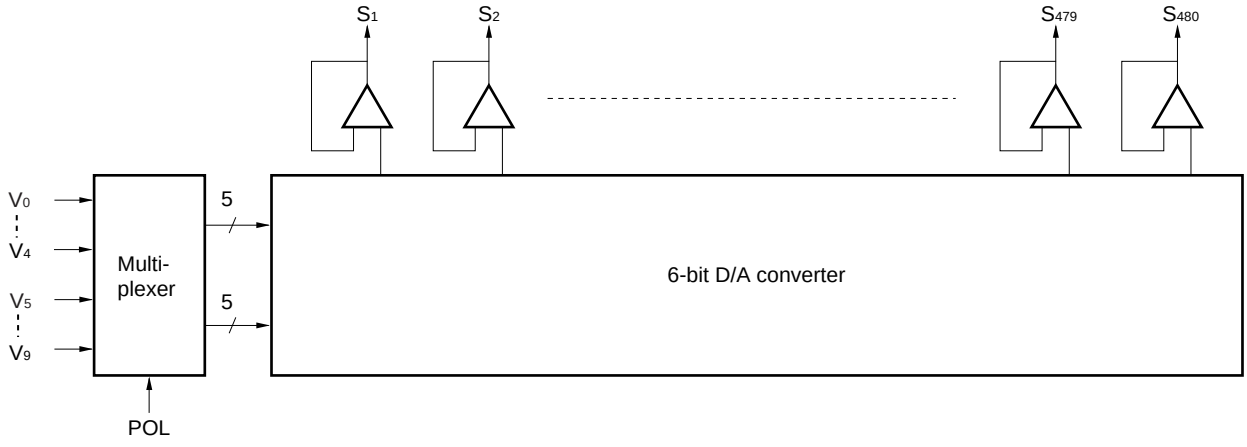
The mark ★ shows major revised points.

1. BLOCK DIAGRAM

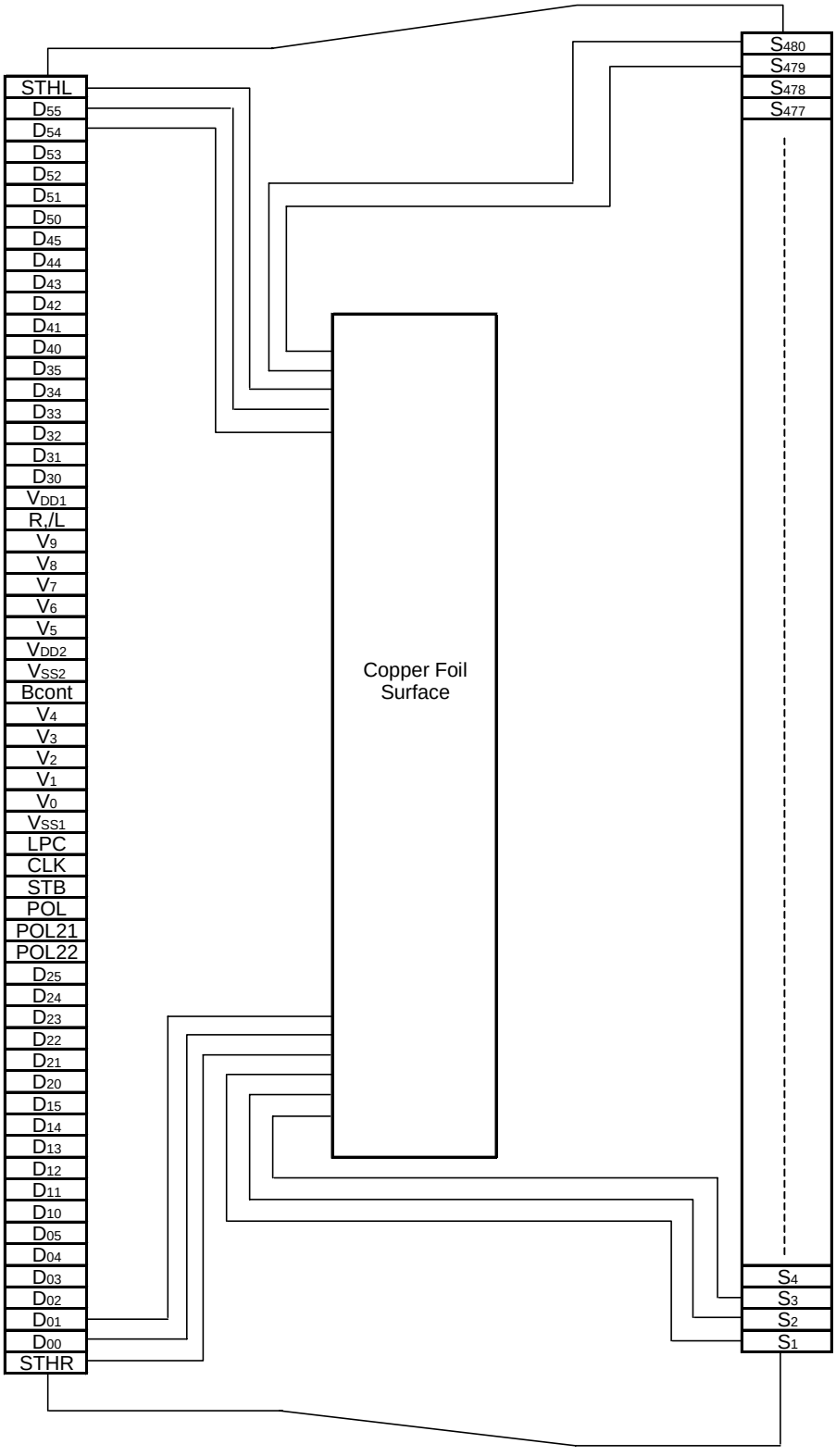


Remark /xxx indicates active low signal.

2. RELATIONSHIP BETWEEN OUTPUT CIRCUIT AND D/A CONVERTER



3. PIN CONFIGURATION (μPD16772AN-xxx: TCP (TAB package))



Remark This figure does not specify the TCP package.

4. PIN FUNCTIONS

Pin Symbol	Pin Name	Description
S_1 to S_{480}	Driver output	The D/A converted 64-gray-scale analog voltage is output.
D_{00} to D_{05}	Display data input	The display data is input with a width of 36 bits, viz., the gray scale data (6 bits) by 6 dots (2 pixels). D_{X0}: LSB, D_{X5}: MSB
D_{10} to D_{15}		
D_{20} to D_{25}		
D_{30} to D_{35}		
D_{40} to D_{45}		
D_{50} to D_{55}		
R,/L	Shift direction control input	These refer to the start pulse I/O pins when driver ICs are connected in cascade. The shift directions of the shift registers are as follows. R,/L = H: STHR input, $S_1 \rightarrow S_{480}$, STHL output R,/L = L: STHL input, $S_{480} \rightarrow S_1$, STHR output
STHR	Right shift start pulse input/output	These refer to the start pulse I/O pins when driver ICs are connected in cascade. Fetching of display data starts when H is read at the rising edge of CLK.
STHL	Left shift start pulse input/output	R,/L = H (right shift): STHR input, STHL output R,/L = L (left shift): STHL input, STHR output The start pulse width (H level) for next-level drivers is 1CLK.
CLK	Shift clock input	Refers to the shift register's shift clock input. The display data is incorporated into the data register at the rising edge. At the rising edge of the 80th clock after the start pulse input, the start pulse output reaches the high level, thus becoming the start pulse of the next-level driver. If 82 clock pulses are input after input of the start pulse, input of display data is halted automatically. The contents of the shift register are cleared at the STB's rising edge.
STB	Latch input	The contents of the data register are transferred to the latch circuit at the rising edge. And, at the falling edge, the gray scale voltage is supplied to the driver. It is necessary to ensure input of one pulse per horizontal period.
POL	Polarity input	POL = L: The S_{2n-1} output uses V_0 to V_4 as the reference supply. The S_{2n} output uses V_5 to V_9 as the reference supply. POL = H: The S_{2n-1} output uses V_5 to V_9 as the reference supply. The S_{2n} output uses V_0 to V_4 as the reference supply. S_{2n-1} indicates the odd output: and S_{2n} indicates the even output. Input of the POL signal is allowed the setup time($t_{POL-STB}$) with respect to STB's rising edge.
POL21, POL22	Data inversion input	Data inversion can invert when display data is loaded. POL21/22 = H : Data inversion loads display data after inverting it. POL21/22 = L : Data inversion does not invert input data. POL21: D_{00} to D_{05}, D_{10} to D_{15}, D_{20} to D_{25} POL22: D_{30} to D_{35}, D_{40} to D_{45}, D_{50} to D_{55}
LPC	Low power control input	The current consumption of V_{DD2} is lowered by controlling the constant current source of the output amplifier. This pin is pulled up to the V_{DD1} power supply inside the IC. For details, see **9. CURRENT CONSUMPTION REDUCTION FUNCTION.**
Bcont	Bias control	This pin can be used to finely control the bias current inside the output amplifier. When this fine-control function is not required, leave this pin open. For details, see **9. CURRENT CONSUMPTION REDUCTION FUNCTION.**
V_0 to V_9	γ-corrected power supplies	Input the γ-corrected power supplies from outside by using operational amplifier. Make sure to maintain the following relationships. During the gray scale voltage output, be sure to keep the gray scale level power supply at a constant level. $V_{DD2} - 0.1\ V > V_0 > V_1 > V_2 > V_3 > V_4 > 0.5\ V_{DD2} > V_5 > V_6 > V_7 > V_8 > V_9 > V_{SS2} + 0.1\ V$
V_{DD1}	Logic power supply	2.3 to 3.6 V
V_{DD2}	Driver power supply	8.5 V ± 0.5 V
V_{SS1}	Logic ground	Grounding
V_{SS2}	Driver ground	Grounding

Cautions 1. The power start sequence must be V_{DD1}, logic input, and V_{DD2} & V_0 to V_9 in that order. Reverse this sequence to shut down (Simultaneous power application to V_{DD2} and V_0 to V_9 is possible.).

2. To stabilize the supply voltage, please be sure to insert a 0.1 μF bypass capacitor between V_{DD1}-V_{SS1} and V_{DD2}-V_{SS2}. Furthermore, for increased precision of the D/A converter, insertion of a bypass capacitor of about 0.01 μF is also advised between the γ-corrected power supply terminals (V_0, V_1, V_2,....., V_9) and V_{SS2}.

5. RELATIONSHIP BETWEEN INPUT DATA AND OUTPUT VOLTAGE VALUE

The μ PD16772A incorporates a 6-bit D/A converter whose odd output pins and even output pins output respectively gray scale voltages of differing polarity with respect to the LCD's counter electrode (common electrode) voltage. The D/A converter consists of ladder resistors and switches.

The ladder resistors (r0 to r62) are designed so that the ratio of LCD panel γ-compensated voltages to V_0' to V_{63}' and V_0" to V_{63}" is almost equivalent. For the 2 sets of five γ-compensated power supplies, V_0 to V_4 and V_5 to V_9, respectively, input gray scale voltages of the same polarity with respect to the common voltage. When fine gray scale voltage precision is not necessary, there is no need to connect a voltage follower circuit to the γ-compensated power supplies V_1 to V_3 and V_6 to V_8.

Figure 5–1 shows the relationship between the driving voltages such as liquid-crystal driving voltages V_{DD2} and V_{SS2}, common electrode potential V_{COM}, and γ-corrected voltages V_0 to V_9 and the input data. Be sure to maintain the voltage relationships of V_{DD2} – 0.1 V > V_0 > V_1 > V_2 > V_3 > V_4 > 0.5 V_{DD2} > V_5 > V_6 > V_7 > V_8 > V_9 > V_{SS2} + 0.1 V

Figures 5–2 and 5–3 show the relationship between the input data and the output voltage and the resistance values of the resistor strings.

Figure 5–1. Relationship between Input Data and γ-corrected Power Supplies

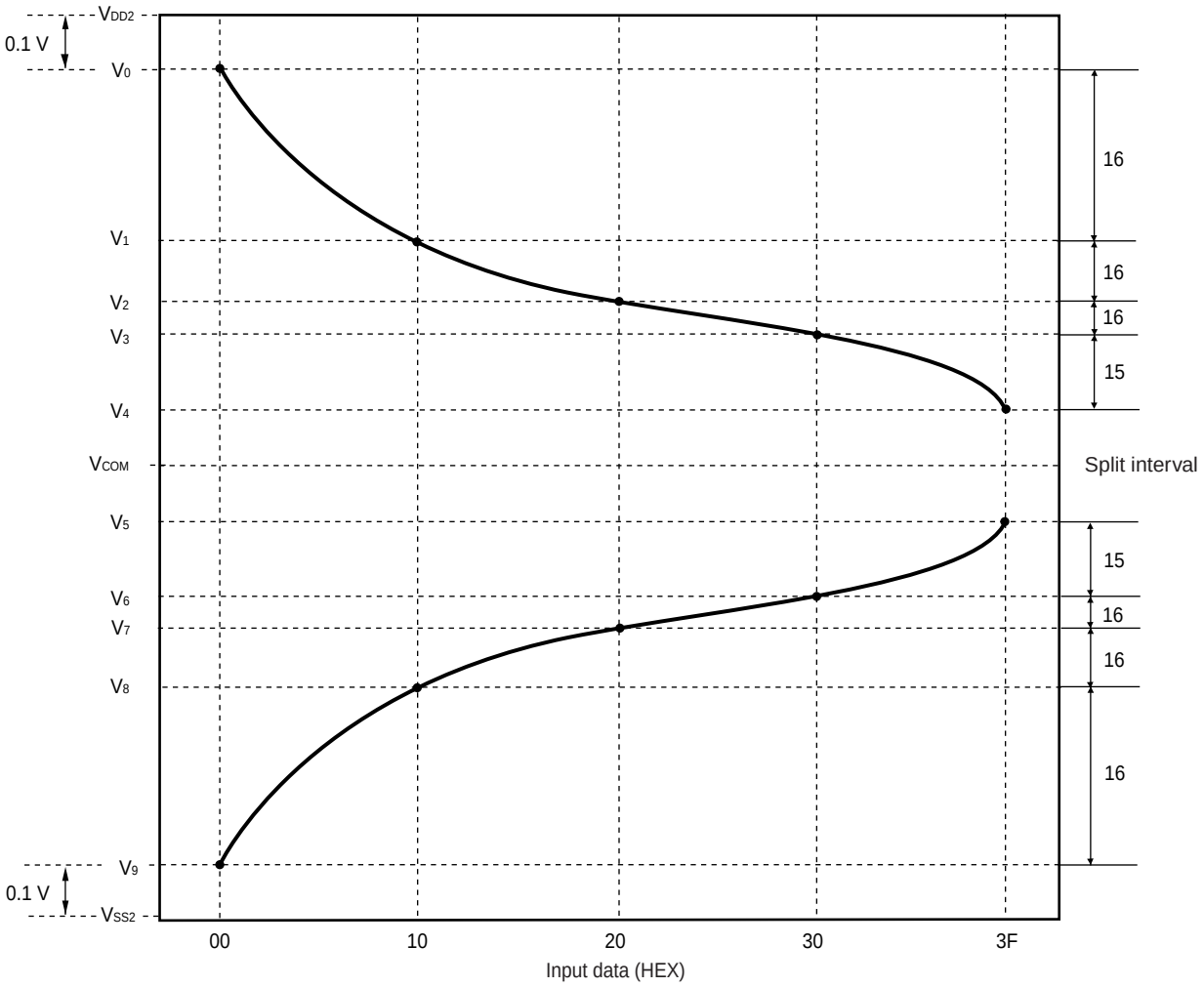
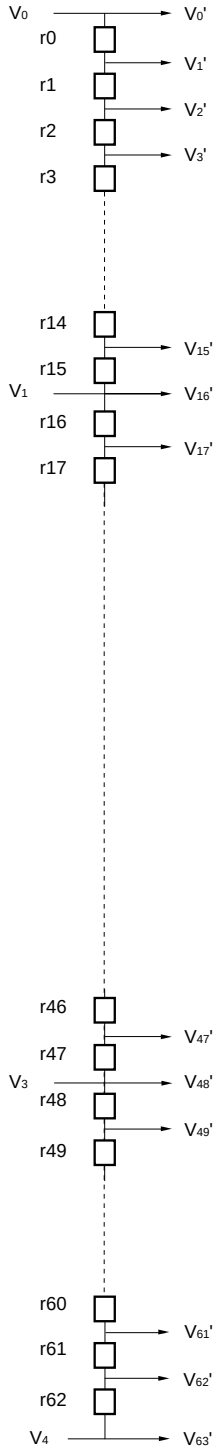


Figure 5–2. Relationship between Input Data and Output Voltage

V_{DD2} – 0.2 V > V_0 > V_1 > V_2 > V_3 > V_4 > 0.5 V_{DD2}, POL21/22 = L

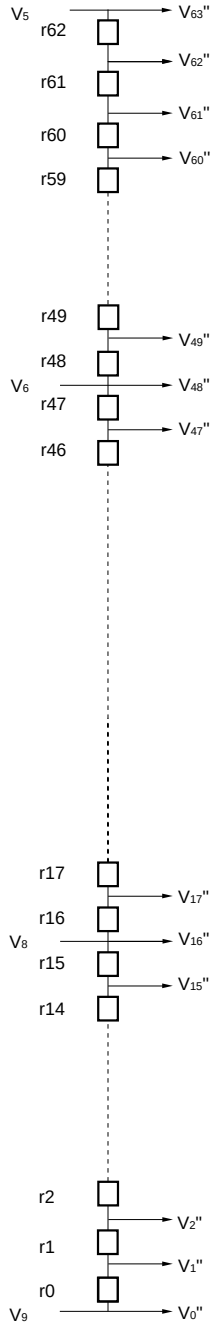


Data	DX5	DX4	DX3	DX2	DX1	DX0	Output votage				rn	(Ω)
00H	0	0	0	0	0	0	V0'	V0			r0	1150
01H	0	0	0	0	0	1	V1'	V1+(V0-V1)×	6500 /	7650	r1	700
02H	0	0	0	0	1	0	V2'	V1+(V0-V1)×	5800 /	7650	r2	700
03H	0	0	0	0	1	1	V3'	V1+(V0-V1)×	5100 /	7650	r3	700
04H	0	0	0	1	0	0	V4'	V1+(V0-V1)×	4400 /	7650	r4	700
05H	0	0	0	1	0	1	V5'	V1+(V0-V1)×	3700 /	7650	r5	350
06H	0	0	0	1	1	0	V6'	V1+(V0-V1)×	3350 /	7650	r6	350
07H	0	0	0	1	1	1	V7'	V1+(V0-V1)×	3000 /	7650	r7	350
08H	0	0	1	0	0	0	V8'	V1+(V0-V1)×	2650 /	7650	r8	350
09H	0	0	1	0	0	1	V9'	V1+(V0-V1)×	2300 /	7650	r9	350
0AH	0	0	1	0	1	0	V10'	V1+(V0-V1)×	1950 /	7650	r10	350
0BH	0	0	1	0	1	1	V11'	V1+(V0-V1)×	1600 /	7650	r11	350
0CH	0	0	1	1	0	0	V12'	V1+(V0-V1)×	1250 /	7650	r12	350
0DH	0	0	1	1	0	1	V13'	V1+(V0-V1)×	900 /	7650	r13	300
0EH	0	0	1	1	1	0	V14'	V1+(V0-V1)×	600 /	7650	r14	300
0FH	0	0	1	1	1	1	V15'	V1+(V0-V1)×	300 /	7650	r15	300
10H	0	1	0	0	0	0	V16'	V1			r16	200
11H	0	1	0	0	0	1	V17	V2+(V1-V2)×	2100 /	2300	r17	200
12H	0	1	0	0	1	0	V18'	V2+(V1-V2)×	1900 /	2300	r18	200
13H	0	1	0	0	1	1	V19'	V2+(V1-V2)×	1700 /	2300	r19	200
14H	0	1	0	1	0	0	V20'	V2+(V1-V2)×	1500 /	2300	r20	200
15H	0	1	0	1	0	1	V21'	V2+(V1-V2)×	1300 /	2300	r21	150
16H	0	1	0	1	1	0	V22'	V2+(V1-V2)×	1150 /	2300	r22	150
17H	0	1	0	1	1	1	V23'	V2+(V1-V2)×	1000 /	2300	r23	150
18H	0	1	1	0	0	0	V24'	V2+(V1-V2)×	850 /	2300	r24	150
19H	0	1	1	0	0	1	V25'	V2+(V1-V2)×	700 /	2300	r25	100
1AH	0	1	1	0	1	0	V26'	V2+(V1-V2)×	600 /	2300	r26	100
1BH	0	1	1	0	1	1	V27'	V2+(V1-V2)×	500 /	2300	r27	100
1CH	0	1	1	1	0	0	V28'	V2+(V1-V2)×	400 /	2300	r28	100
1DH	0	1	1	1	0	1	V29'	V2+(V1-V2)×	300 /	2300	r29	100
1EH	0	1	1	1	1	0	V30'	V2+(V1-V2)×	200 /	2300	r30	100
1FH	0	1	1	1	1	1	V31'	V2+(V1-V2)×	100 /	2300	r31	100
20H	1	0	0	0	0	0	V32'	V2			r32	100
21H	1	0	0	0	0	1	V33'	V3+(V2-V3)×	1550 /	1650	r33	100
22H	1	0	0	0	1	0	V34'	V3+(V2-V3)×	1450 /	1650	r34	100
23H	1	0	0	0	1	1	V35'	V3+(V2-V3)×	1350 /	1650	r35	100
24H	1	0	0	1	0	0	V36'	V3+(V2-V3)×	1250 /	1650	r36	100
25H	1	0	0	1	0	1	V37'	V3+(V2-V3)×	1150 /	1650	r37	100
26H	1	0	0	1	1	0	V38'	V3+(V2-V3)×	1050 /	1650	r38	100
27H	1	0	0	1	1	1	V39'	V3+(V2-V3)×	950 /	1650	r39	100
28H	1	0	1	0	0	0	V40'	V3+(V2-V3)×	850 /	1650	r40	100
29H	1	0	1	0	0	1	V41'	V3+(V2-V3)×	750 /	1650	r41	100
2AH	1	0	1	0	1	0	V42'	V3+(V2-V3)×	650 /	1650	r42	100
2BH	1	0	1	0	1	1	V43'	V3+(V2-V3)×	550 /	1650	r43	100
2CH	1	0	1	1	0	0	V44'	V3+(V2-V3)×	450 /	1650	r44	100
2DH	1	0	1	1	0	1	V45'	V3+(V2-V3)×	350 /	1650	r45	100
2EH	1	0	1	1	1	0	V46'	V3+(V2-V3)×	250 /	1650	r46	100
2FH	1	0	1	1	1	1	V47'	V3+(V2-V3)×	150 /	1650	r47	150
30H	1	1	0	0	0	0	V48'	V3			r48	150
31H	1	1	0	0	0	1	V49'	V4+(V3-V4)×	4100 /	4250	r49	150
32H	1	1	0	0	1	0	V50'	V4+(V3-V4)×	3950 /	4250	r50	150
33H	1	1	0	0	1	1	V51'	V4+(V3-V4)×	3800 /	4250	r51	150
34H	1	1	0	1	0	0	V52'	V4+(V3-V4)×	3650 /	4250	r52	150
35H	1	1	0	1	0	1	V53'	V4+(V3-V4)×	3500 /	4250	r53	150
36H	1	1	0	1	1	0	V54'	V4+(V3-V4)×	3350 /	4250	r54	150
37H	1	1	0	1	1	1	V55'	V4+(V3-V4)×	3200 /	4250	r55	250
38H	1	1	1	0	0	0	V56'	V4+(V3-V4)×	2950 /	4250	r56	250
39H	1	1	1	0	0	1	V57'	V4+(V3-V4)×	2700 /	4250	r57	250
3AH	1	1	1	0	1	0	V58'	V4+(V3-V4)×	2450 /	4250	r58	300
3BH	1	1	1	0	1	1	V59'	V4+(V3-V4)×	2150 /	4250	r59	300
3CH	1	1	1	1	0	0	V60'	V4+(V3-V4)×	1850 /	4250	r60	300
3DH	1	1	1	1	0	1	V61'	V4+(V3-V4)×	1550 /	4250	r61	450
3EH	1	1	1	1	1	0	V62'	V4+(V3-V4)×	1100 /	4250	r62	1100
3FH	1	1	1	1	1	1	V63'	V4			r total	15850

Caution There is no connection between V_4 and V_5 terminal in the chip.

Figure 5-3. Relationship between Input Data and Output Voltage

0.5 V_{DD2} > V_5 > V_6 > V_7 > V_8 > V_9 > V_{SS2} + 0.1 V, POL21/22 = L



Data	DX5	DX4	DX3	DX2	DX1	DX0	Output voltage				rn	(Ω)
00H	0	0	0	0	0	0	V0"	V9			r0	1150
01H	0	0	0	0	0	1	V1"	V9+(V8-V9)×	1150 /	7650	r1	700
02H	0	0	0	0	1	0	V2"	V9+(V8-V9)×	1850 /	7650	r2	700
03H	0	0	0	0	1	1	V3"	V9+(V8-V9)×	2550 /	7650	r3	700
04H	0	0	0	1	0	0	V4"	V9+(V8-V9)×	3250 /	7650	r4	700
05H	0	0	0	1	0	1	V5"	V9+(V8-V9)×	3950 /	7650	r5	350
06H	0	0	0	1	1	0	V6"	V9+(V8-V9)×	4300 /	7650	r6	350
07H	0	0	0	1	1	1	V7"	V9+(V8-V9)×	4650 /	7650	r7	350
08H	0	0	1	0	0	0	V8"	V9+(V8-V9)×	5000 /	7650	r8	350
09H	0	0	1	0	0	1	V9"	V9+(V8-V9)×	5350 /	7650	r9	350
0AH	0	0	1	0	1	0	V10"	V9+(V8-V9)×	5700 /	7650	r10	350
0BH	0	0	1	0	1	1	V11"	V9+(V8-V9)×	6050 /	7650	r11	350
0CH	0	0	1	1	0	0	V12"	V9+(V8-V9)×	6400 /	7650	r12	350
0DH	0	0	1	1	0	1	V13"	V9+(V8-V9)×	6750 /	7650	r13	300
0EH	0	0	1	1	1	0	V14"	V9+(V8-V9)×	7050 /	7650	r14	300
0FH	0	0	1	1	1	1	V15"	V9+(V8-V9)×	7350	7650	r15	300
10H	0	1	0	0	0	0	V16"	V8			r16	200
11H	0	1	0	0	0	1	V17"	V8+(V7-V8)×	200 /	2300	r17	200
12H	0	1	0	0	1	0	V18"	V8+(V7-V8)×	400 /	2300	r18	200
13H	0	1	0	0	1	1	V19"	V8+(V7-V8)×	600 /	2300	r19	200
14H	0	1	0	1	0	0	V20"	V8+(V7-V8)×	800 /	2300	r20	200
15H	0	1	0	1	0	1	V21"	V8+(V7-V8)×	1000 /	2300	r21	150
16H	0	1	0	1	1	0	V22"	V8+(V7-V8)×	1150 /	2300	r22	150
17H	0	1	0	1	1	1	V23"	V8+(V7-V8)×	1300 /	2300	r23	150
18H	0	1	1	0	0	0	V24"	V8+(V7-V8)×	1450 /	2300	r24	150
19H	0	1	1	0	0	1	V25"	V8+(V7-V8)×	1600 /	2300	r25	100
1AH	0	1	1	0	1	0	V26"	V8+(V7-V8)×	1700 /	2300	r26	100
1BH	0	1	1	0	1	1	V27"	V8+(V7-V8)×	1800 /	2300	r27	100
1CH	0	1	1	1	0	0	V28"	V8+(V7-V8)×	1900 /	2300	r28	100
1DH	0	1	1	1	0	1	V29"	V8+(V7-V8)×	2000 /	2300	r29	100
1EH	0	1	1	1	1	0	V30"	V8+(V7-V8)×	2100 /	2300	r30	100
1FH	0	1	1	1	1	1	V31"	V8+(V7-V8)×	2200	2300	r31	100
20H	1	0	0	0	0	0	V32"	V7			r32	100
21H	1	0	0	0	0	1	V33"	V7+(V6-V7)×	100 /	1650	r33	100
22H	1	0	0	0	1	0	V34"	V7+(V6-V7)×	200 /	1650	r34	100
23H	1	0	0	0	1	1	V35"	V7+(V6-V7)×	300 /	1650	r35	100
24H	1	0	0	1	0	0	V36"	V7+(V6-V7)×	400 /	1650	r36	100
25H	1	0	0	1	0	1	V37"	V7+(V6-V7)×	500 /	1650	r37	100
26H	1	0	0	1	1	0	V38"	V7+(V6-V7)×	600 /	1650	r38	100
27H	1	0	0	1	1	1	V39"	V7+(V6-V7)×	700 /	1650	r39	100
28H	1	0	1	0	0	0	V40"	V7+(V6-V7)×	800 /	1650	r40	100
29H	1	0	1	0	0	1	V41"	V7+(V6-V7)×	900 /	1650	r41	100
2AH	1	0	1	0	1	0	V42"	V7+(V6-V7)×	1000 /	1650	r42	100
2BH	1	0	1	0	1	1	V43"	V7+(V6-V7)×	1100 /	1650	r43	100
2CH	1	0	1	1	0	0	V44"	V7+(V6-V7)×	1200 /	1650	r44	100
2DH	1	0	1	1	0	1	V45"	V7+(V6-V7)×	1300 /	1650	r45	100
2EH	1	0	1	1	1	0	V46"	V7+(V6-V7)×	1400 /	1650	r46	100
2FH	1	0	1	1	1	1	V47"	V7+(V6-V7)×	1500 /	1650	r47	150
30H	1	1	0	0	0	0	V48"	V6			r48	150
31H	1	1	0	0	0	1	V49"	V6+(V5-V6)×	150 /	4250	r49	150
32H	1	1	0	0	1	0	V50"	V6+(V5-V6)×	300 /	4250	r50	150
33H	1	1	0	0	1	1	V51"	V6+(V5-V6)×	450 /	4250	r51	150
34H	1	1	0	1	0	0	V52"	V6+(V5-V6)×	600 /	4250	r52	150
35H	1	1	0	1	0	1	V53"	V6+(V5-V6)×	750 /	4250	r53	150
36H	1	1	0	1	1	0	V54"	V6+(V5-V6)×	900 /	4250	r54	150
37H	1	1	0	1	1	1	V55"	V6+(V5-V6)×	1050 /	4250	r55	250
38H	1	1	1	0	0	0	V56"	V6+(V5-V6)×	1300 /	4250	r56	250
39H	1	1	1	0	0	1	V57"	V6+(V5-V6)×	1550 /	4250	r57	250
3AH	1	1	1	0	1	0	V58"	V6+(V5-V6)×	1800 /	4250	r58	300
3BH	1	1	1	0	1	1	V59"	V6+(V5-V6)×	2100 /	4250	r59	300
3CH	1	1	1	1	0	0	V60"	V6+(V5-V6)×	2400 /	4250	r60	300
3DH	1	1	1	1	0	1	V61"	V6+(V5-V6)×	2700 /	4250	r61	450
3EH	1	1	1	1	1	0	V62"	V6+(V5-V6)×	3150 /	4250	r62	1100
3FH	1	1	1	1	1	1	V63"	V5			r total	15850

Caution There is no connection between V_4 and V_5 terminal in the chip.

6. RELATIONSHIP BETWEEN INPUT DATA AND OUTPUT PIN

Data format : 6 bits x 2 RGBs (6 dots)

Input width : 36 bits (2-pixel data)

(1) R,/L = H (Right shift)

Output	S_1	S_2	S_3	S_4	···	S_{479}	S_{480}
Data	D_{00} to D_{05}	D_{10} to D_{15}	D_{20} to D_{25}	D_{30} to D_{35}	···	D_{40} to D_{45}	D_{50} to D_{55}

(2) R,/L = L (Left shift)

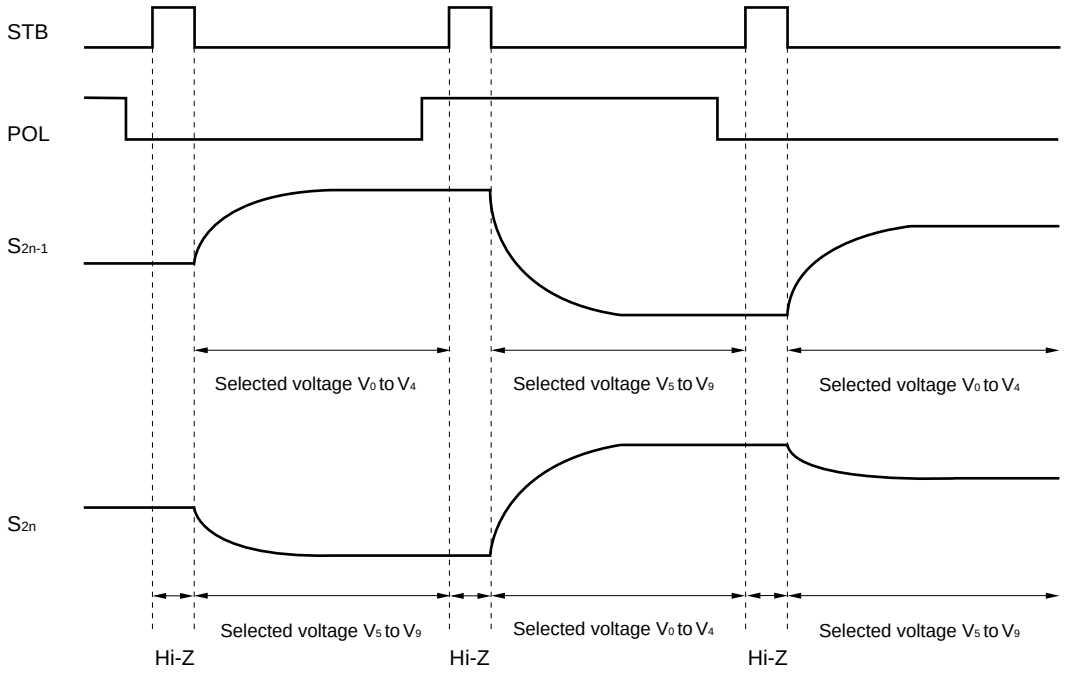
Output	S_1	S_2	S_3	S_4	···	S_{479}	S_{480}
Data	D_{00} to D_{05}	D_{10} to D_{15}	D_{20} to D_{25}	D_{30} to D_{35}	···	D_{40} to D_{45}	D_{50} to D_{55}

POL	S_{2n-1} Note	S_{2n} Note
L	V_0 to V_4	V_5 to V_9
H	V_5 to V_9	V_0 to V_4

Note S_{2n-1} (Odd output), S_{2n} (Even output)

7. RELATIONSHIP BETWEEN STB, POL AND OUTPUT WAVEFORM

The output voltage is written to the LCD panel synchronized with the STB falling edge.



8. RELATIONSHIP BETWEEN STB, CLK AND OUTPUT WAVEFORM

The output voltage is written to the LCD panel synchronized with the STB falling edge.

Figure 8–1. Output Circuit Block Diagram

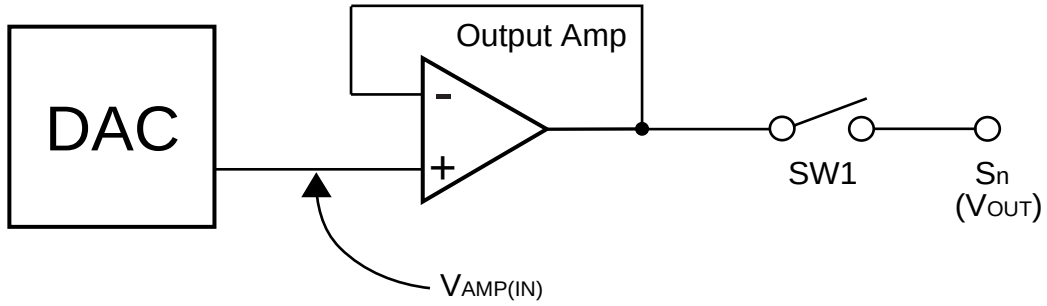
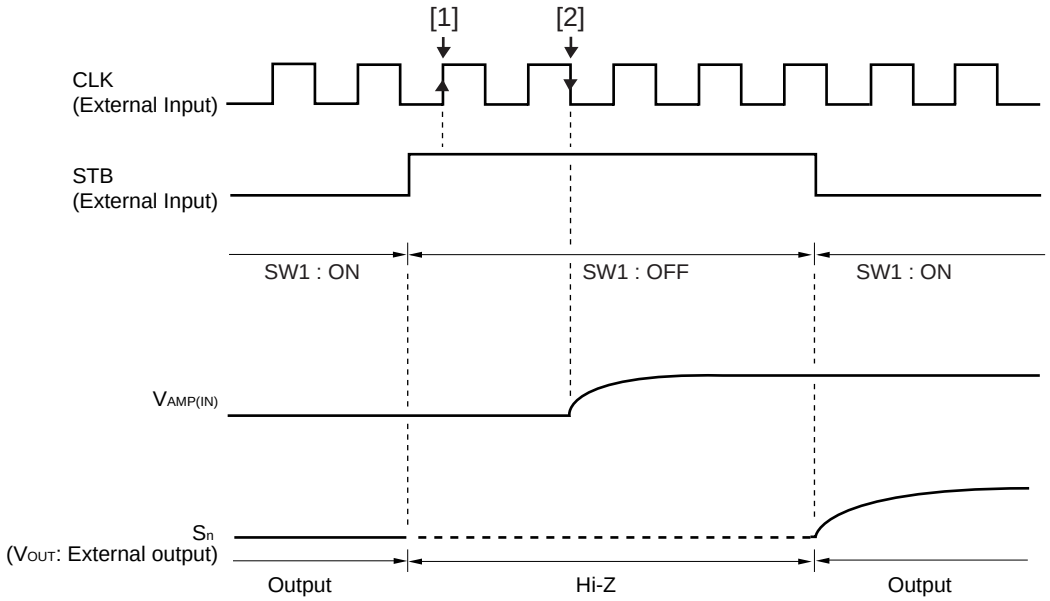


Figure 8–2. Output Circuit Timing Waveform



Remarks 1. STB = L : SW1 = ON
STB = H : SW1 = OFF

2. STB = “H” is acknowledged at timing [1].

3. The display data latch is compensated at timing [2] and the input voltage ($V_{AMP(IN)}$: gray-scale level voltage) of the output amplifier changes.

9. CURRENT CONSUMPTION REDUCTION FUNCTION

The μPD16772A has a low power control function (LPC) which can switch the bias current of the output amplifier between two levels and a bias control function (Bcont) which can be used to finely control the bias current.

- Low Power Control Function (LPC)

  The bias current of the output amplifier can be switched between two levels using this pin (Bcont: Open).

  LPC = H or Open: Low power mode

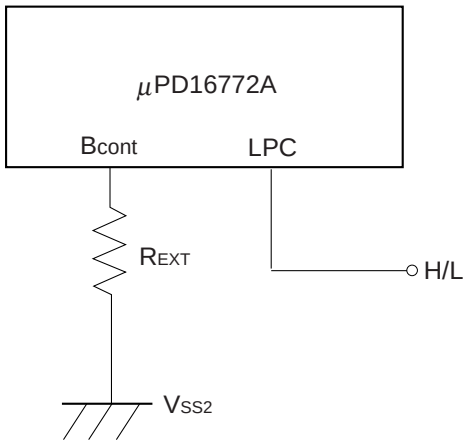
  LPC = L: Normal power mode

  The V_{DD2} of static current consumption can be reduced to two thirds of that in normal mode. Input a stable DC current (V_{DD1}/V_{SS1}) to this pin.

- Bias Current Control Function (Bcont)

  It is possible to fine-control the current consumption by using the bias current control function (Bcont pin). When using this function, connect this pin to the stabilized ground potential (V_{SS2}) via an external resistor (R_{EXT}). When not using this function, leave this pin open.

Figure 9–1. Bias Current Control Function (Bcont)



Refer to the table below for the percentage of current regulation when using the bias current control function.

Table 9–1. Current Consumption Regulation Percentage Compared to Normal Mode

R_{EXT}	Current Consumption Regulation Percentage		
	LPC = L	LPC = H/Open	
∞ (Open)	100%	65%	V_{DD1} = 3.3 V
50 kΩ	120%	80%	V_{DD2} = 8.7 V
20 kΩ	140%	100%	
0 Ω	240%	210%	

Remark The above current consumption regulation percentages are not product-characteristic guaranteed as they re based on the results of simulation.

Caution Because the low-power and bias-current control functions control the bias current in the output amplifier and regulate the over-all current consumption of the driver IC, when this occurs, the characteristics of the output amplifier will simultaneously change. Therefore, when using these functions, be sure to sufficiently evaluate the picture quality.

10. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Rating	Unit
Logic Part Supply Voltage	V_{DD1}	–0.5 to +4.0	V
Driver Part Supply Voltage	V_{DD2}	–0.5 to +10.0	V
Logic Part Input Voltage	V_{I1}	–0.5 to V_{DD1} + 0.5	V
Driver Part Input Voltage	V_{I2}	–0.5 to V_{DD2} + 0.5	V
Logic Part Output Voltage	V_{O1}	–0.5 to V_{DD1} + 0.5	V
Driver Part Output Voltage	V_{O2}	–0.5 to V_{DD2} + 0.5	V
Operating Ambient Temperature	T_A	–10 to +75	°C
Storage Temperature	T_{stg}	–55 to +125	°C

★ **Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.**

Recommended Operating Range (T_A = –10 to +75°C, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Logic Part Supply Voltage	V_{DD1}		2.3		3.6	V
Driver Part Supply Voltage	V_{DD2}		8.0	8.5	9.0	V
High-Level Input Voltage	V_{IH}		0.7 V_{DD1}		V_{DD1}	V
Low-Level Input Voltage	V_{IL}		0		0.3 V_{DD1}	V
γ-Corrected Voltage	V_0 to V_9		V_{SS2} + 0.1		V_{DD2} – 0.1	V
Driver Part Output Voltage	V_O		V_{SS2} + 0.1		V_{DD2} – 0.1	V
Clock Frequency	f_{CLK}	V_{DD2} = 2.3 V			45	MHz

Electrical Characteristics (T_A = –10 to +75°C, V_{DD1} = 2.3 to 3.6 V, V_{DD2} = 8.5 V ± 0.5 V, V_{SS1} = V_{SS2} = 0 V, unless otherwise specified, the input level is defined to be LPC = L, Bcont = Open)

	Parameter	Symbol	Condition		MIN.	TYP.	MAX.	Unit
	Input Leak Current	I_{IL}					±1.0	μA
	High-Level Output Voltage	V_{OH}	STHR (STHL), I_{OH} = 0 mA		V_{DD1} – 0.1			V
	Low-Level Output Voltage	V_{OL}	STHR (STHL), I_{OL} = 0 mA				0.1	V
	γ-Corrected Supply Current	I_γ	V_{DD2} = 8.5 V	V_0 pin, V_5 pin	126	252	504	μA
			V_0 to V_4 = V_5 to V_9 = 4.0 V	V_4 pin, V_9 pin	–504	–252	–126	μA
	Driver Output Current	I_{VOH}	V_X = 7.0 V, V_{OUT} = 6.5 V **Note**				–30	μA
		I_{VOL}	V_X = 1.0 V, V_{OUT} = 1.5 V **Note**		30			μA
	Output Voltage Deviation	ΔV_O	T_A = 25°C			±7	±20	mV
	Output Swing Difference Deviation	ΔV_{P-P}	V_{DD1} = 3.3 V, V_{DD2} = 8.5 V V_{OUT} = 2.0 V, 4.25 V, 6.5 V			±2	±15	mV
★	Logic Part Dynamic Current Consumption	I_{DD1}	V_{DD1}			1.0	7.5	mA
★	Driver Part Dynamic Current Consumption	I_{DD2}	V_{DD2}, with no load			3.5	7.5	mA

Note V_X refers to the output voltage of analog output pins S_1 to S_{480}.
V_{OUT} refers to the voltage applied to analog output pins S_1 to S_{480}.

★ **Cautions 1. f_{STB} = 50 kHz, f_{CLK} = 40 MHz.**

2. The TYP. values refer to an all black or all white input pattern. The MAX. value refers to the measured values in the dot checkerboard input pattern.

3. Refers to the current consumption per driver when cascades are connected under the assumption of UXGA single-sided mounting (10 units).

Switching Characteristics (T_A = –10 to +75°C, V_{DD1} = 2.3 to 3.6 V, V_{DD2} = 8.5 V ± 0.5 V, V_{SS1} = V_{SS2} = 0 V, unless otherwise specified, the input level is defined to be LPC = L, Bcont = Open)

	Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
	Start Pulse Delay Time	t_{PLH1}	C_L = 10 pF		10	20	ns
		t_{PHL1}			10	20	ns
★	Driver Output Delay Time	t_{PLH2}	C_L = 75 pF, R_L = 5 kΩ		2.5	5	μs
★		t_{PLH3}			5	8	μs
★		t_{PHL2}			2.5	5	μs
★		t_{PHL3}			5	8	μs
	Input Capacitance	C_{I1}	STHR (STHL) excluded, T_A = 25°C		5	10	pF
		C_{I2}	STHR (STHL), T_A = 25°C		8	10	pF

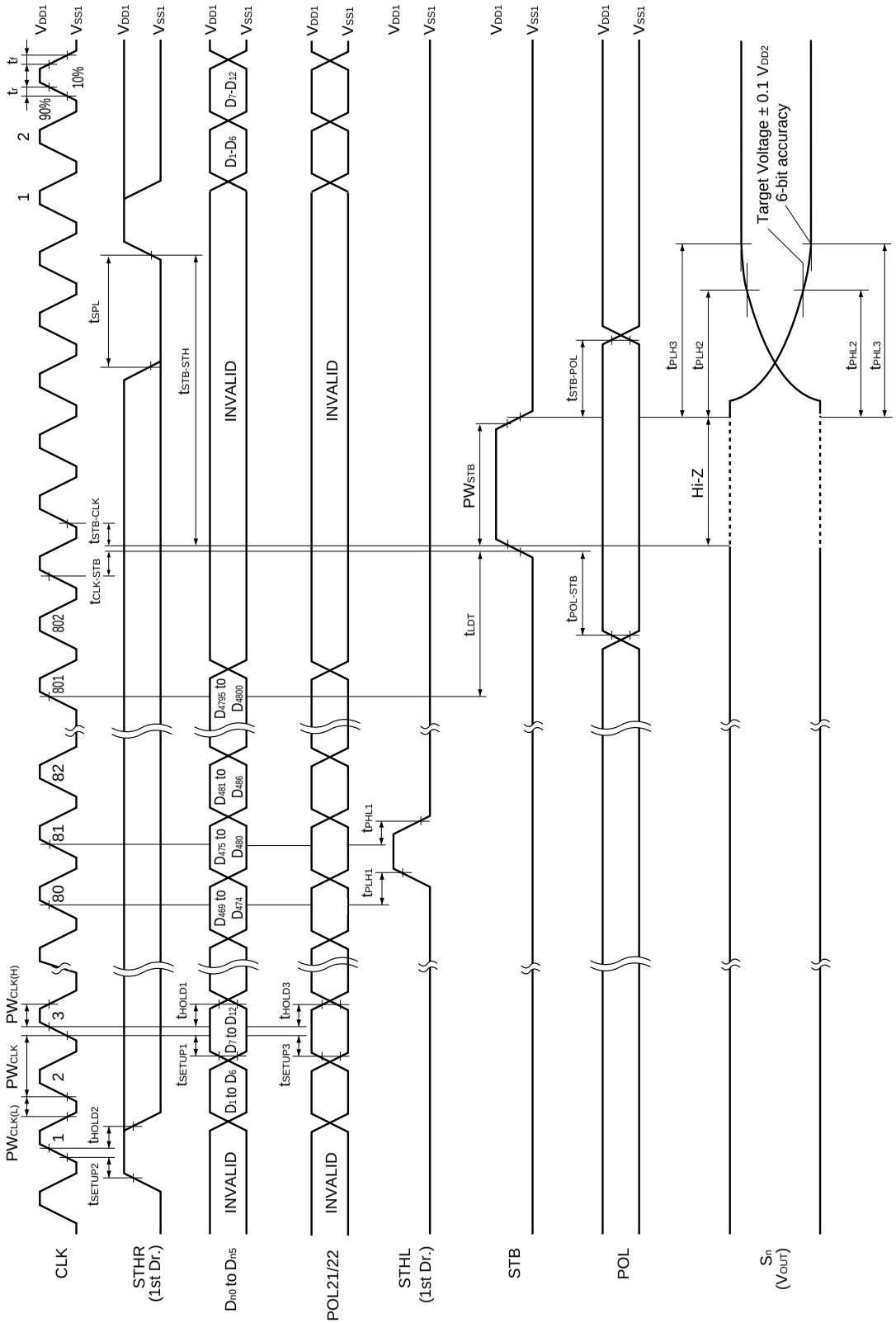
★ **Timing Requirements (T_A = –10 to +75°C, V_{DD1} = 2.3 to 3.6 V, V_{SS1} = 0 V, $t_r = t_f$ = 5.0 ns)**

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Clock Pulse Width	PW_{CLK}	V_{DD1} = 2.3 to 3.6 V	22			ns
Clock Pulse High Period	$PW_{CLK(H)}$		4			ns
Clock Pulse Low Period	$PW_{CLK(L)}$	V_{DD1} = 2.3 to 3.0 V	7			ns
		V_{DD1} = 3.0 to 3.6 V	4			ns
Data Setup Time	t_{SETUP1}		3			ns
Data Hold Time	t_{HOLD1}		0			ns
Start Pulse Setup Time	t_{SETUP2}		3			ns
Start Pulse Hold Time	t_{HOLD2}		0			ns
POL21/22 Setup Time	t_{SETUP3}		3			ns
POL21/22 Hold Time	t_{HOLD3}	V_{DD1} = 2.3 to 3.0 V	1			ns
		V_{DD1} = 3.0 to 3.6 V	0			ns
Start Pulse Low Period	t_{SPL}		1			CLK
STB Pulse Width	PW_{STB}		2			CLK
Last Data Timing	t_{LDT}		2			CLK
CLK-STB Time	$t_{CLK-STB}$	CLK ↑ → STB ↑	6			ns
STB-CLK Time	$t_{STB-CLK}$	STB ↑ → CLK ↑ V_{DD1} = 2.3 to 3.0 V	14			ns
		STB ↑ → CLK ↑ V_{DD1} = 3.0 to 3.6 V	6			ns
Time Between STB and Start Pulse	$t_{STB-STH}$	STB ↑ → STHR(STHL) ↑	2			CLK
POL-STB Time	$t_{POL-STB}$	POL ↑ or ↓ → STB ↑	–5			ns
STB-POL Time	$t_{STB-POL}$	STB ↓ → POL ↓ or ↑	6			ns

Remark Unless otherwise specified, the input level is defined to be V_{IH} = 0.7 V_{DD1}, V_{IL} = 0.3 V_{DD1}.

11. SWITCHING CHARACTERISTIC WAVEFORM(R,/L= H)

Unless otherwise specified, the input level is defined to be V_{IH} = 0.7 V_{DD1}, V_{IL} = 0.3 V_{DD1}.



12. RECOMMENDED MOUNTING CONDITIONS

The following conditions must be met for mounting conditions of the μPD16772A.

For more details, refer to the **Semiconductor Device Mounting Technology Manual (C10535E).**

Please consult with our sales offices in case other mounting process is used, or in case the mounting is done under different conditions.

μPD16772AN-xxx: TCP (TAB Package)

Mounting Condition	Mounting Method	Condition
Thermocompression	Soldering	Heating tool 300 to 350°C, heating for 2 to 3 seconds : pressure 100 g (per solder)
	ACF (Adhesive Conductive Film)	Temporary bonding 70 to 100°C : pressure 3 to 8 kg/cm^2: time 3 to 5 sec. Real bonding 165 to 180°C: pressure 25 to 45 kg/cm^2: time 30 to 40 sec. (When using the anisotropy conductive film SUMIZAC1003 of Sumitomo Bakelite,Ltd).

Caution To find out the detailed conditions for mounting the ACF part, please contact the ACF manufacturing company. Be sure to avoid using two or more mounting methods at a time.

[MEMO]

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Reference Documents

NEC Semiconductor Device Reliability/Quality Control System(C10983E)

Quality Grades to NEC's Semiconductor Devices(C11531E)

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