Applications

- Dual-mode GPS and Galileo receivers
- Software-defined GNSS radio systems
- High sensitivity / low power GNSS / A-GNSS apps.
- Portable navigation devices, mobile phones, and GNSS peripheral devices
- Telematics equipment

Features

- Single conversion L1-band GPS/Galileo radio with integrated IF filter
- 2-bit serialized digital I/Q output at near-zero IF
- Integrated LNA with high-gain (18.5 dB typ.) and low NF (1.7 dB typ.)
- Low 2.2 dB typ. RF system noise figure
- Low 10 mA operating current with 2.7-3.6 V supply; 8 mA with internal LNA disabled
- Low Standby current 3 µA typical
- Fully integrated VCO and resonator
- Integrated PLL supporting 16.368 MHz reference frequency
- I/O supply range extends down to 1.7 V
- 4 x 4 mm 24 pin QFN, RoHS-compliant package

Ordering Information

Part No.	Package	Remark
SE4120L-R	24 Pin QFN	Shipped in Tape & Reel

Product Description

The SE4120L is a highly-integrated GNSS radio front end IC offering high performance and low power operation in a wide range of low-cost applications. It supports GPS and dual-mode L1-band GPS/Galileo products. The SE4120L features a conditioned interface for software implementations of GNSS baseband signal processing.

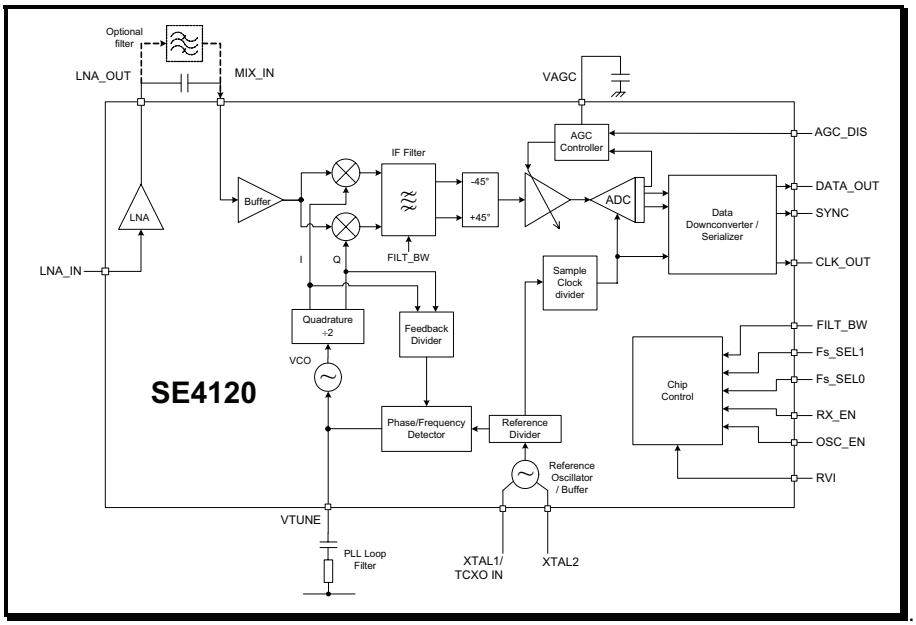
The SE4120L includes an on-chip LNA, a low IF receiver with a linear AGC and an advanced multi-bit I/Q analog to digital converter (ADC) with serialized data output. The receiver incorporates a fully integrated image reject mixer, obviating the need for a SAW filter in many applications. The SE4120L's on-chip IF filter may be adjusted from 2.2 MHz BW (for GPS only) to 4.4MHz BW (for simultaneous reception of Galileo and GPS signals). The digitized I/Q output, centered near-zero IF, is available in a serialized data stream to facilitate software signal processing.

The highly-integrated PLL synthesizer of the SE4120L requires only two passive components to implement an off-chip loop filter.

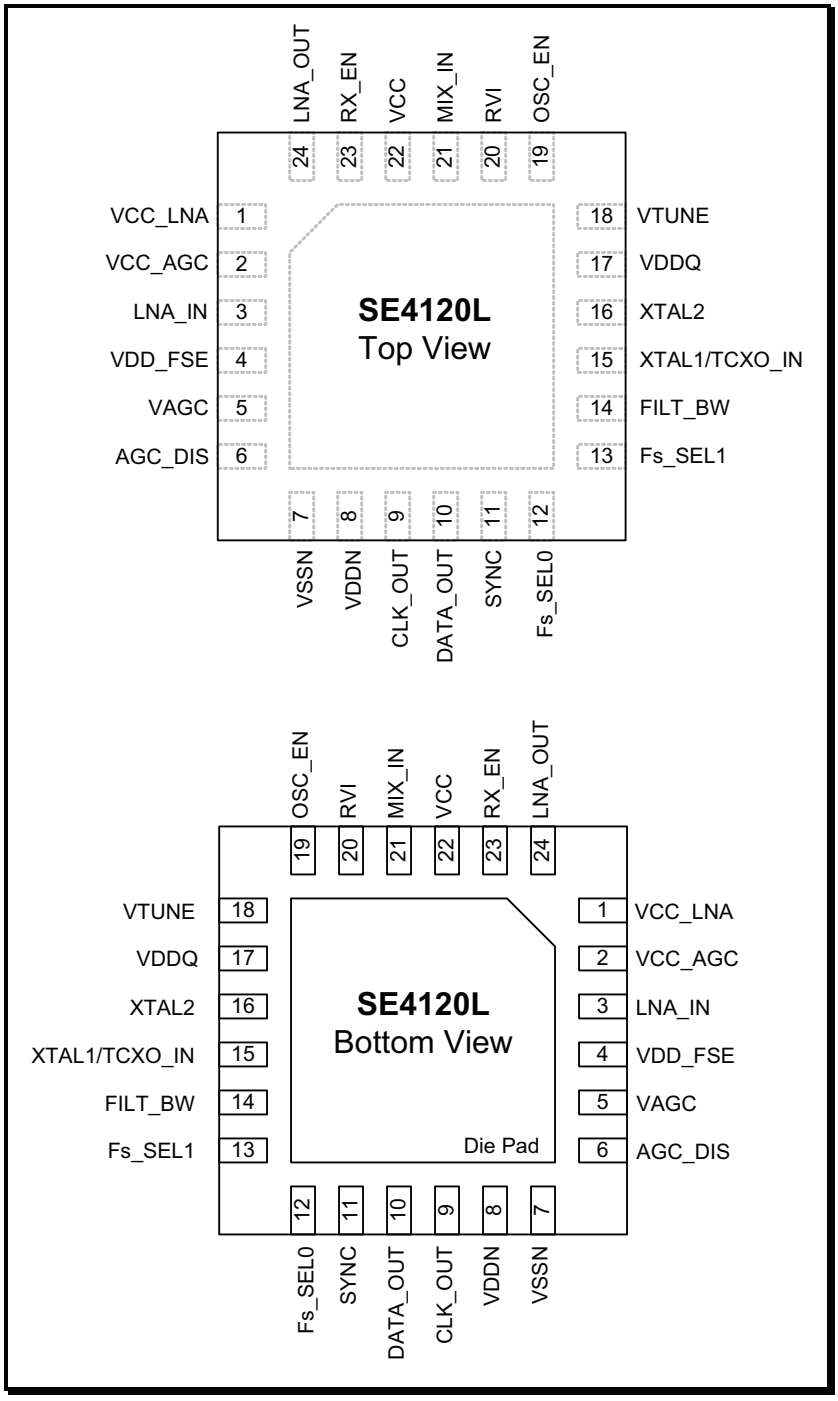
The SE4120L is optimized for the lowest possible power consumption consistent with a very low external component count.

The SE4120L incorporates current-controlled low-spurious output buffers which may be run from a separate external supply to interface to low voltage systems. Output buffers supply sufficient current to drive most baseband devices directly.

Functional Block Diagram



Pin Out Diagram



Pin Descriptions

Pin No.	Name	Description	Connection
1	VCC_LNA	Analogue power supply for LNA	Connect to VCC via dedicated decoupling network to enable LNA Connect to GND to disable LNA
2	VCC_AGC	Analogue power supply for AGC	Connect to VCC
3	LNA_IN	LNA RF input	DC blocking capacitor required Connect to matching network in a compact RF layout
4	VDD_FSE	Power supply for configuration logic	Connect to VCC
5	VAGC	AGC filter capacitor	Single capacitor to GND (Pin also allows external control of AGC when AGC_DIS = '1')
6	AGC_DIS	AGC inhibit input	AGC Gain hold (Connect to VDD) or Enable AGC (Connect to VSSN / GND)
7	VSSN	Ground return for digital interface	Connect to GND, or digital ground for baseband IC
8	VDDN	Digital power supply for digital interface	Connect to VDD, or digital supply for baseband IC
9	CLK_OUT	Sample clock output	ADC Sample Clock output at VDDN logic levels
10	DATA_OUT	Serialized IF data output	ADC serial I/Q output at VDDN logic levels
11	SYNC	IF data sync output	ADC data Sync output at VDDN logic levels
12	Fs_SEL0	Serial IF data output select (bit 0)	Select desired serial data output, sample rate, and format, as per "Fs_SEL Hardware Configuration" Table (Connect to RX_EN (pin 23) or VSSN / GND as required)
13	Fs_SEL1	Serial IF data output select (bit 1)	
14	FILT_BW	IF filter bandwidth select	Connect to RX_EN for dual-mode Galileo/GPS Connect to VSSN for GPS only
15	XTAL1/TCXO_IN	Crystal / TCXO connection	Connect to AC coupled TCXO reference signal if using a TCXO reference source. Connect to one lead of crystal if using a crystal reference source
16	XTAL2	Crystal connection	Leave unconnected if using a TCXO reference source. Connect to other lead of crystal if using a crystal reference source.

Pin No.	Name	Description	Connection
17	VDDQ	Power supply for quiet digital circuits	Connect to VCC
18	VTUNE	VCO tuning voltage input / PLL phase-detector output	Connect to PLL filter network
19	OSC_EN	Crystal oscillator enable	Connect to VSSN / GND if using a TCXO reference source. Connect to VDD if using a crystal reference source.
20	RVI	Program baseband output drive current	Leave unconnected or Connect via a resistor to analogue VCC for up to 2x output drive current
21	MIX_IN	Mixer input	DC coupled RF input to RF mixer
22	VCC	Analogue power supply for RF front end	Connect to VCC
23	RX_EN	Receiver enable	Connect to VDD to enable radio Connect to VSSN / GND to disable radio
24	LNA_OUT	LNA RF output	RF output from LNA. DC blocked, with 10 kΩ (nom.) DC impedance to ground.
Die Pad	GND	Ground connection	Main IC GND connection

Functional Description

LNA

LNA performance is the largest single contributor to overall system sensitivity in both GPS and Galileo signal reception. The internal LNA of the SE4120L allows excellent performance to be achieved from a low-power GNSS receiver without requiring any additional active components.

The Galileo and GPS L1 input signals are both centered on 1575.42 MHz, and can be simultaneously applied to LNA_IN (pin 3).

The SE4120L LNA input requires a minimum of external matching components to achieve good RF gain with minimal noise figure: only a single series inductor and single shunt capacitor are required. The input requires a DC blocking cap if circuitry prior the LNA has a DC bias. Although attention should be paid to track lengths and interference throughout the design, the LNA input matching circuit is the only RF circuit critically sensitive to layout.

The LNA output includes internal 50 Ω matching for connection to the mixer input either directly or via an optional external filter.

In applications where the internal LNA is not required, the LNA may be disabled by connecting VCC_LNA (pin 1) to GND. This will save approximately 1.9 mA of active current.

Mixer RF Input

The mixer RF input pin MIX_IN (pin 21) is a single ended 50 Ω input, designed to interface either with LNA_OUT (pin 24) or with the output of an external filter. An external active antenna can also be connected to the mixer input.

The image reject mixer ensures that the receiver's full sensitivity is achieved without an external filter. For applications where additional selectivity is required, an external filter can be added between the LNA_OUT and MIX_IN pins.

IF Filter

The SE4120L includes a fully-integrated intermediate frequency (IF) filter that provides excellent interference rejection with no additional external components. The filter has a 3rd order Butterworth bandpass response.

The IF filter operates in two modes. In one mode, Galileo and GPS signals are allowed to pass; in the other, only GPS signals are captured. The two modes can be set by a Logic '1' on FILT_BW (pin 14) for Galileo + GPS (4.4 MHz BW), and a Logic '0' on the same pin for GPS only (2.2 MHz BW). In both cases, the nominal center frequency of the filter is preset to 4.092 MHz.

AGC and ADC

The SE4120L features a linear IF chain with a multi-bit analogue-to-digital converter (ADC).

An Automatic Gain Control (AGC) system is included. This provides gain control over a range greater than 40 dB so that signals are presented at an optimum level to the input of the ADC.

The ADC quantizes the IF signal into a traditional 2-bit real digital IF data comprising MAG and SIGN components. The MAG values control the AGC loop, such that the MAG bit is active (HIGH) for approximately 33% of the time.

The SIGN and MAG signals are fed into a data downconverter and serializer, which in turn generates I/Q digital data that is ultimately available from DATA_OUT (pin 10). Refer to the "Digital Down Sampler" section below for further information.

The AGC time constant is determined by a single external capacitor connected between the VAGC pin, and VSSN / GND. The settling-time of the AGC is within 10 ms with a 10nF capacitor.

The AGC system also features a control-inhibit facility, via AGC_DIS (pin 6). By connecting AGC_DIS to VDDN, the internal AGC controller is inhibited and the gain held at the level set prior to the inhibition. While the AGC controller is inhibited, it is possible to control the AGC gain from an external source by applying a low-impedance voltage to VAGC (pin 5).

Digital Downconverter / Serializer

The SE4120L includes a digital signal conditioning and serial interface function which prepares the digitized GNSS signal data for baseband signal processing. This interface provides a near-zero IF signal data at a minimum data rate and formatted for efficient processing via synchronous serial interface hardware commonly found on microprocessor integrated circuits.

The 2-bit real IF data input to the Downconverter/Serializer is downconverted and represented as 2-bit in-phase (I) and 2-bit

quadrature (Q) components of the signal bandwidth centered at near-zero frequency (0 Hz when using a 16.368 MHz reference).

To allow the lowest possible sample rate, the downconverted IF signal is further filtered to re-shape the noise spectrum and remove any significant degradation from aliasing. Both frequency conversion and filtering functions are performed digitally, avoiding the tolerance, offset and imbalance imperfections associated with analogue converters.

The output data is can be presented in two ways:

1) a series of 8-bit streams of alternating I and Q samples with an Active LO SYNC framing pulse at the beginning of every 8 bits of data. This format is referred to as "Byte Sync."

2) a continuous stream of alternating I and Q samples with an Active HI SYNC pulse coinciding with every SIGN I bit. This format is referred to as "Pulse Sync."

Each sample is presented as alternate I & Q bit values. In 2-bit I/Q mode, a single bit is allocated to I and a single bit allocated to Q. In 4-bit I/Q mode, a SIGN bit and a MAG bit are allocated to each of the I & Q samples.

Serial Data Output format / Sampling Frequency Selection

The serial IF data output is available on a three-wire bus system comprising a single-bit DATA_OUT (pin 10), SYNC (pin 11) and CLK_OUT (pin 9). The output of the data can be configured to be either Byte Sync (distinct 8-bit sequences of data) or Pulse Sync (continuous datastream). The data which is encoded in these formats is derived from the internal ADC in either 2-bit I/Q (1-bit I & 1-bit Q) or 4-bit I/Q (2-bit I and 2-bit Q). Diagrams showing Pulse Sync and Byte Sync serial data appear below.

The following truth table gives the permutations for the serial IF data output. The required configuration may be set by wiring the Fs_SEL[1:0] pins (12, 13) HIGH or LOW to select the required mode. In each of the modes, the same frequency appears at CLK_OUT (pin 9), but in Byte-Sync, wait-states (clock-idle cycles) will be inserted.

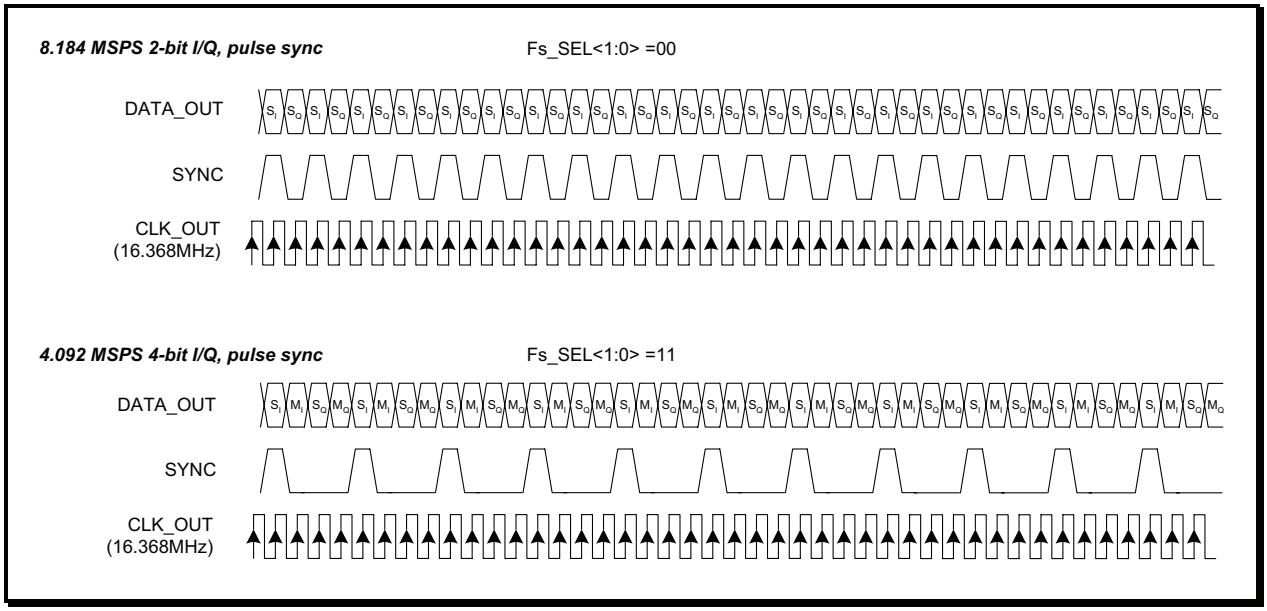
Fs_SEL Hardware Configuration

Fs_SEL [1:0]	Data Output Sampling Rate	Data Output Format	Serial Output Format
00	8.184 MSPS	2 bit I/Q	Pulse
01	5.456 MSPS	2 bit I/Q	Byte
10	4.092 MSPS	2 bit I/Q	Byte
11	4.092 MSPS	4-bit I/Q	Pulse

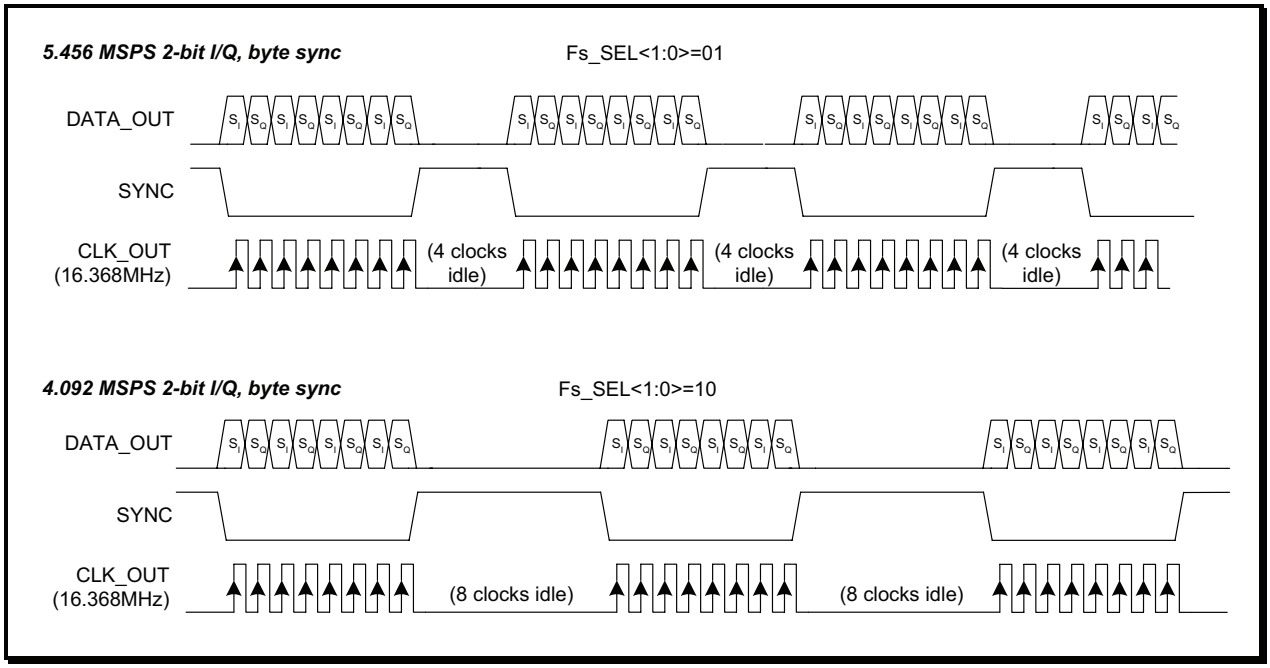
Power-up Sequencing

To use the SE4120L device with either the Fs_SEL0 (pin 12), Fs_SEL1 (pin 13) or FILT_BW (pin 14) connections set to a logic '1' to enable one of the Hardware Configurations described above, it is recommended that the pins concerned are connected directly to the signal driving RX_EN (pin 23). The RX_EN signal should be set to VDD levels (logic '1') a short time (>100us) *after* main VCC/VDD power is applied to the SE4120L device.

Pulse-Sync Serial Data Output Formats



Byte-Sync Serial Data Output Formats



PLL and Loop Filter

The entire phase-locked loop (PLL) generating the local oscillator for the mixer is contained on-chip, with the exception of the PLL loop filter.

A PLL loop filter can be implemented by attaching a capacitor (220pF) and a resistor (33kΩ) in series between VTUNE (pin 18) and GND / VSSN. The PLL follows a classic 3rd-order response; this is achieved in conjunction with an on-chip 10pF capacitor connected between VTUNE and GND / VSSN. Typical PLL loop bandwidth is set to be 200 kHz.

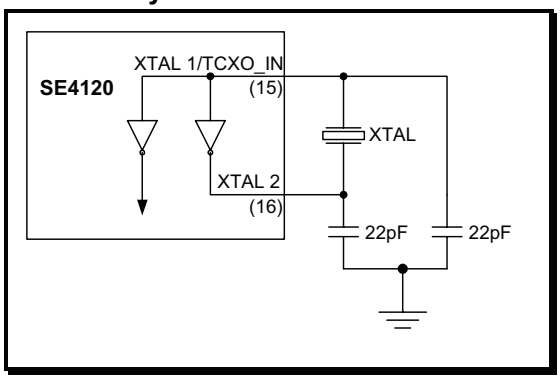
The reference frequency for the PLL may be supplied either externally or using the on-chip crystal oscillator.

Crystal Oscillator

The SE4120L features a very low power crystal oscillator which may be used to provide the frequency reference. The oscillator is designed to work with parallel resonant crystals or be driven from an external TCXO.

The crystal drive level is carefully controlled so that the device is well-suited for use with miniature surface mount crystals. The crystal oscillator is a Pierce configuration, as shown in the diagram below. The application circuit is designed to work with parallel resonant crystals with a parallel load capacitance of approx. 10 pF.

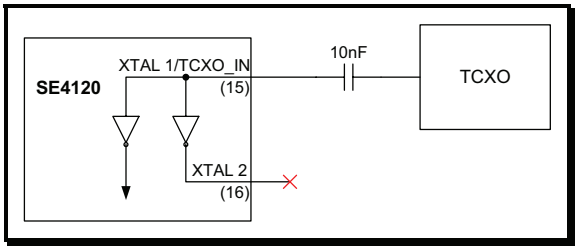
SE4120L Crystal Oscillator



The PCB layout should avoid excessive track length between XTAL1/TCXO_IN (pin 15) and XTAL2 (pin 16) and the crystal. The capacitors at each terminal of the crystal should be mounted adjacent to the crystal and have a low impedance connection to the ground plane in order to maintain the oscillator loop gain and phase noise performance under all conditions.

The SE4120L can also be used with an external TCXO as shown below. The TCXO should provide a clipped sinewave signal. The XTAL2 pin should be left unconnected in this configuration.

SE4120L TCXO Connection



Clock and Data Output Coupling

The high input sensitivity achieved by the SE4120L's internal LNA requires careful control of harmonically related sources of interference.

For this reason the CLK_OUT (pin 9), DATA_OUT (pin 10) and SYNC (pin 11) outputs provide carefully controlled current and slew rate. The data and clock outputs of the SE4120L are specified to drive up to 10pF load (max standard CMOS input capacitance). The output drive of the SE4120L can be adjusted with a resistor connected between VDDQ (pin 17) and RVI (pin 20), as shown in the Logic Level Characteristics section below.

The output current drive is determined by a bias current ratio internal to the SE4120L and the external resistor.

Power Management

The SE4120L has three levels of power control. The primary levels are controlled by two enable pins, RX_EN (pin 23) and OSC_EN (pin 19). A table showing the power control states follows:

SE4120L Power Control States

RX_EN	OSC_EN	Power state
0	0	Standby
0	1	Oscillator only
1	0	Fully active (external reference)
1	1	Fully active (internal reference)

In standby mode all circuits are off and the device consumes only leakage current.

The oscillator-only mode is provided for applications in which the sample clock (CLK_OUT (pin 9)) must remain available even when active GPS reception is not needed. This feature allows a clock to be maintained with reduced current consumption.

The settings described in the SE4120L Power Control States table for fully active operation depend on whether an external reference source or the internal crystal oscillator is used. Where an external oscillator is used to provide a reference signal to the XTAL1 pin, the fully active (external reference) mode may be used and will result in a reduction in supply current of 0.4 mA.

The RX_EN input, (pin 23), has a 1.5 MΩ pull-down resistor to GND, on-chip. This ensures that the SE4120L will put itself in standby mode (or oscillator only mode, if OSC_EN is controlled separately) when the RX_EN controller on the baseband is tri-stated to an impedance much greater than 1.5 MΩ.

The internal LNA can be disabled by connecting the LNA's Vcc supply connection, VCC_LNA (pin 1), to GND. This may be desirable in some applications, and prevents the LNA from consuming any current and will result in a reduction in supply current of approximately 1.9 mA.

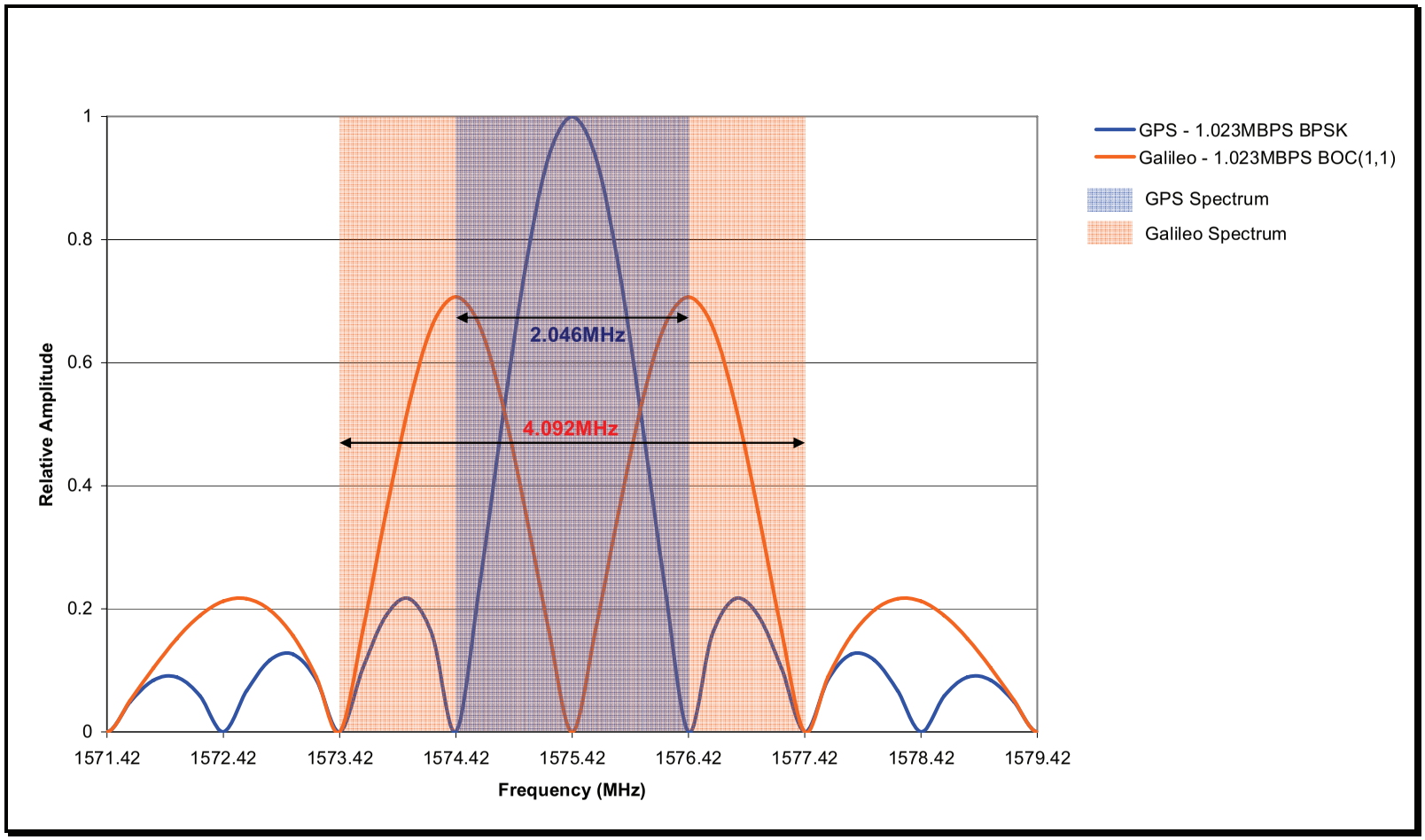
Logic Interfacing

The SE4120L logic Inputs can be controlled from an external baseband or permanently set by connecting to either VDDN (pin 8) for Logic '1', or VSSN (pin 7) for Logic '0'. The digital interface on the SE4120L, supplied from VDDN, has been designed to operate at the same voltage as the GNSS baseband across a wider voltage range than the RF sections of the device. It will accommodate the lower voltage baseband interfaces down to 1.7 V. The SE4120L logic input signals are shown in the following table:

SE4120L Logic Inputs

Pin	Name	Description	Logic
6	AGC_DIS	AGC inhibit input	'1' Hold AGC gain '0' Enable AGC
12	Fs_SEL0	Serial IF data format select (bit 0)	See table: *"Fs_SEL Hardware Configuration"*
13	Fs_SEL1	Serial IF data format select (bit 1)	
14	FILT_BW	IF Filter bandwidth select	'1' Dual-mode Galileo/GPS (4.4MHz) '0' GPS only (2.2MHz)
19	OSC_EN	Crystal oscillator enable	'1' Crystal source with osc. enabled '0' TCXO source with osc. disabled
23	RX_EN	Radio enable	'1' Enable radio '0' Standby mode

L1 Band GPS & Galileo Signal Spectra



The GPS signal is a Binary Phase-Shift Keying (BPSK) modulated spread spectrum signal with a chip rate of 1.023 MSPS.
The Galileo signal is a Binary Offset Carrier (BOC) modulated spread-spectrum signal with subcarrier at 1 MHz offset and a chip-rate of 1.023 MSPS.

Absolute Maximum Ratings

These are stress ratings only. Exposure to stresses beyond these maximum ratings may cause permanent damage to, or affect the reliability of the device. Avoid operating the device outside the recommended operating conditions defined below. This device can be damaged by electro-static discharges. Handling and assembly of this device should be at ESD protected workstations.

Symbol	Parameter	Note	Min.	Max.	Unit
V_{CC}/V_{DD}	Supply voltage	1	-0.3	+3.6	V
V_{XSS}	Voltage on any pin with respect to V_{SS}	1	-0.3	V_{DD}+0.3	V
LNA_IN_{MAX}	LNA input power	1	-	+3	dBm
ESD	Electrostatic discharge immunity (HBM)	1, 2	-	2	KV
T_{STG}	Storage temperature range	1	-40	+150	°C
T_{SLDR}	Solder reflow temperature	1	-	+260	°C

Note: (1) No damage assuming only one parameter is set at limit at a time with all other parameters set at or below the recommended operating conditions.
(2) ESD checked to the Human Body Model (HBM). A charged 100 pF capacitor discharged through a switch and 1.5 kΩ series resistor into the component.

Recommended Operating Conditions

Symbol	Parameter	Note	Min.	Max.	Unit
T_A	Ambient operating temperature	-	-40	+85	°C
V_{CC}	Main supply voltage	1	2.7	3.6	V
V_{DDN}	Digital I/O supply voltage	-	1.7	3.6	V

Note: (1) All supply pins (V_{CC}, V_{DD}) except V_{DDN} (pin 8).

DC Electrical Characteristics

Conditions: $V_{CC} = V_{DD} = 3.3$ V, $T_A = 25$ °C

Symbol	Parameter	Note	Min.	Typ.	Max.	Unit
I_{CC}	Total supply current, all circuits active	1	-	10	-	mA
$I_{CC(OSC)}$	Total supply current, receiver shut down, clock circuits only active		-	1	-	mA
$I_{CC(OFF)}$	Supply current, all circuits shut down		-	3	10	µA
$I_{CC(LNA)}$	LNA supply current		-	1.9	-	mA

Note: (1) Using on-chip crystal oscillator with CLK_OUT (pin 9), DATA_OUT (pin 10) and SYNC (pin 11) outputs unloaded.

AC Electrical Characteristics, LNA Input

Conditions: V_{CC}= V_{DD} =3.3 V, T_A =25 °C, f_{RF} = 1575.42 MHz unless otherwise stated

Symbol	Parameter	Note	Min.	Typ.	Max.	Unit
S_{21}	Forward gain	-	-	18.5	-	dB
NF_{LNA}	Noise figure	1	-	1.7	-	dB
S_{11}	Input 50 Ω return loss	1	-	7	-	dB
S_{22}	Output 50 Ω return loss, f_{RF}=1570 MHz to 1580 MHz	-	-	18	-	dB
P_{1dB}	Input power at which gain falls by 1dB	-	-	-29	-	dBm
$P_{1dBLNBLK}$	1dB GPS signal input gain compression (1575.42 MHz) in presence of CW blocking signal 1227.6 MHz (GPS L2) 824 - 849 MHz (GSM850) 880 - 915 MHz (GSM900) 1710 - 1785 MHz (DCS) 1850 - 1910 MHz (PCS) 1920 – 1980 MHz (W-CDMA) 2.4 -2.5 GHz (WLAN/Bluetooth)	2, 3	-	 -24.0 -22.7 -22.0 -22.8 -19.0 -16.2 -7.0	-	dBm
t_R	Recovery time from 0 dBm input overload signal	4	-	1.3	-	µs

Note: (1) With specified input matching network
(2) Levels do not include effects of any external RF filtering
(3) 1575.42MHz signal for blocking measurement is CW at a fixed level of -50 dBm.
(4) LNA has recovered when forward gain (S_{21}) has resettled to achieve its minimum specification limit.

AC Electrical Characteristics, Receiver

Conditions: V_{CC}= V_{DD} =3.3 V, T_A =25 °C, f_{RF} = 1575.42 MHz unless otherwise stated

Symbol	Parameter	Note	Min.	Typ.	Max.	Unit
NF_{RX_GPS}	Noise figure, f_{RF}=1570 to 1580 MHz, input to 'MIX_IN' – GPS mode	-	-	8.2	-	dB
NF_{RX_GAL}	Noise figure, f_{RF}=1570 to 1580 MHz, input to 'MIX_IN' – Galileo mode	-	-	9.8	-	dB
S_{11}	Input 50 Ω return loss, f_{RF}=1570 MHz to 1580 MHz	-	-	19	-	dB
f_{IF_ADC}	IF center frequency at input to ADC (16.368 MHz reference)	-	-	4.092	-	MHz
$f_{IF\_DATA\_OUT}$	IF center frequency at DATA_OUT	1	-	0	-	Hz
M_{IX_IR}	Mixer image rejection	2	20	40	-	dB
P_{MAX}	Maximum signal load at MIX_IN (pin 21) (for normal AGC operation)	3	-	-	-137	dBm/Hz
$P_{1dBRXBLK}$	1dB GPS signal gain compression (1575.42MHz) in presence of CW blocking signal 1227.6 MHz (GPS L2) 824 - 849 MHz (GSM850) 880 - 915 MHz (GSM900) 1710 - 1785 MHz (DCS) 1850 - 1910 MHz (PCS) 1920 – 1980 MHz (W-CDMA) 2.4 -2.5 GHz (WLAN/Bluetooth)	4, 5	-	 -36.2 -37.7 -38.0 -34.8 -33.4 -32.3 -28.0	-	dBm
t_R	Recovery time from -20 dBm Input overload signal	6	-	2	-	ms

Note: (1) Near-zero IF
(2) Ratio of level through mixer between wanted input signal at 1575.42 MHz and image signal at 1567.236MHz.
(3) The application should be designed to meet this maximum level across 1575.42 ±5 MHz. An absence of strong interferers is assumed.
(4) Levels do not include effects of any external RF filtering.
(5) 1575.42MHz signal for blocking measurement is CW at a fixed level of -101 dBm.
(6) AGC loop disabled. Receiver is deemed to have recovered when the rms signal level in the ADC has resettled to its initial value ±1.5 dB.

AC Electrical Characteristics, IF Filter – GPS Mode

Conditions: V_{CC}= V_{DD} =3.3 V, T_A =25 °C

Symbol	Parameter	Note	Min.	Typ.	Max.	Unit
f_{IF}	IF center frequency	-	-	4.092	-	MHz
BW_{GPS}	-3dB bandwidth	-	-	2.05	-	MHz
A_{RIPGPS}	Amplitude ripple , $f_C \pm 512$ kHz	-	-	0.4	-	dBpp
ΔT_{gGPS}	Group delay variation, $f_C \pm 512$ kHz	-	-	75	-	ns
Av_{2GPS}	Selectivity at $f_C \pm 2$ MHz	-	-	12	-	dB
Av_{4GPS}	Selectivity at $f_C \pm 4$ MHz	-	-	25	-	dB

AC Electrical Characteristics, IF Filter – Galileo + GPS Mode

Conditions: V_{CC}= V_{DD} =3.3 V, T_A =25 °C

Symbol	Parameter	Note	Min.	Typ.	Max.	Unit
f_{IF}	IF center frequency	-	-	4.092	-	MHz
BW_{GAL}	-3dB bandwidth	-	-	4.5	-	MHz
A_{RIPGAL}	Amplitude ripple , $f_C \pm 1.023$ MHz	-	-	1.0	-	dBpp
ΔT_{gGAL}	Group delay variation, $f_C \pm 1.023$ MHz	-	-	68	-	ns
Av_{2GAL}	Selectivity at $f_C \pm 3.5$ MHz	-	-	8	-	dB
Av_{5GAL}	Selectivity at $f_C \pm 5$ MHz	-	-	18	-	dB

AC Electrical Characteristics, VCO and Local Oscillator

Conditions: V_{CC}= V_{DD} =3.3 V, T_A =25 °C, TCXO frequency = 16.368 MHz

Symbol	Parameter	Note	Min.	Typ.	Max.	Unit
f_{LO}	LO center frequency	1	-	1571.328	-	MHz
L_{1k}	LO SSB phase noise at 1 kHz offset	-	-	-84	-65	dBc/Hz
L_{10k}	LO SSB phase noise at 10 kHz offset	-	-	-89	-65	dBc/Hz
L_{100k}	LO SSB phase noise at 100 kHz offset	-	-	-87	-80	dBc/Hz

Note: (1) VCO runs at twice the local oscillator frequency.

AC Electrical Characteristics, Crystal Oscillator

Conditions: V_{CC}= V_{DD} =3.3 V, T_A =25 °C

Symbol	Parameter	Note	Min.	Typ.	Max.	Unit
f_{XTAL}	Oscillator frequency	-	-	16.368	-	MHz
	Recommended crystal parameters					
R_X	ESR	1	-	-	80	Ω
C_{LOAD}	Load capacitance		-	10	-	pF
P_X	Drive power specification		50	-	-	µW
t_{START}	Oscillator startup time to 95% of final amplitude	-	-	2	-	ms
V_{IN}	External oscillator drive level	-	0.2	1	-	V p-p

Note: (1) Recommended crystal parameters assume a parallel, fundamental mode crystal is used.

Logic Level Characteristics

Conditions: V_{CC} = V_{DD} = 3.3 V, T_A = 25 °C

Symbol	Parameter	Note	Min.	Typ.	Max.	Unit
V_{IH}	Logic high input voltage	1	0.7V_{DDN}	-	V_{DDN}	V
V_{IL}	Logic low input voltage	1	0	-	0.3V_{DDN}	V
I_{IH}	Input current logic high voltage	1	-	200	-	nA
$I_{IH\_RX\_EN}$	Input current logic high voltage for RX_EN input (pin 23)	2	-	2.2	-	µA
I_{IL}	Input current logic low voltage	1	-	-200	-	nA
C_{ILOAD}	Input load capacitance	1	-	-	2	pF
V_{OH}	Logic high output voltage	3	V_{DDN} - 0.1V	-	V_{DDN}	V
V_{OL}	Logic low output voltage	3	0	-	0.1	V
I_{OH}	Output current logic high voltage	3, 4	-	1.45	-	mA
I_{OL}	Output current logic low voltage	3, 4	-	-1.45		mA
C_{OLOAD}	Output load capacitance	3	-	-	10	pF

Note: (1) Applies to all logic pins used as inputs: AGC_DIS (pin 6), Fs_SEL0 (pin 12), Fs_SEL1 (pin 13), FILT_BW (pin 14), OSC_EN (pin 19) and RX_EN (pin 23).
(2) Applies to RX_EN (pin 23) only. Figure dominated by 1.5 MΩ (nom.) on-chip pull-down resistor.
(3) Applies to all logic pins used as outputs: CLK_OUT (pin 9), DATA_OUT (pin 10), and SYNC (pin 11).
(4) Output current set at nominal level; no current setting resistor on RVI (pin 20). Positive value indicates current source; negative value indicates current sink.

Logic Output Current Drive Adjustment Settings

The Logic Outputs on the SE4120L can be adjusted to compensate for parasitics in application board layout. This can be achieved by adding a resistor between RVI (pin 20) and VDDQ (pin 17) as shown below.
The additional interface capacitance of PCB tracking and connectors between the SE4120L output and baseband interface input is included in these figures.
These figures are typical only and are not guaranteed across temperature and silicon process.

Conditions: V_{CC} = V_{DD} = 3.3 V, T_A = 25 °C

Current Setting Resistor Value (RVI (pin 20) to VDDQ (pin 17)) (Ω)	Maximum Allowable Capacitive Loading (pF)	Current Drive Level
Not Fitted	5	Nominal
100K	6	X 1.2
39K	7	X 1.4
0R	10	X 2.0

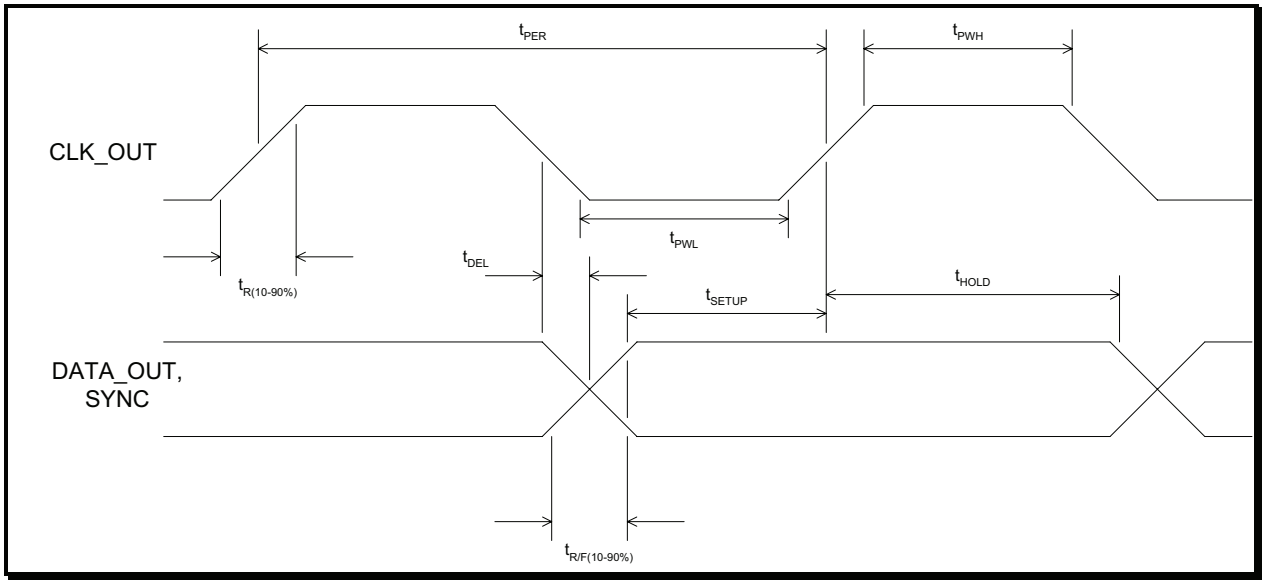
Logic Timing Characteristics

Conditions: $C_L \leq 10$ pF, $V_{CC} = V_{DD} = 3.3$ V, $T_A = 25$ °C at Maximum Buffer Current

Symbol	Parameter	Note	Min.	Typ.	Max.	Unit
t_{PER}	Clock Period	-	-	61.1	-	ns
t_{PWL}	Clock Low Width	1	10	-	-	ns
t_{PWH}	Clock High Width	1	10	-	-	ns
t_{DEL}	Clock To Data Delay Time	2	-	-	12	ns
t_{SETUP}	Setup Time	1	10	-	-	ns
t_{HOLD}	Hold Time	-	10	-	-	ns
t_R	Rise Time, 10-90%	1	-	-	17	ns
$t_{R/F}$	Rise and Fall Time, 10 - 90%	1	-	-	17	ns

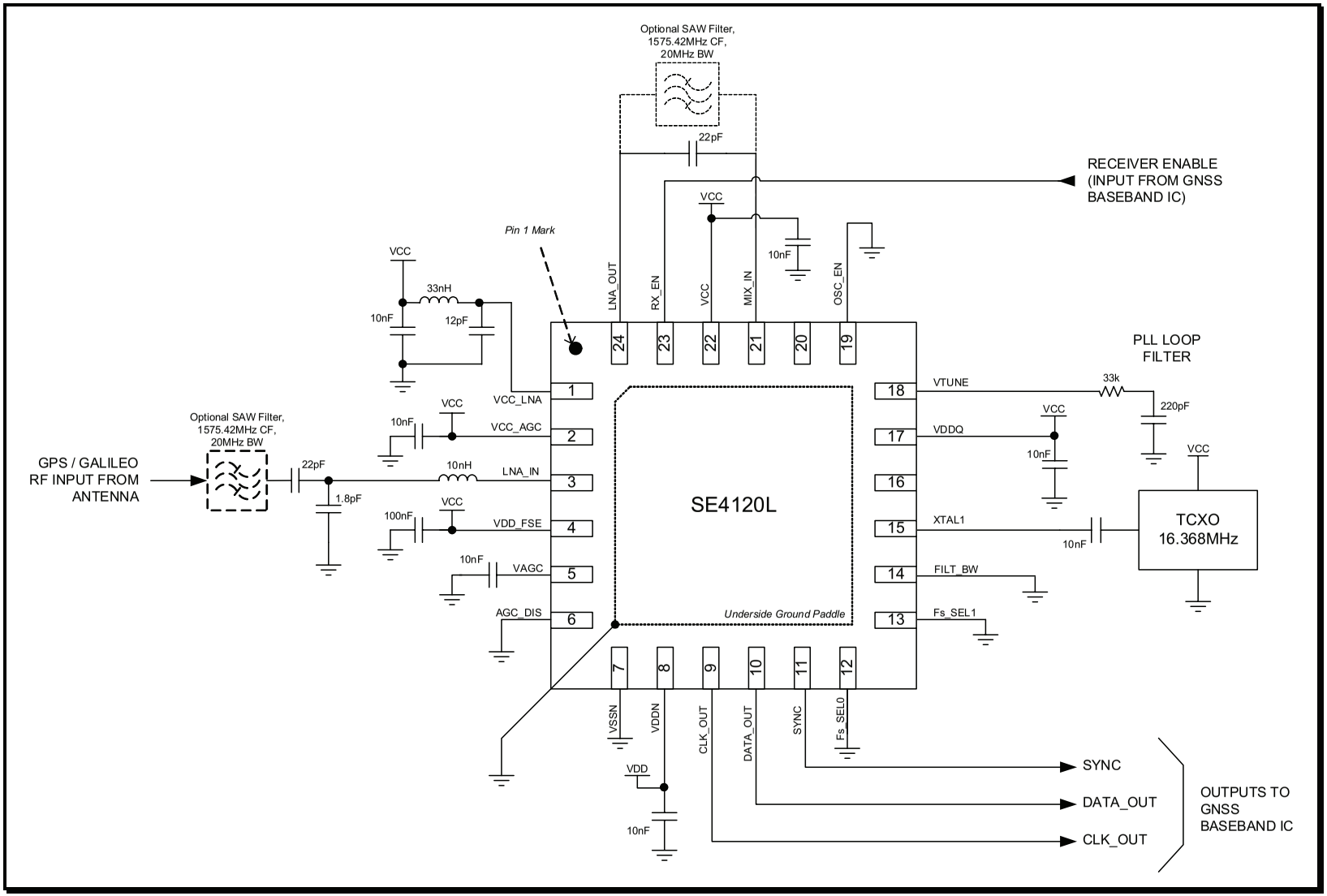
Note: (1) Values dependent on output drive set.
(2) Maximum Values dependent on load capacitance and output drive current level; determined by resistor on RVI (pin 20).

Logic Output Data Timing Diagram

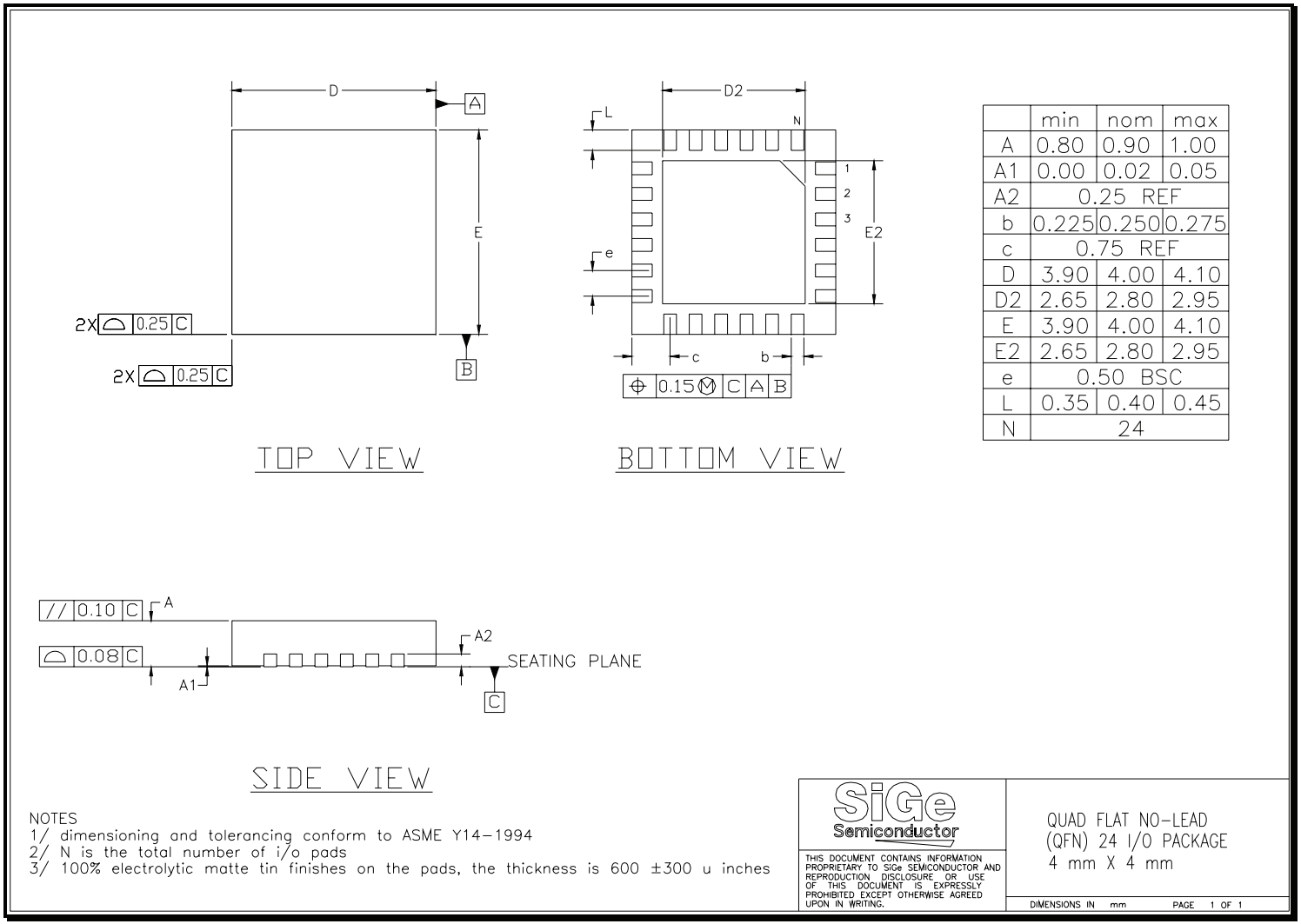


Conditions: $C_L \leq 10$ pF at Maximum Buffer Current

Typical Application Circuit Diagram



Package Information



	min	nom	max
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A2		0.25 REF	
b	0.225	0.250	0.275
c		0.75 REF	
D	3.90	4.00	4.10
D2	2.65	2.80	2.95
E	3.90	4.00	4.10
E2	2.65	2.80	2.95
e		0.50 BSC	
L	0.35	0.40	0.45
N		24	

Note: (1) This package is Pb-free and RoHS compliant. The product is rated MSL1.

Recommended PCB Footprint – PCB Metal & Solder Mask

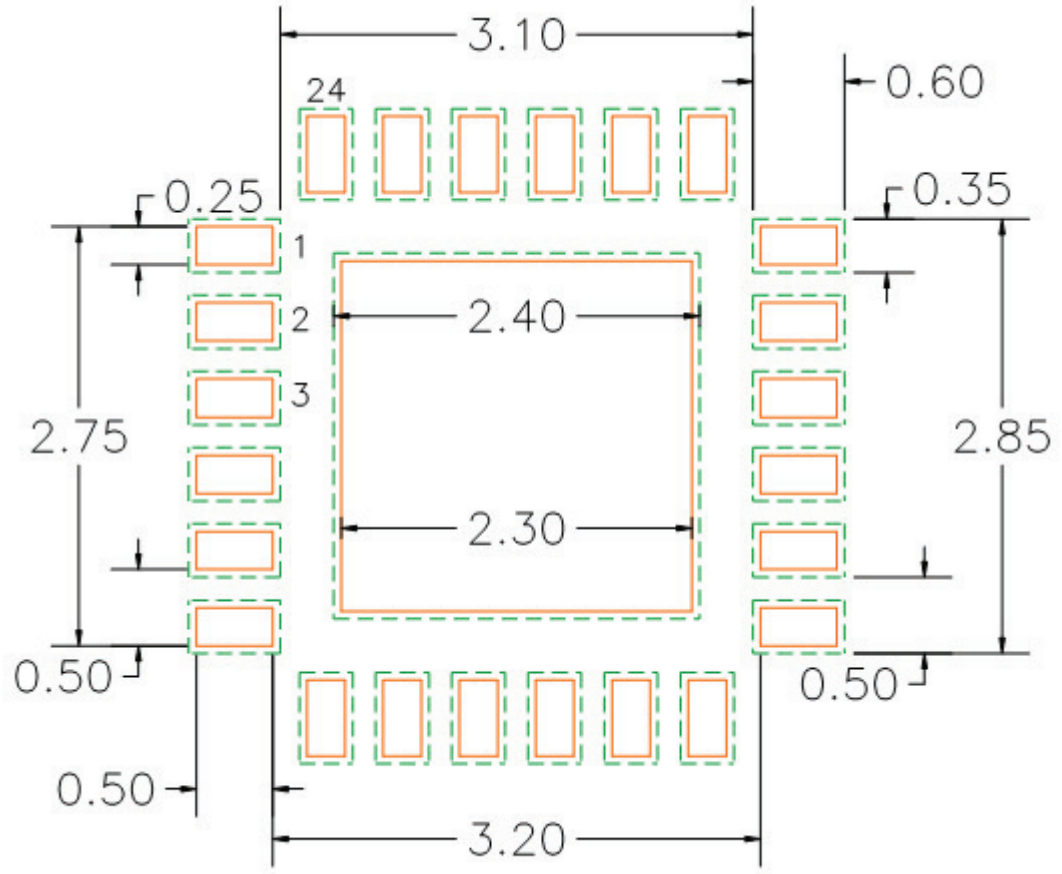
The PCB footprint below is only for reference.

This footprint is a Non-Solder Mask Defined layout [NSMD]. The dotted-green lines define the solder mask apertures. The solid-red lines define the metal pad sizes.

The user should modify the design layout in order to meet their specific solder fillet requirements & solder joint reliability requirements.

All dimensions in the figure below are in mm.

SE4120L QFN 24-pin [4x4mm] PCB Footprint



Scale 20:1 **Units in mm**

Recommended PCB Footprint – Stencil Apertures Pattern

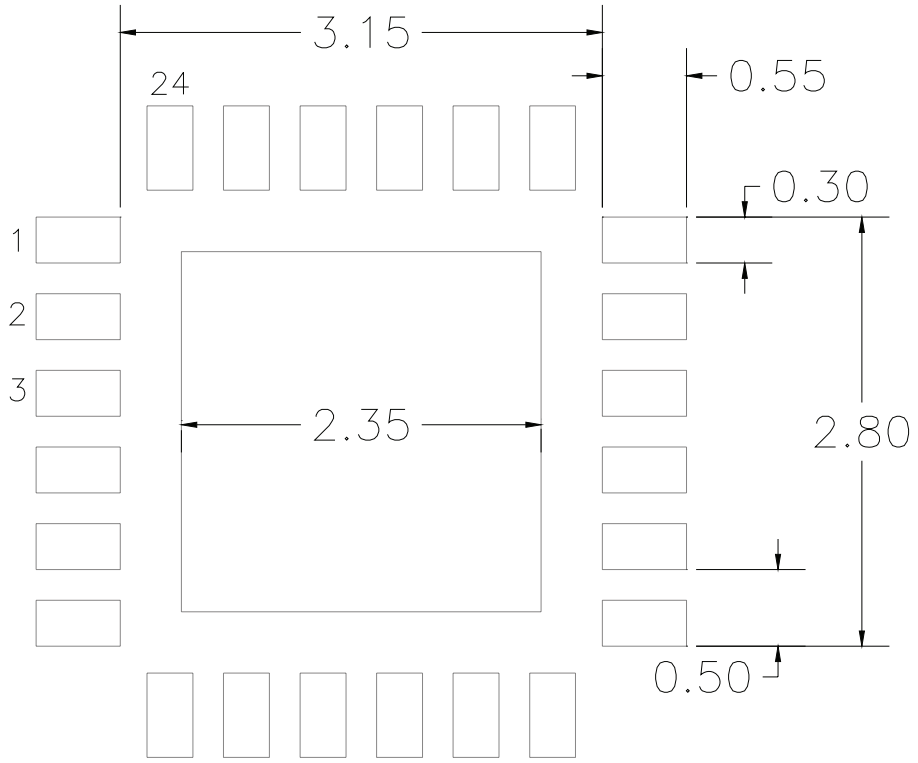
The stencil apertures design below is only for reference.

It is based on a 6 mil [0.15 mm] stencil thickness with apertures oversized by 1 mil [0.025 mm] on the pad metal.

The user should modify the design layout in order to meet their particular solder fillet & solder joint reliability requirements.

All dimensions in the figure below are in mm.

SE4120L QFN 24-pin [4x4mm] PCB Footprint – Stencil Pattern

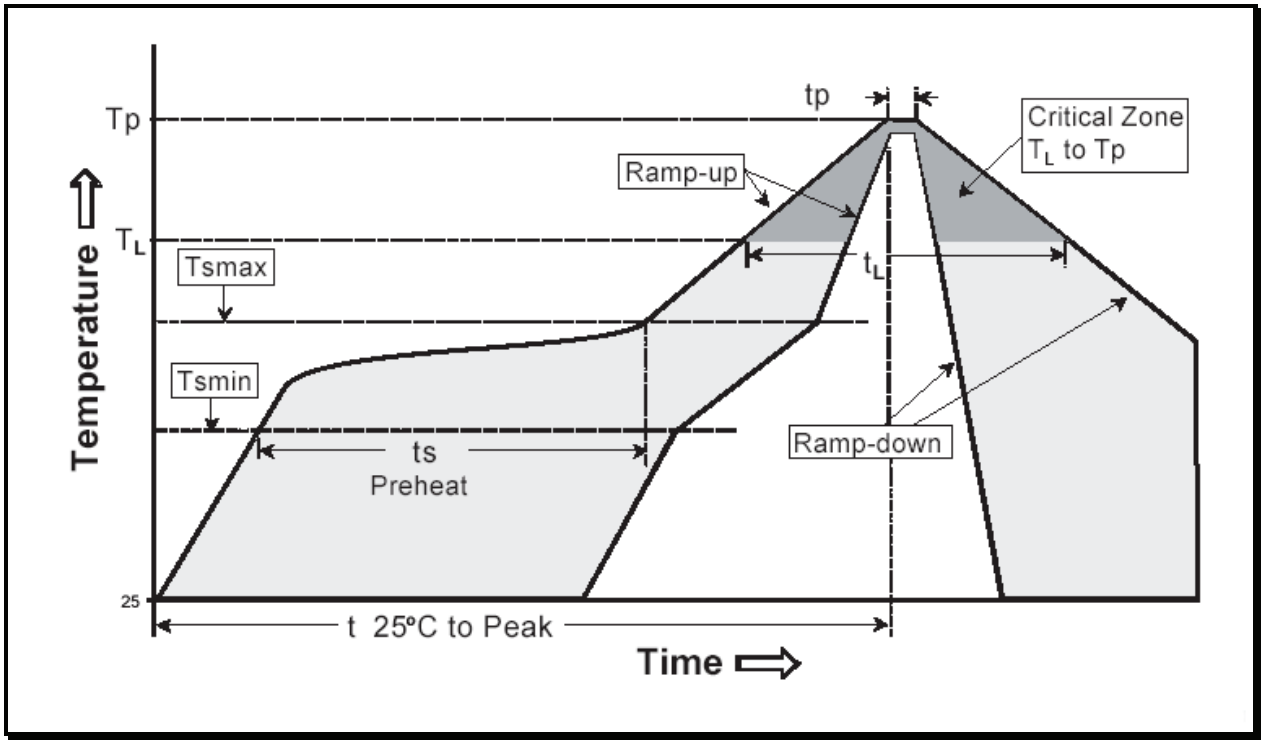


Scale 20:1 **Units in mm**

Recommended Reflow Temperature Profile

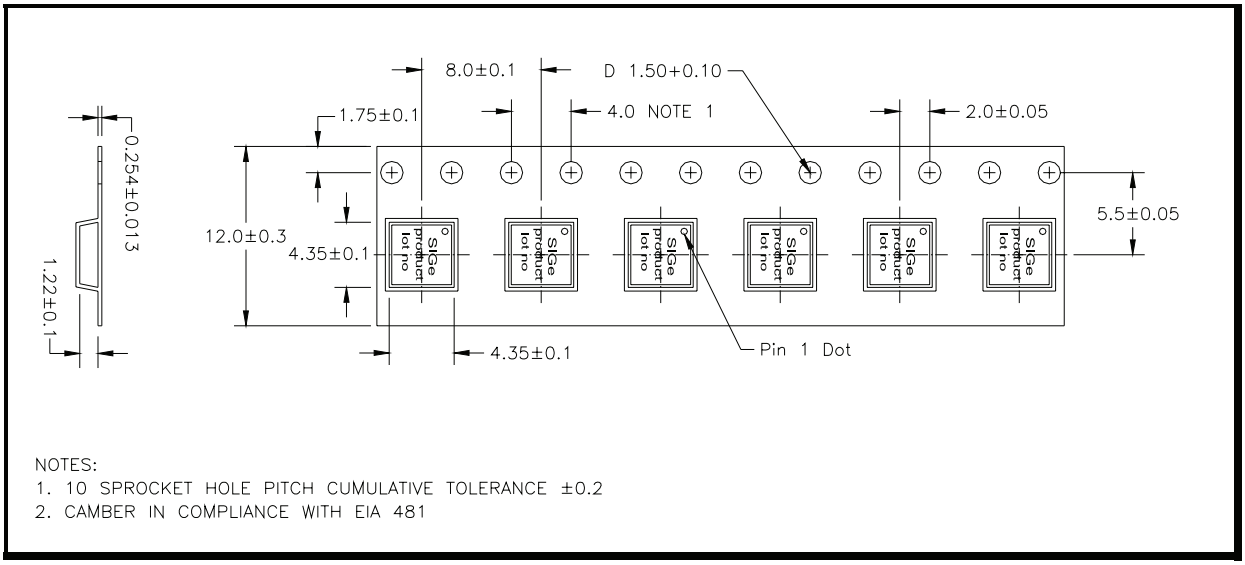
Profile Feature	SnPb Eutectic Assembly	Lead (Pb) Free Assembly
Average Ramp-up Rate (T_L to T_P)	3 °C / s (max)	3 °C / s (max)
Preheat		
Temperature Min. (T_{smin})	100 °C	150 °C
Temperature Max. (T_{smax})	150 °C	200 °C
Time (Min. to Max) (t_s)	60 - 120 s	60 - 80 s
Ramp Up		
Tsmax to t_L	-	3 °C / s (max)
Time 25°C to Peak Temperature	6 mins. (max)	8 mins. (max)
Reflow		
Temperature (t_L)	183 °C	217°C
Time maintained above t_L	60 - 150 s	60 - 150 s
Peak Temperature (t_p)	240 ±5 °C	260 +0/-5 °C
Time Within 5°C of Actual Peak Temperature (t_p)	10 - 30 s	20 - 40 s
Ramp-Down		
Ramp-Down Rate	6 °C / s (max)	6 °C / s (max)

Reflow Profile (Reference JEDEC J-STD-020)



Tape and Reel Information

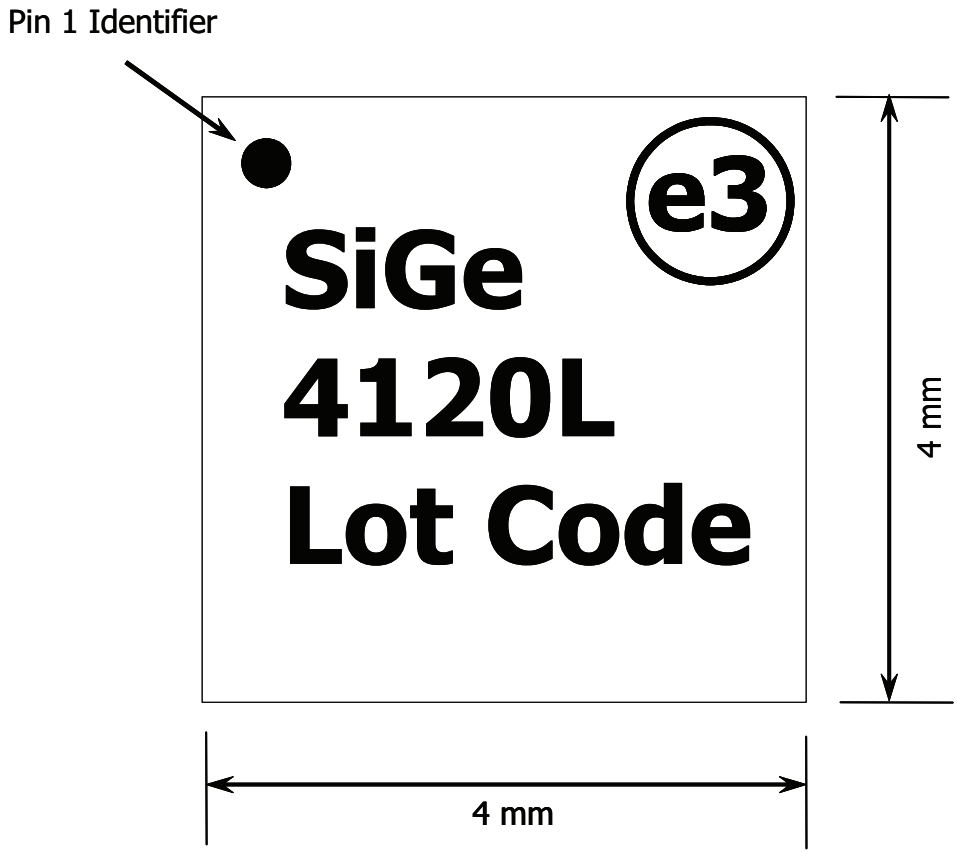
Parameter	Value
Devices Per Reel	3000
Reel Diameter	13 inches
Tape Width	12 millimeters



NOTES:
1. 10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE ±0.2
2. CAMBER IN COMPLIANCE WITH EIA 481

Branding Information

SE4120L TOP MARK [4x4mm]



e3 = JEDEC Pb-free finish designation

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