

TPS793xxYEQEVM

Evaluation Module

User's Guide

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the specified input and output ranges described in the EVM User's Guide.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 60°C. The EVM is designed to operate properly with certain components above 60°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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Preface

Read This First

About This Manual

This user's guide describes the characteristics, operation, and use of the TPS793xxYEQEVM low drop-out (LDO) evaluation module (EVM). This EVM features a TI LDO that offers ultra low noise performance with high PSRR, and 200mA load current capability all in the chip-scale package. This user's guide includes setup instructions, a schematic diagram, a bill of materials (BOM), and PCB layout drawings for the evaluation module.

How to Use This Manual

This document contains the following chapters:

- ☐ Chapter 1 – Introduction
- ☐ Chapter 2 – Setup
- ☐ Chapter 3 – Board Layout
- ☐ Chapter 4 – Schematic and Bill of Materials

Related Documentation From Texas Instruments

The following documents provide information regarding the TPS793xxYEQ EVM. These documents are available from the TI web site. The last character of the literature number corresponds to the document revision, which is current at the time of the writing of this User's Guide. Newer revisions may be available from the TI web site at <http://www.ti.com/> or call the Texas Instruments Literature Response Center at (800) 477-8924 or the Product Information Center at (972) 644-5580. When ordering, identify the item(s) by both title and literature number.

Data sheets	Literature number
TPS793xxYEQ Data Sheet	SLVS348
Wafer Chip-Scale Package Design Guide	SBVA016

If You Need Assistance

If you have questions regarding either the use of this evaluation module or the information contained in this documentation, please contact your local TI sales representative.

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Introduction

The Texas Instruments TPS793xxYEQEVM evaluation module (EVM) helps designers evaluate the operation and performance of the TPS793 family of devices in the chip-scale package. These devices are ultra low noise, high PSRR low drop-outs (LDOs) suitable for RF applications.

This EVM is specifically designed and optimized to operate over the entire input voltage range of the TPS793xxYEQ LDO (2.7V to 5.5V). The default output voltage of this EVM is denoted by the checkbox on the back of the printed circuit board. The layout of this board can be used as a starting point for designs using the TPS793xxYEQ.

Setup

This chapter describes the jumpers and connectors on the EVM as well as how to properly connect, set up, and use the TPS793xxYEQEVM.

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2.1 Input/Output Connector Descriptions

2.1.1 J1 – VIN

This is the positive connection to the input power supply. For best performance this connection should have low inductance and be driven by a low-impedance source.

2.1.2 J2 – GND

This is the return connection for the input power supply.

2.1.3 J3 – VOUT

This is the positive connection from the output of the low dropout regulator. Connect this pin to the positive input of the load.

2.1.4 J4 – GND

This is the negative connection from the output of the low dropout regulator. Connect this pin to the negative input of the load.

2.1.5 J5 – EN

This jumper enables and disables the LDO output. Connecting EN to ON enables the device, while connecting EN to OFF disables the device.

2.2 Set-Up

Connect an input supply between J1 and J2. The voltage range on this supply should not exceed 5.5V. The load should be connected between J4 and J5. To enable the device, configure J3 so that the ON terminal is shorted to the EN terminal with the provided terminal post.

2.3 Operation

This EVM has been optimized to operate over the entire input voltage range of the TPS793xxYEQ LDO (2.7V to 5.5V). The output is a low-noise source capable of supplying 200mA. Only input and output ceramic capacitors are required for the LDO to function; however, an optional bypass capacitor is connected to BYP to further reduce output noise.

Printed Circuit Board Layout

This chapter provides the TPS793xxYEQEVM printed circuit board layout and illustrations.

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3.1 Layout

Board layout is critical for reliable and easy to assemble chip-scale designs. Figure 3–1, Figure 3–2, and Figure 3–3 show the board layout for the TPS793xxYEQEVM printed wiring board (PWB). Careful attention should be given to the routing to the chip-scale IC lands. Refer to the NanoStar™ Wafer Chip-Scale Package Design Guide for specific layout guidelines.

Figure 3–1. Assembly Layer

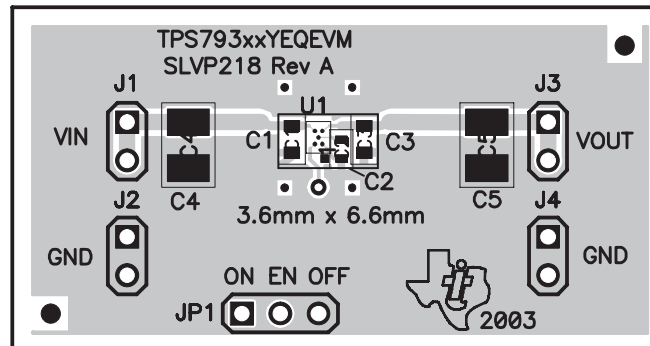


Figure 3–2. Top Layer Routing

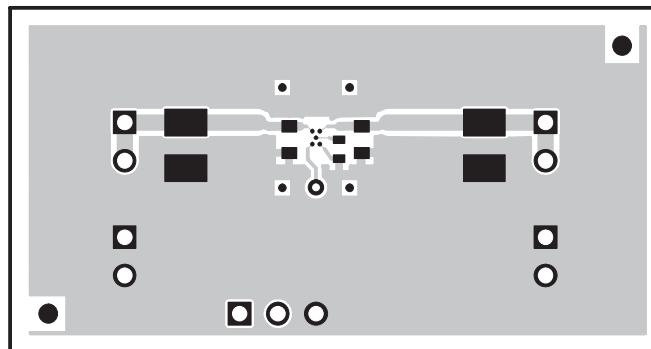
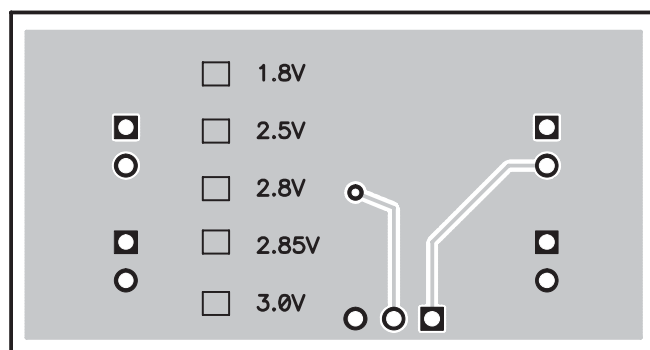


Figure 3–3. Bottom Layer Routing



Schematic and Bill of Materials

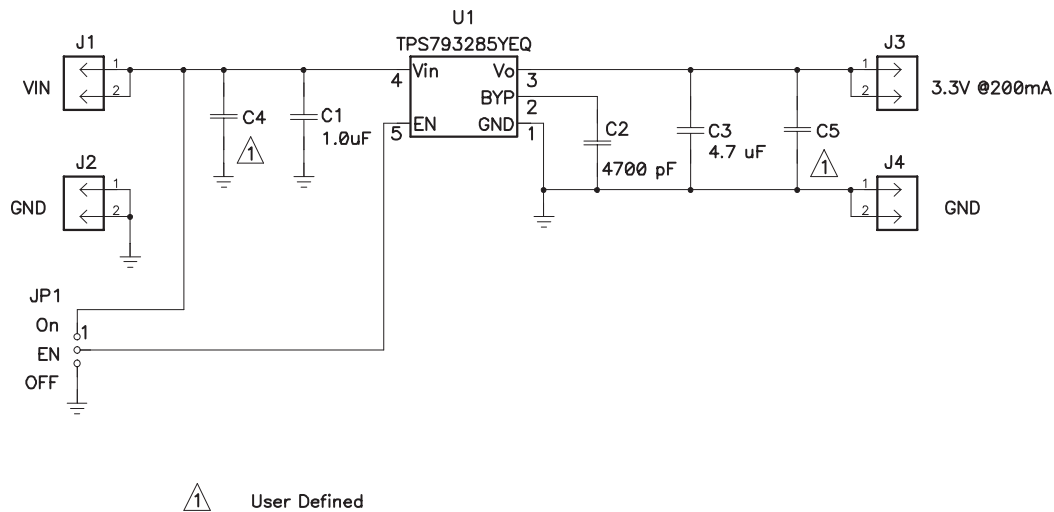
This chapter provides the schematic for the TPS793xxYEQVM. The bill of materials is also included for component and manufacturer reference.

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4.1 Schematic

The complete electrical schematic for the TPS793xxYEQEVM is shown in Figure 4-1.

Figure 4-1. TPS793xxYEQEVM Schematic Diagram



4.2 Bill of Materials

Table 4-1. Bill of Materials

Count	Reference Designator	Description	Size	Manufacturer	Mfg Part Number
1	C1	Capacitor, ceramic, 1.0µF, 10V, X5R, 10%	603	TDK	C1608X5R1A105KT
1	C2	Capacitor, 4700pF, 50V, X7R, 10%,	402	TDK	C1005X7R1H472KT
1	C3	Capacitor, ceramic, 4.7µF, 6.3V, X5R, 10%	603	TDK	C1608X5R0J475KT
0	C4, C5	Capacitor, ceramic, xxxµF, 6.3V	1210		
4	J1, J2, J3, J4	Header, 2-pin, 100 mil spacing (36-pin strip)		Sullins	PTC36SAAN
1	JP1	Header, 3-pin, 100 mil spacing (36-pin strip)		Sullins	PTC36SAAN
1	U1	IC, Ultralow-Noise, Fast RF 200 mA, LDO Regulator		Texas Instruments	TPS793xxYEQ
1		PC Board, 1.700 in. x .900 in. x .062 in.		Any	SLVP218
1		Shunt, 100 mil (black)		3M	929950-00