



## LMC567 Low-Power Tone Decoder

### 1 Features

- Functionally Similar to LM567
- 2-V to 9-V Supply Voltage Range
- Low Supply Current Drain
- No Increase in Current With Output Activated
- Operates to 500-kHz Input Frequency
- High Oscillator Stability
- Ground-Referenced Input
- Hysteresis Added to Amplitude Comparator
- Out-of-Band Signals and Noise Rejected
- 20-mA Output Current Capability

### 2 Applications

- Touch-Tone Decoding
- Precision Oscillators
- Frequency Monitoring and Control
- Wide-Band FSK Demodulation
- Ultrasonic Controls
- Carrier Current Remote Controls
- Communications Paging Decoders

### 3 Description

The LMC567 device is a low-power, general-purpose LMCMOS tone decoder which is functionally similar to the industry standard LM567. The device consists of a twice frequency voltage-controlled oscillator (VCO) and quadrature dividers which establish the reference signals for phase and amplitude detectors.

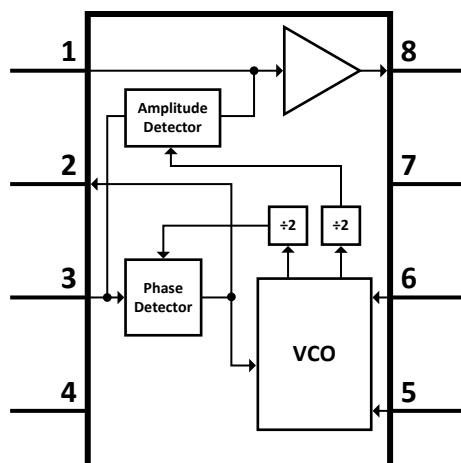
The phase detector and VCO form a phase-locked loop (PLL) which locks to an input signal frequency which is within the control range of the VCO. When the PLL is locked and the input signal amplitude exceeds an internally pre-set threshold, a switch to ground is activated on the output pin. External components set up the oscillator to run at twice the input frequency and determine the phase and amplitude filter time constants.

#### Device Information <sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LMC567	SOIC (8)	4.90 mm x 3.91 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

#### Simplified Diagram



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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

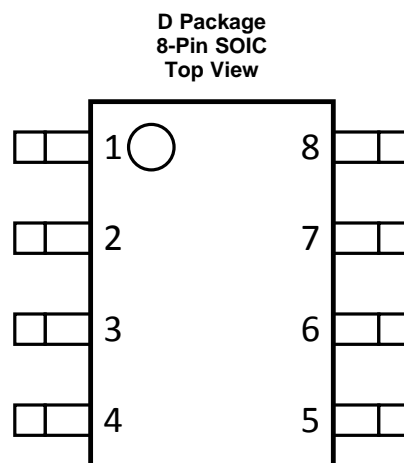
Changes from Revision B (April 2013) to Revision C	Page
<ul style="list-style-type: none"> <li>Added <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> section, <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section. ....</li> </ul>	<b>1</b>

Changes from Revision A (April 2013) to Revision B	Page
<ul style="list-style-type: none"> <li>Changed layout of National Data Sheet to TI format .....</li> </ul>	<b>9</b>

## 5 Device Comparison Table

DEVICE NUMBER	DESCRIPTION
LMC567	Low power tone decoder
LM567, LM567C	General-purpose tone decoder with half oscillator frequency than LMC567

## 6 Pin Configuration and Functions



**Pin Functions**

PIN		TYPE <sup>(1)</sup>	DESCRIPTION
NAME	NO.		
GND	7	PWR	Ground connection
IN	3	I	Device input
LF_CAP	2	I	Loop filter capacitor terminal
OF_CAP	1	I	Output filter capacitor terminal
OUT	8	O	Device output
T_CAP	5	I	Timing capacitor connection terminal
T_RES	6	I	Timing resistor connection terminal
VCC	4	PWR	Voltage supply connection

(1) I = input, O = output, PWR = power

## 7 Specifications

### 7.1 Absolute Maximum Ratings

 over operating free-air temperature range (unless otherwise noted)<sup>(1)(2)</sup>

		MIN	MAX	UNIT
Input voltage	IN	2		V <sub>P-P</sub>
Supply voltage	VCC		10	V
Output voltage	OUT		13	V
Output current	OUT		30	mA
Package dissipation			500	mW
Operating temperature, T <sub>A</sub>		–25	125	°C
Storage temperature, T <sub>stg</sub>		–55	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.

### 7.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	2	9	V
F <sub>IN</sub>	Input frequency	1	500	Hz
T <sub>A</sub>	Operating temperature	–25	125	°C

### 7.3 Thermal Information

THERMAL METRIC <sup>(1)</sup>		LMC567	UNIT
		D (SOIC)	
		8 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	111.8	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	59.2	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	52.2	°C/W
Ψ <sub>JT</sub>	Junction-to-top characterization parameter	13.5	°C/W
Ψ <sub>JB</sub>	Junction-to-board characterization parameter	51.7	°C/W

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

### 7.4 Electrical Characteristics

 Test Circuit, T<sub>A</sub> = 25°C, V<sub>s</sub> = 5 V, RtCt #2, Sw. 1 Pos. 0, and no input, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I <sub>4</sub>	Power supply current	RtCt #1, quiescent or activated	V <sub>s</sub> = 2 V		0.3		mAdc
			V <sub>s</sub> = 5 V		0.5	0.8	
			V <sub>s</sub> = 9 V		0.8	1.3	
V <sub>3</sub>	Input D.C. bias				0		mVdc
R <sub>3</sub>	Input resistance				40		kΩ
I <sub>8</sub>	Output leakage				1	100	nAdc
f <sub>0</sub>	Center frequency, F <sub>osc</sub> ÷ 2	RtCt #2, measure oscillator Frequency and divide by 2	V <sub>s</sub> = 2 V		98		kHz
			V <sub>s</sub> = 5 V	92	103	113	
			V <sub>s</sub> = V		105		
Δf <sub>0</sub>	Center frequency shift with supply	$\frac{f_{0 9V} - f_{0 2V}}{7 f_{0 5V}} \times 100$			1	2	%/V

(1)

## Electrical Characteristics (continued)

Test Circuit,  $T_A = 25^\circ\text{C}$ ,  $V_s = 5\text{ V}$ , RtCt #2, Sw. 1 Pos. 0, and no input, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{in}$	Input threshold	Set input frequency equal to $f_0$ measured above. Increase input level until pin 8 goes low.	$V_s = 2\text{ V}$	11	20	27	mVrms
			$V_s = 5\text{ V}$	17	30	45	
			$V_s = 9\text{ V}$		45		
$\Delta V_{in}$	Input hysteresis	Starting at input threshold, decrease input level until pin 8 goes high.			1.5		mVrms
$V_8$	Output sat voltage	Input level > threshold Choose RL for specified I8.	I8 = 2 mA		0.06	0.15	Vdc
			I8 = 20 mA		0.7		
L.D.B.W.	Largest detection bandwidth	Measure $F_{osc}$ with Sw. 1 in Pos. 0, 1, and 2; $\text{L.D.B.W.} = \frac{F_{osc P2} - F_{osc P1}}{F_{osc P0}} \times 100 \quad (2)$	$V_s = 2\text{ V}$	7%	11%	15%	
			$V_s = 5\text{ V}$	11%	14%	17%	
			$V_s = 9\text{ V}$		15%		
$\Delta BW$	Bandwidth skew	$\text{Skew} = \left( \frac{F_{osc P2} - F_{osc P1}}{2 F_{osc P0}} - 1 \right) \times 100 \quad (3)$			0%	$\pm 1.0\%$	
$f_{max}$	Highest center frequency	RtCt #3 Measure oscillator frequency and divide by 2.			700		kHz
$V_{in}$	Input threshold at $f_{max}$	Set input frequency equal to $f_{max}$ measured above. Increase input level until pin 8 goes low.			35		mVrms

## 7.5 Typical Characteristics

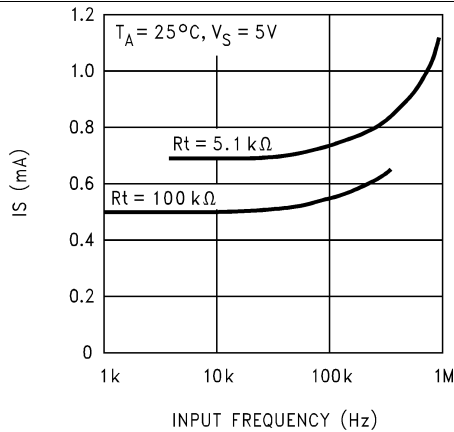


Figure 1. Supply Current vs Operating Frequency

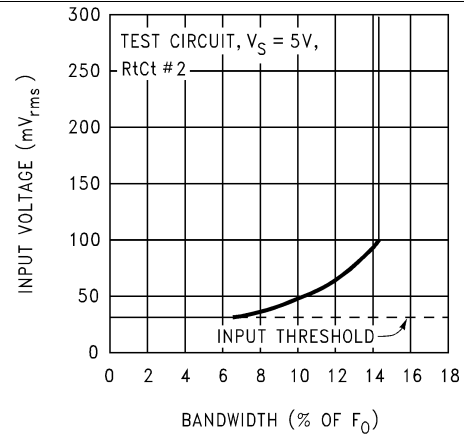


Figure 2. Bandwidth vs Input Signal Level

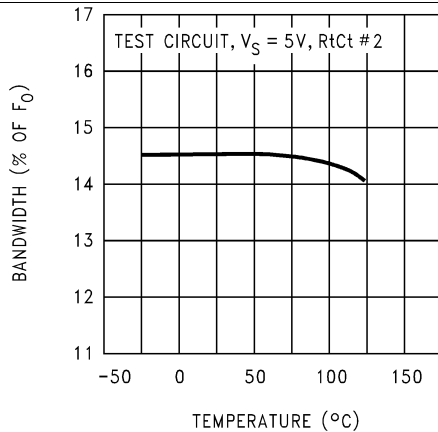


Figure 3. Largest Detection Bandwidth vs Temperature

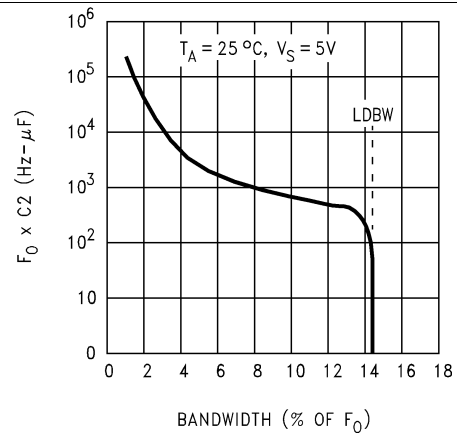


Figure 4. Bandwidth as a Function of C2

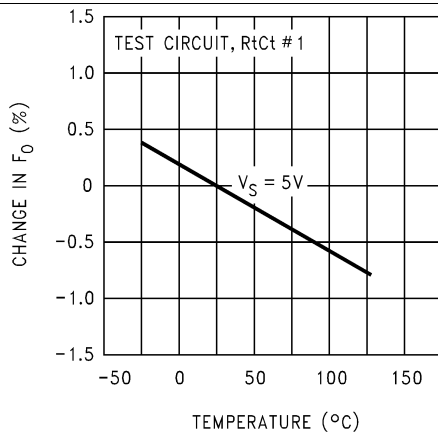


Figure 5. Frequency Drift With Temperature

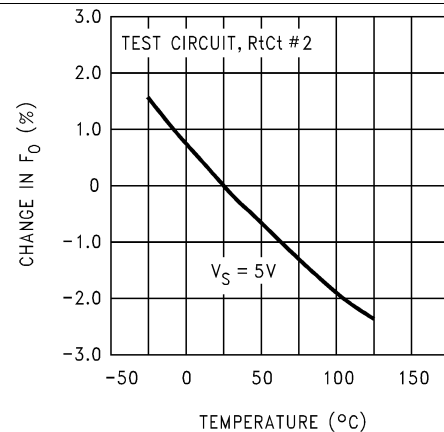


Figure 6. Frequency Drift With Temperature

## 8 Parameter Measurement Information

All parameters are measured according to the conditions described in [Specifications](#).

### 8.1 Test Circuit

Figure 7 was used to make the measurements of the typical characteristics of the LMC567.

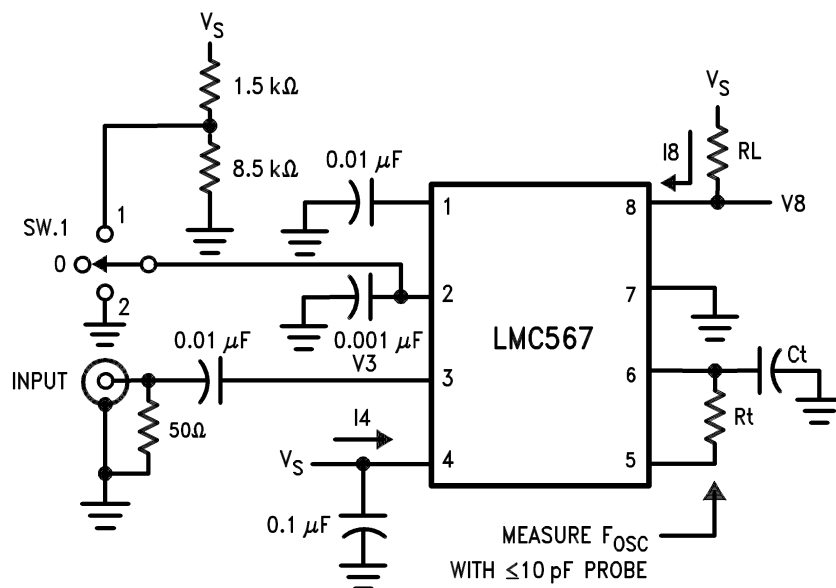


Figure 7. LMC567 Test Circuit

Table 1. R<sub>t</sub> and C<sub>t</sub> Values for the Test Circuit

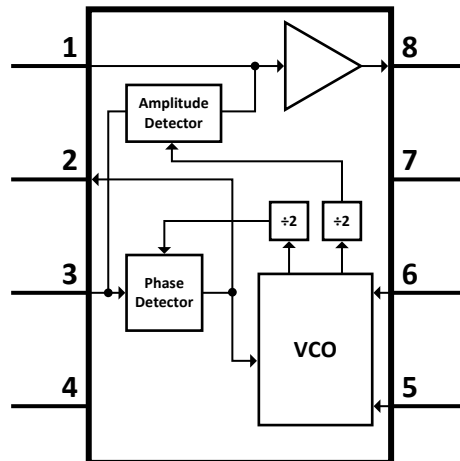
R <sub>t</sub> C <sub>t</sub>	R <sub>t</sub>	C <sub>t</sub>
#1	100k	300 pF
#2	10k	300 pF
#3	5.1k	62 pF

## 9 Detailed Description

### 9.1 Overview

The LMC567C is a low-power, general-purpose tone decoder with similar functionality to the industry standard LM567. The device requires external components set up the internal oscillator to run at twice the input frequency and determine the required filter constants. Internal VCO and Phase detector form a Phase-locked loop which locks to an input signal frequency that is established by external timing components. When PLL is locked, a switch to ground is activated in the output of the device.

### 9.2 Functional Block Diagram



### 9.3 Feature Description

#### 9.3.1 Oscillator

The voltage-controlled oscillator (VCO) on the LMC567 must be set up to run at twice the frequency of the input signal tone to be decoded. The center frequency of the VCO is set by timing resistor  $R_t$  and timing capacitor  $C_t$  connected to pins 5 and 6 of the IC. The center frequency as a function of  $R_t$  and  $C_t$  is given by [Equation 4](#):

$$F_{OSC} \cong \frac{1}{1.4 R_t C_t} \text{ Hz} \quad (4)$$

Because this causes an input tone of half  $F_{OSC}$  to be decoded by [Equation 5](#),

$$F_{INPUT} \cong \frac{1}{2.8 R_t C_t} \text{ Hz} \quad (5)$$

[Equation 5](#) is accurate at low frequencies; however, above 50 kHz ( $F_{OSC} = 100$  kHz), internal delays cause the actual frequency to be lower than predicted.

The choice of  $R_t$  and  $C_t$  is a tradeoff between supply current and practical capacitor values. An additional supply current component is introduced in [Equation 6](#) due to  $R_t$  being switched to  $V_s$  every half cycle to charge  $C_t$ :

$$I_s \text{ due to } R_t = V_s / (4R_t) \quad (6)$$

Thus the supply current can be minimized by keeping  $R_t$  as large as possible (see [Figure 1](#)). However, the desired frequency dictates an  $R_t C_t$  product such that increasing  $R_t$  requires a smaller  $C_t$ . Below  $C_t = 100$  pF, circuit board stray capacitances begin to play a role in determining the oscillation frequency which ultimately limits the minimum  $C_t$ .

To allow for IC and component value tolerances, the oscillator timing components requires a trim. This is generally accomplished by using a variable resistor as part of  $R_t$ , although  $C_t$  could also be padded. The amount of initial frequency variation due to the LMC567 itself is given in the [Electrical Characteristics](#); the total trim range must also accommodate the tolerances of  $R_t$  and  $C_t$ .



## Feature Description (continued)

### 9.3.2 Input

The input pin 3 is internally ground-referenced with a nominal 40-k $\Omega$  resistor. Signals which are already centered on 0 V may be directly coupled to pin 3; however, any DC potential must be isolated through a coupling capacitor. Inputs of multiple LMC567 devices can be paralleled without individual DC isolation.

### 9.3.3 Loop Filter

Pin 2 is the combined output of the phase detector and control input of the VCO for the phase-locked loop (PLL). Capacitor C2 in conjunction with the nominal 80-k $\Omega$  pin 2 internal resistance forms the loop filter.

For small values of C2, the PLL has a fast acquisition time and the pull-in range is set by the built in VCO frequency stops, which also determines the largest detection bandwidth (LDBW). Increasing C2 results in improved noise immunity at the expense of acquisition time, and the pull-in range begins to become narrower than the LDBW (see [Figure 4](#)). However, the maximum hold-in range always equal the LDBW.

### 9.3.4 Output Filter

Pin 1 is the output of a negative-going amplitude detector which has a nominal 0 signal output of  $7/9 V_s$ . When the PLL is locked to the input, an increase in signal level causes the detector output to move negative. When pin 1 reaches  $2/3 V_s$ , the output is activated (see [Output](#)).

Capacitor C1 in conjunction with the nominal 40-k $\Omega$  pin 1 internal resistance forms the output filter. The size of C1 is a tradeoff between slew rate and carrier ripple at the output comparator. Low values of C1 produce the least delay between the input and output for tone burst applications, while larger values of C1 improve noise immunity.

Pin 1 also provides a means for shifting the input threshold higher or lower by connecting an external resistor to supply or ground. However, reducing the threshold using this technique increases sensitivity to pin 1 carrier ripple and also results in more part to part threshold variation.

### 9.3.5 Output

The output at pin 8 is an N-channel FET switch to ground which is activated when the PLL is locked and the input tone is of sufficient amplitude to cause pin 1 to fall below  $2/3 V_s$ . Apart from the obvious current component due to the external pin 8 load resistor, no additional supply current is required to activate the switch. The ON-resistance of the switch is inversely proportional to supply; thus the *sat* voltage for a given output current increases at lower supplies.

## 9.4 Device Functional Modes

### 9.4.1 Operation as LM567

The LMC567 low power tone decoder can be operated at supply voltages of 2 V to 9 V and at input frequencies ranging from 1 Hz up to 500 kHz.

The LMC567 can be directly substituted in most LM567 applications with the following provisions:

1. Oscillator timing capacitor Ct must be halved to double the oscillator frequency relative to the input frequency (see [Oscillator](#)).
2. Filter capacitors C1 and C2 must be reduced by a factor of 8 to maintain the same filter time constants.
3. The output current demanded of pin 8 must be limited to the specified capability of the LMC567.



## 10.2.2 Detailed Design Procedure

### 10.2.2.1 Timing Components

As VCO frequency ( $F_{OSC}$ ) runs at twice the frequency of the input tone, the desired input detection frequency can be defined by [Equation 7](#):

$$F_{INPUT} = 2 F_{OSC} \quad (7)$$

The central frequency of the oscillator is set by timing capacitor and resistor. The timing capacitor value ( $C_T$ ) must be set in order to calculate the timing resistor value ( $R_T$ ). This is given by [Equation 8](#):

$$R_T \approx \frac{1}{1.4 F_{OSC} C_T} \quad (8)$$

So, in order to found the required component values to set the detection frequency [Equation 9](#):

$$R_T \approx \frac{1}{2.8 F_{INPUT} C_T} \quad (9)$$

This approximation is valid with lower frequencies; considerations must be taken when using higher frequencies. More information on this can be found in [Oscillator](#).

### 10.2.2.2 Bandwidth

Detection bandwidth is represented as a percentage of  $F_{OSC}$ . It can be approximated as a function of  $F_{OSC} \times C_2$  following the behavior indicated in [Figure 4](#). More information on this can be found in [Loop Filter](#).

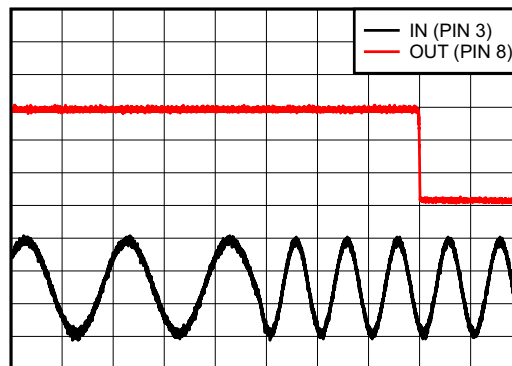
### 10.2.2.3 Output Filter

The size of the output filter capacitor  $C_1$  is a tradeoff between slew rate and carrier ripple. More information on this can be found in [Output Filter](#).

### 10.2.2.4 Supply Decoupling

The decoupling of supply pin 4 becomes more critical at high supply voltages with high operating frequencies, requiring  $C_4$  to be placed as close as possible to pin 4.

## 10.2.3 Application Curve



**Figure 9. Frequency Detection**

## 11 Power Supply Recommendations

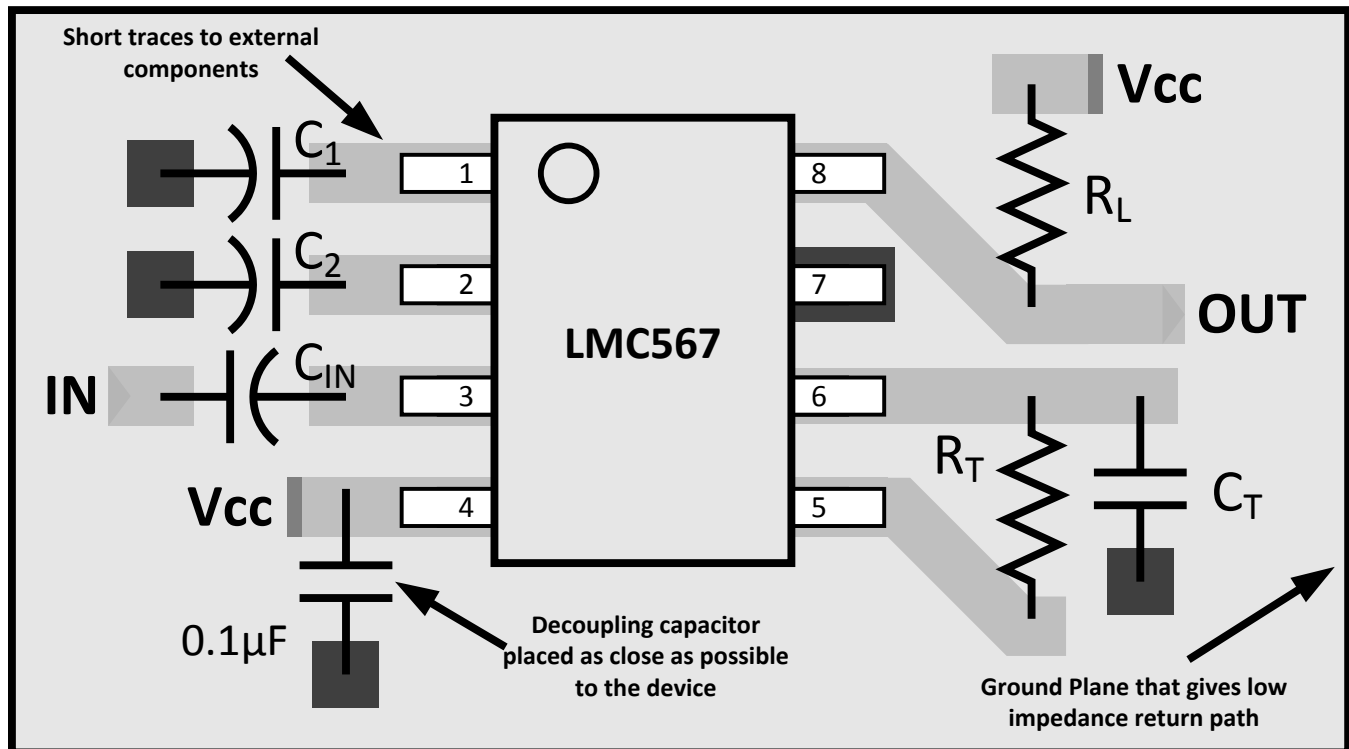
The LMC567 is designed to operate with an input power supply range between 2 V and 9 V. Therefore, the output voltage range of power supply must be within this range and well regulated. The current capability of upper power must not exceed the maximum current limit of the power switch. Because the operating frequency of the device could be very high for some applications, the decoupling of power supply becomes critical, so is required to place a proper decoupling capacitor as close as possible to VCC pin. Low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1  $\mu\text{F}$ , is typically used. This capacitor must be placed within 2 mm of the supply pin.

## 12 Layout

### 12.1 Layout Guidelines

The VCC pin of the LMC567 must be decoupled to ground plane as the device can work with high switching speeds. The decoupling capacitor must be placed as close as possible to the device. Traces length for the timing and external filter components must be kept at minimum in order to avoid any possible interference from other close traces.

### 12.2 Layout Example



Top Layer Ground Plane



Top Layer Traces



Pad to Top Layer Ground Plane



Connection to Power Supply

**Figure 10. LMC567 Board Layout**

## 13 Device and Documentation Support

### 13.1 Device Support

#### 13.1.1 Development Support

For development support, see the following:

[support.ti.com](http://support.ti.com)

### 13.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](http://e2e.ti.com), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 13.3 Trademarks

E2E is a trademark of Texas Instruments.  
All other trademarks are the property of their respective owners.

### 13.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 13.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">LMC567CMX/NOPB</a>	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-25 to 100	LMC 567CM
LMC567CMX/NOPB.A	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-25 to 100	LMC 567CM
LMC567CMX/NOPB.B	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-25 to 100	LMC 567CM

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMC567CMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMC567CMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0



**D0008A****PACKAGE OUTLINE****SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

**NOTES:**

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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