



# STE70NM50

## N-CHANNEL 500V - 0.045Ω - 70A ISOTOP Zener-Protected MDmesh™ Power MOSFET

TYPE	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>
STE70NM50	500V	< 0.05Ω	70 A

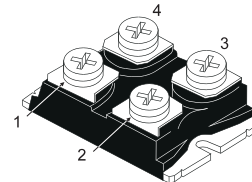
- TYPICAL R<sub>DS(on)</sub> = 0.045Ω
- HIGH dv/dt AND AVALANCHE CAPABILITIES
- IMPROVED ESD CAPABILITY
- LOW INPUT CAPACITANCE AND GATE CHARGE
- LOW GATE INPUT RESISTANCE
- TIGHT PROCESS CONTROL
- INDUSTRY'S LOWEST ON-RESISTANCE

### DESCRIPTION

The MDmesh™ is a new revolutionary MOSFET technology that associates the Multiple Drain process with the Company's PowerMESH™ horizontal layout. The resulting product has an outstanding low on-resistance, impressively high dv/dt and excellent avalanche characteristics. The adoption of the Company's proprietary strip technique yields overall dynamic performance that is significantly better than that of similar competition's products.

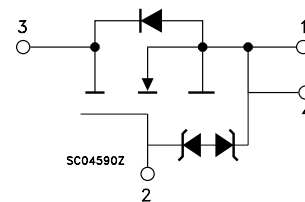
### APPLICATIONS

The MDmesh™ family is very suitable for increasing power density of high voltage converters allowing system miniaturization and higher efficiencies.



ISOTOP

### INTERNAL SCHEMATIC DIAGRAM



### ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V <sub>DS</sub>	Drain-source Voltage (V <sub>GS</sub> = 0)	500	V
V <sub>DGR</sub>	Drain-gate Voltage (R <sub>GS</sub> = 20 kΩ)	500	V
V <sub>GS</sub>	Gate- source Voltage	±30	V
I <sub>D</sub>	Drain Current (continuous) at T <sub>C</sub> = 25°C	70	A
I <sub>D</sub>	Drain Current (continuous) at T <sub>C</sub> = 100°C	44	A
I <sub>DM</sub> (•)	Drain Current (pulsed)	280	A
P <sub>TOT</sub>	Total Dissipation at T <sub>C</sub> = 25°C	600	W
V <sub>ESD(G-S)</sub>	Gate source ESD(HBM-C=100pF, R=15KΩ)	6	KV
	Derating Factor	5	W/°C
dv/dt (1)	Peak Diode Recovery voltage slope	15	V/ns
T <sub>stg</sub>	Storage Temperature	-65 to 150	°C
T <sub>j</sub>	Max. Operating Junction Temperature	150	°C

(•)Pulse width limited by safe operating area  
September 2002

(1)I<sub>SD</sub> ≤ 60A, di/dt ≤ 400A/μs, V<sub>DD</sub> ≤ V<sub>(BR)DSS</sub>, T<sub>j</sub> ≤ T<sub>JMAX</sub>

## STE70NM50

### THERMAL DATA

Rthj-case	Thermal Resistance Junction-case	Max	0.2	°C/W
Rthj-amb	Thermal Resistance Junction-ambient	Max	30	°C/W
T <sub>I</sub>	Maximum Lead Temperature For Soldering Purpose		300	°C

### AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I <sub>AR</sub>	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T <sub>j</sub> max)	30	A
E <sub>AS</sub>	Single Pulse Avalanche Energy (starting T <sub>j</sub> = 25 °C, I <sub>D</sub> = I <sub>AR</sub> , V <sub>DD</sub> = 35 V)	1.4	J

### ELECTRICAL CHARACTERISTICS (T<sub>CASE</sub> = 25 °C UNLESS OTHERWISE SPECIFIED)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-source Breakdown Voltage	I <sub>D</sub> = 250 µA, V <sub>GS</sub> = 0	500			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current (V <sub>GS</sub> = 0)	V <sub>DS</sub> = Max Rating V <sub>DS</sub> = Max Rating, T <sub>C</sub> = 125 °C			10 100	µA µA
I <sub>GSS</sub>	Gate-body Leakage Current (V <sub>DS</sub> = 0)	V <sub>GS</sub> = ± 20V			± 10	µA

ON (1)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250µA	3	4	5	V
R <sub>DS(on)</sub>	Static Drain-source On Resistance	V <sub>GS</sub> = 10V, I <sub>D</sub> = 30A		0.045	0.05	Ω

### DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g <sub>fs</sub> (1)	Forward Transconductance	V <sub>DS</sub> > I <sub>D(on)</sub> × R <sub>DS(on)</sub> max, I <sub>D</sub> = 30A		35		S
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 25V, f = 1 MHz, V <sub>GS</sub> = 0		7500		pF
C <sub>oss</sub>	Output Capacitance			980		pF
C <sub>rss</sub>	Reverse Transfer Capacitance			200		pF
R <sub>G</sub>	Gate Input Resistance	f=1 MHz Gate DC Bias = 0 Test Signal Level = 20mV Open Drain		1.5		Ω

Note: 1. Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %.

**ELECTRICAL CHARACTERISTICS (CONTINUED)****SWITCHING ON**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	$V_{DD} = 250V$ , $I_D = 30A$		51		ns
$t_r$	Rise Time	$R_G = 4.7\Omega$ , $V_{GS} = 10V$ (see test circuit, Figure 3)		58		ns
$Q_g$	Total Gate Charge	$V_{DD} = 400V$ , $I_D = 60A$ , $V_{GS} = 10V$		190	266	nC
$Q_{gs}$	Gate-Source Charge			53		nC
$Q_{gd}$	Gate-Drain Charge			97		nC

**SWITCHING OFF**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{r(Voff)}$	Off-voltage Rise Time	$V_{DD} = 400V$ , $I_D = 60A$ , $R_G = 4.7\Omega$ , $V_{GS} = 10V$		51		ns
$t_f$	Fall Time	(see test circuit, Figure 5)		46		ns
$t_c$	Cross-over Time			108		ns

**SOURCE DRAIN DIODE**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain Current				60	A
$I_{SDM} (2)$	Source-drain Current (pulsed)				240	A
$V_{SD} (1)$	Forward On Voltage	$I_{SD} = 60A$ , $V_{GS} = 0$			1.5	V
$t_{rr}$	Reverse Recovery Time	$I_{SD} = 60A$ , $di/dt = 100A/\mu s$ , $V_{DD} = 100V$ , $T_J = 25^\circ C$		532		ns
$Q_{rr}$	Reverse Recovery Charge	(see test circuit, Figure 5)		9.9		$\mu C$
$I_{rrm}$	Reverse Recovery Current			37		A
$t_{rr}$	Reverse Recovery Time	$I_{SD} = 60A$ , $di/dt = 100A/\mu s$ , $V_{DD} = 100V$ , $T_J = 150^\circ C$		636		ns
$Q_{rr}$	Reverse Recovery Charge	(see test circuit, Figure 5)		13.4		$\mu C$
$I_{rrm}$	Reverse Recovery Current			42		A

Note: 1. Pulsed: Pulse duration = 300  $\mu s$ , duty cycle 1.5 %.  
2. Pulse width limited by safe operating area.

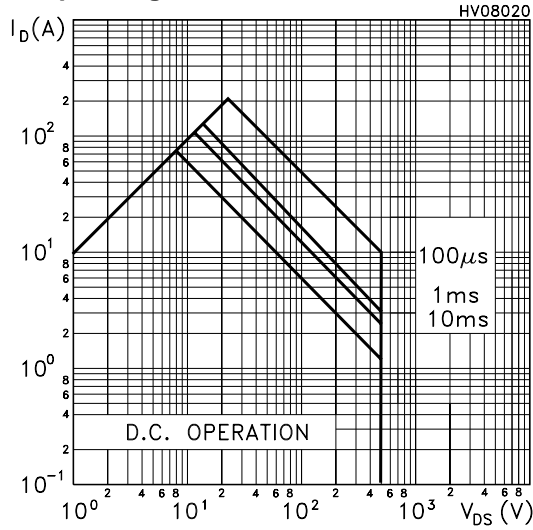
**GATE-SOURCE ZENER DIODE**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$BV_{GSO}$	Gate-Source Breakdown Voltage	$I_{gs} = \pm 1mA$ (Open Drain)	30			V

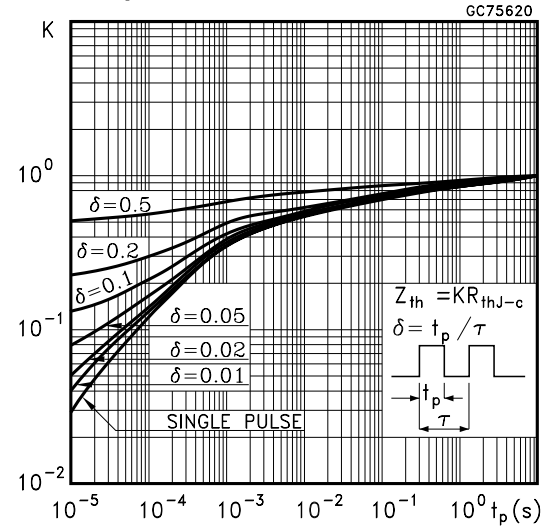
**PROTECTION FEATURES OF GATE-TO-SOURCE ZENER DIODES**

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the 25V Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

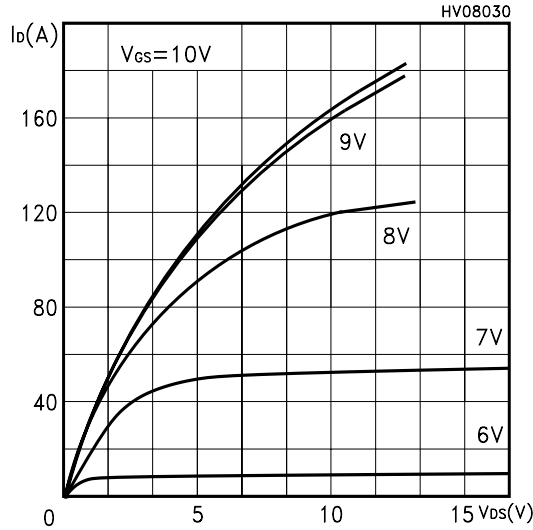
Safe Operating Area



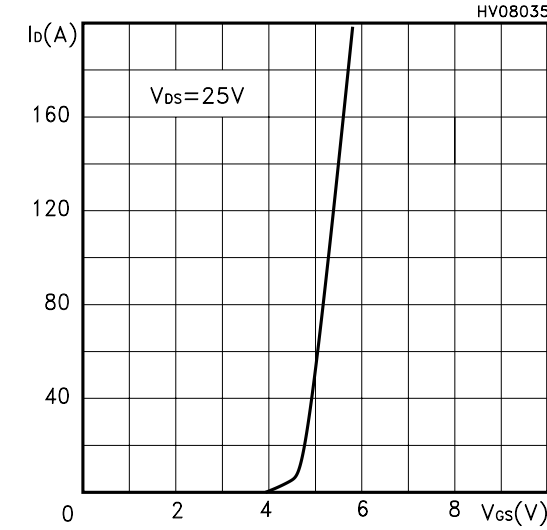
Thermal Impedance



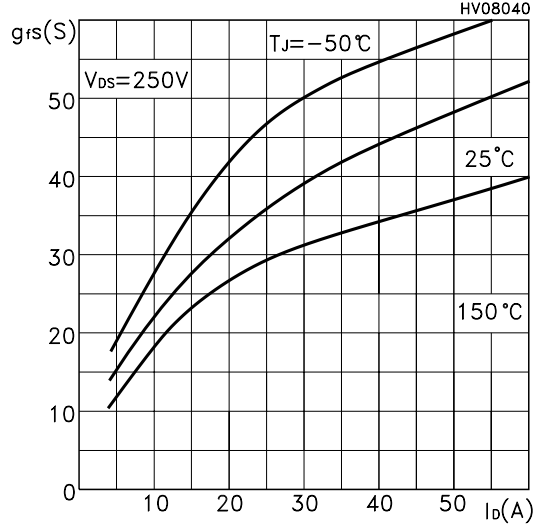
Output Characteristics



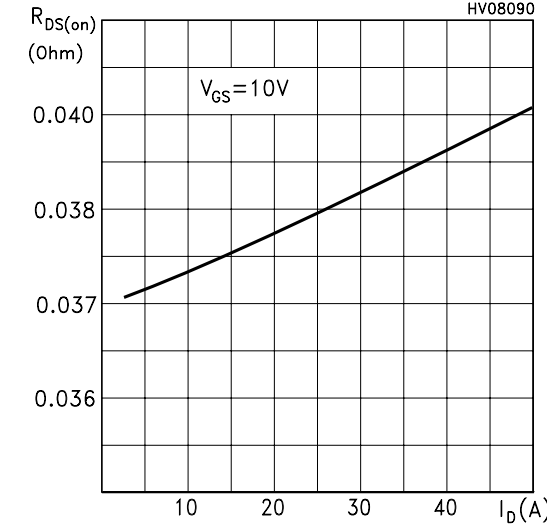
Transfer Characteristics



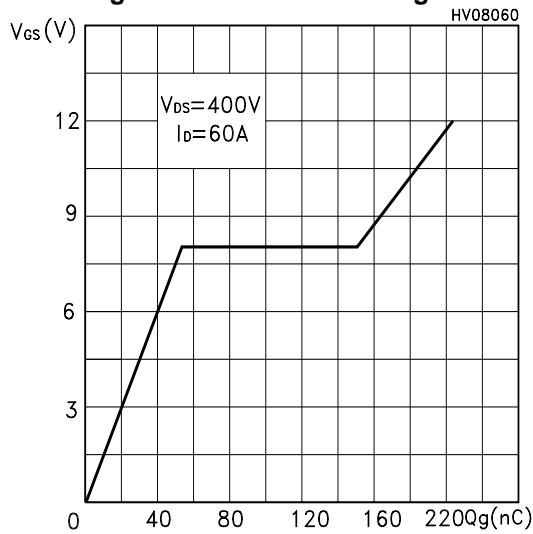
Transconductance



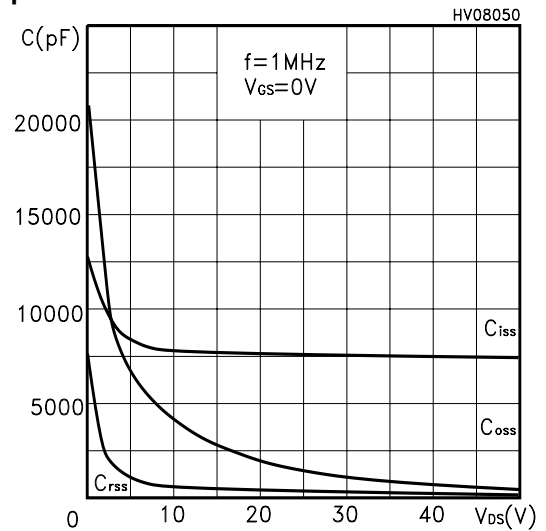
Static Drain-source On Resistance



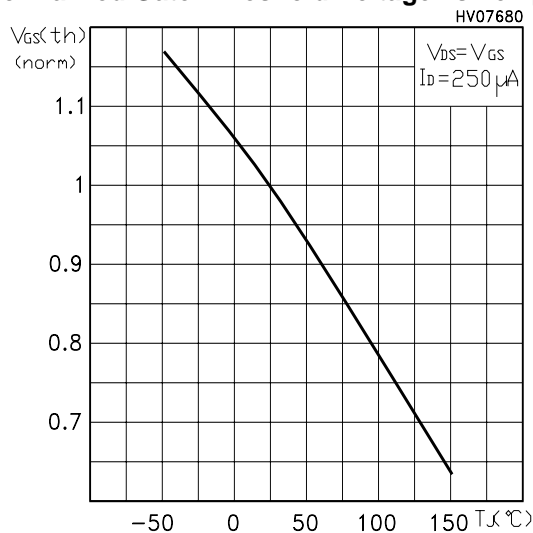
Gate Charge vs Gate-source Voltage



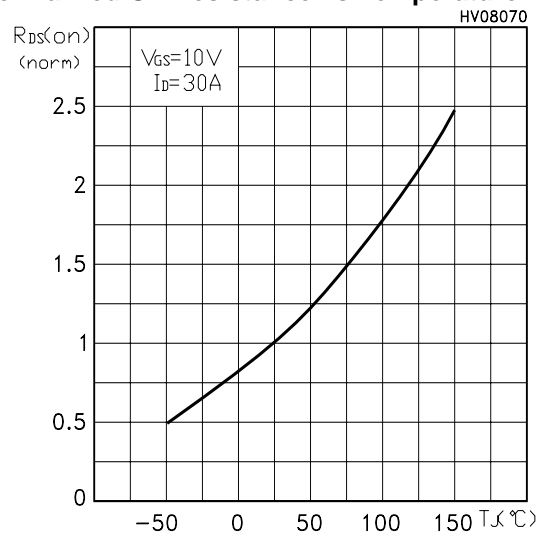
Capacitance Variations



Normalized Gate Threshold Voltage vs Temp.



Normalized On Resistance vs Temperature



Source-drain Diode Forward Characteristics

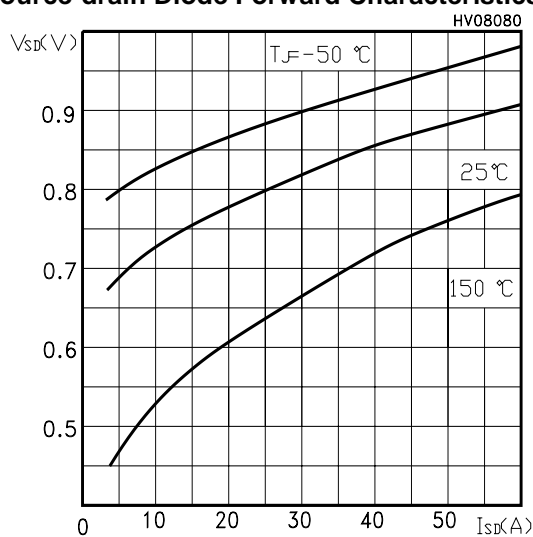


Fig. 1: Unclamped Inductive Load Test Circuit

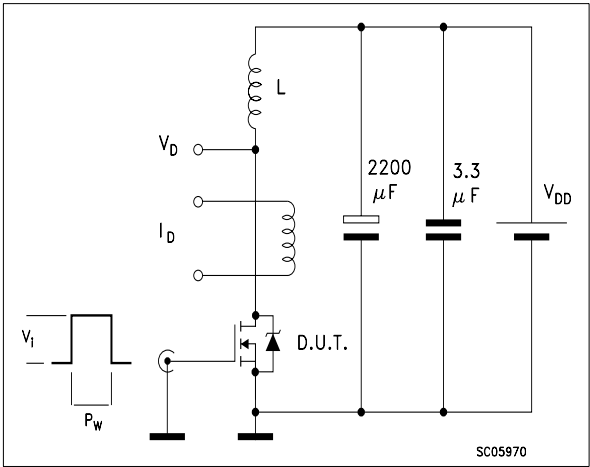


Fig. 2: Unclamped Inductive Waveform

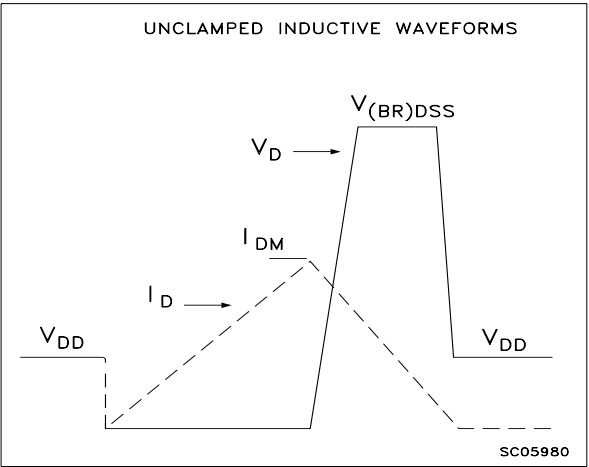


Fig. 3: Switching Times Test Circuit For Resistive Load

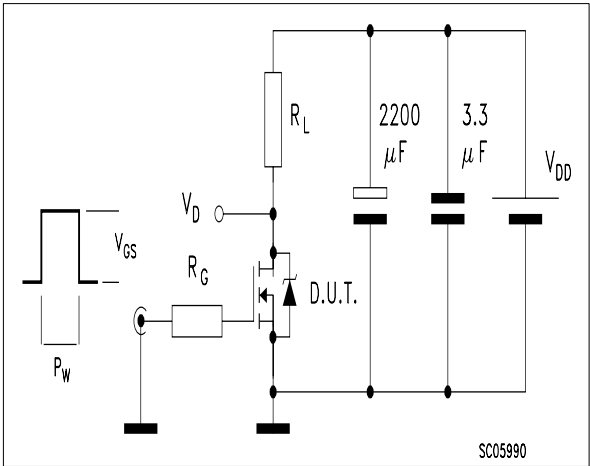


Fig. 4: Gate Charge test Circuit

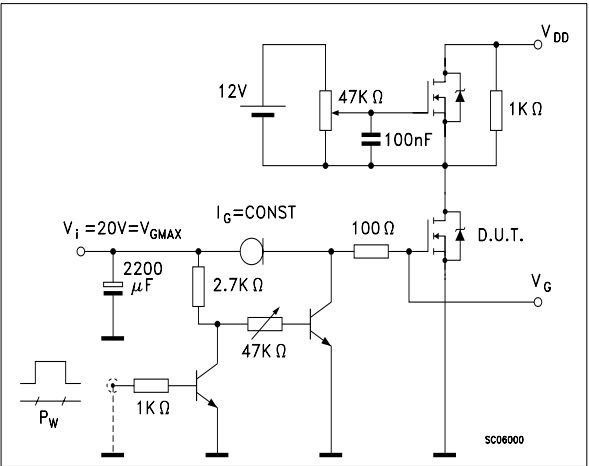
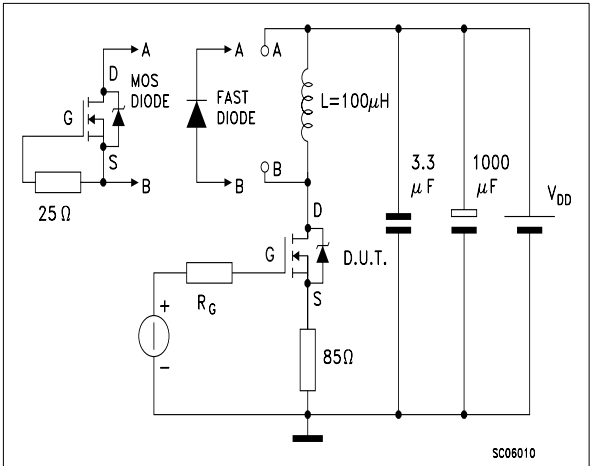
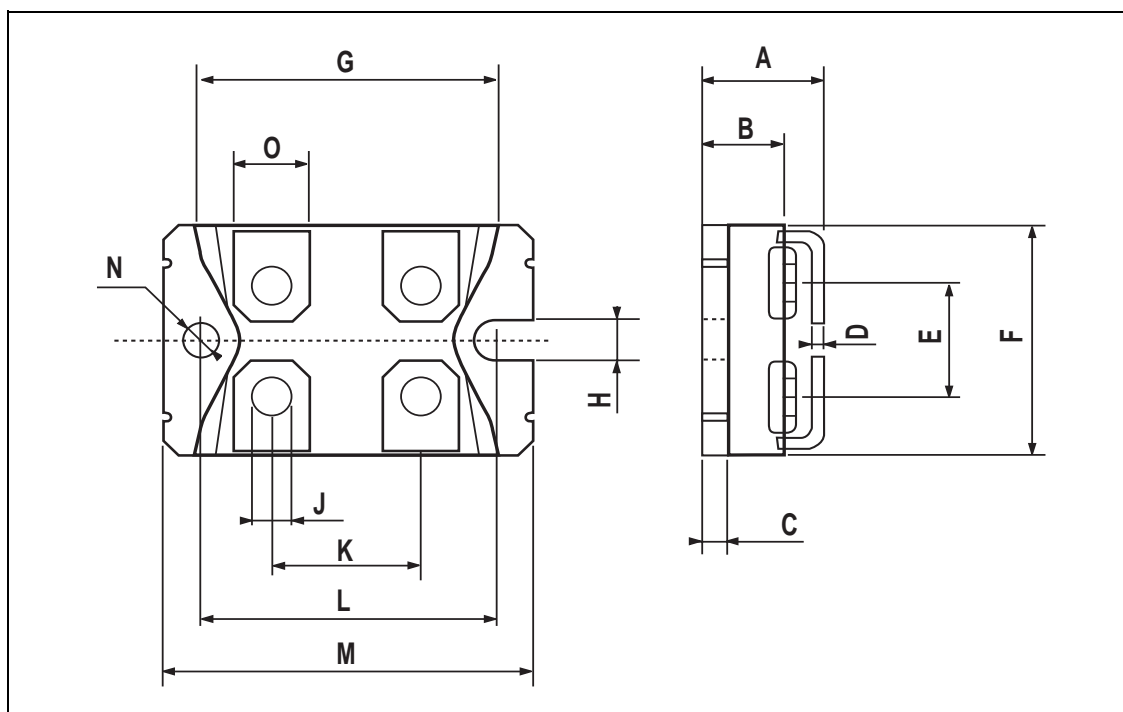


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



## ISOTOP MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	11.8		12.2	0.466		0.480
B	8.9		9.1	0.350		0.358
C	1.95		2.05	0.076		0.080
D	0.75		0.85	0.029		0.033
E	12.6		12.8	0.496		0.503
F	25.15		25.5	0.990		1.003
G	31.5		31.7	1.240		1.248
H	4			0.157		
J	4.1		4.3	0.161		0.169
K	14.9		15.1	0.586		0.594
L	30.1		30.3	1.185		1.193
M	37.8		38.2	1.488		1.503
N	4			0.157		
O	7.8		8.2	0.307		0.322



Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

© The ST logo is a registered trademark of STMicroelectronics

© 2002 STMicroelectronics - Printed in Italy - All Rights Reserved  
STMicroelectronics GROUP OF COMPANIES

Australia - Brazil - Canada - China - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco  
Singapore - Spain - Sweden - Switzerland - United Kingdom - United States.

© <http://www.st.com>