SK10/100EL39W ÷2/4, ÷4/6 Clock Generation Chip

Description

The SK10/100EL39W is a low skew, ÷2/4, ÷4/6 clock generation chip designed explicitly for low skew clock generation applications. The internal dividers are synchronous to each other, therefore, the common output edges are all precisely aligned. The device can be driven by either a differential or single-ended ECL/LVECL or, if positive power supplies are used, PECL/LVPECL input signal. In addition, by using the VBB output, a sinusoidal source can be AC coupled into the device. If a single-ended input is to be used, the VBB output should be connected to the CLK* input and bypassed to VCC via a 0.01 µF capacitor. The VBB output is designed to act as the switching reference of the input of the EL39W under single-ended input conditions. As a result, this pin can only source/sink up to 0.5 mA of current.

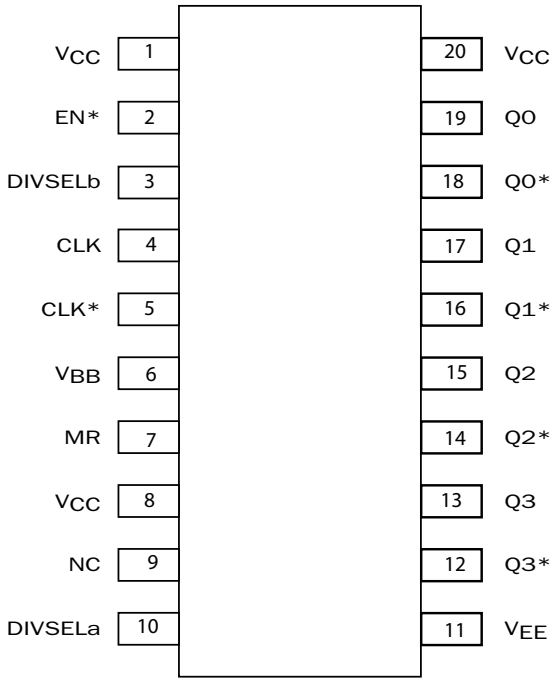
The common enable (EN*) is synchronous so that the internal dividers will only be enabled/disabled when the internal clock is already in the LOW state. This avoids any chance of generating a runt clock pulse on the internal clock when the device is enabled/disabled as can happen with an asynchronous control. An internal runt pulse could lead to losing synchronization between the internal divider stages. The internal enable flip-flop is clocked on the falling edge of the input clock, therefore, all associated specification limits are referenced to the negative edge of the clock input.

Upon start-up, the internal flip-flops will attain a random state; therefore, for systems which utilize multiple EL39Ws, the master reset (MR) input must be asserted to ensure synchronization. For systems which only use one EL39W, the MR pin need not be exercised as the internal divider design ensures synchronization between the ÷2/4 and the ÷4/6 outputs of a single device.

Features

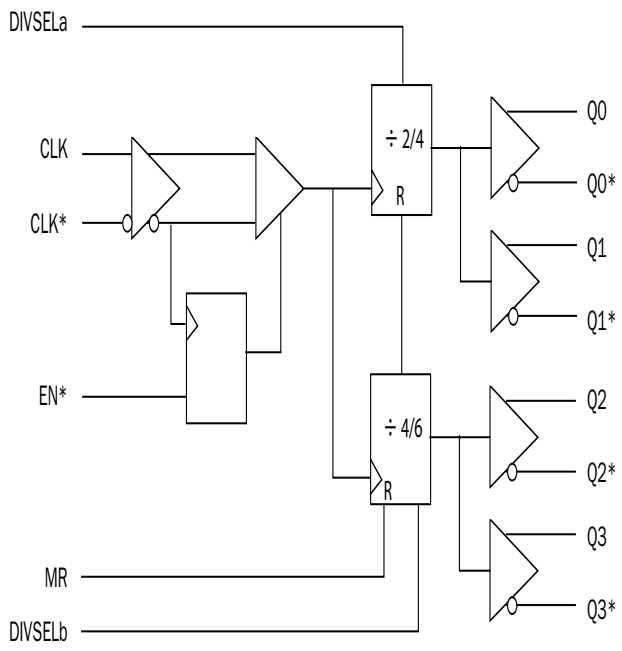
- Extended Supply Voltage Range: (VEE = –3.0V to –5.5V, VCC = 0V) or (VCC = +3.0V to +5.5V, VEE = 0V)
- 50 ps Output-to-Output Skew
- Synchronous Enable/Disable
- Master Reset for Synchronization
- Internal 75KΩ Input Pull-Down Resistors
- Fully Compatible with MC100EL39 and MC100LVEL39
- Specified Over Industrial Temperature Range: –40°C to 85°C
- ESD Protection of >4000V
- Available in 20-Pin SOIC Package

Functional Block Diagram



Pin Descriptions

Logic Diagram



PIn Names

Pin Name	Function
CLK	Differential Clock Inputs
EN*	Synchronous Enable
MR	Master Reset
V_{BB}	Reference Output
Q0, Q0*, Q1, Q1*	Differential ÷2/4 Outputs
Q2, Q2*, Q3, Q3*	Differential ÷4/6 Outputs
DIVSEL	Frequency Select Input

Function Tables

CLK	EN*	MR	Function
Z	L	L	Divide
ZZ	H	L	Hold Q0–3
X	X	H	Reset Q0–3

Z = Low-to-High transistion
ZZ = High-to-Low transition

DIVSELa	Q0, Q1 Outputs
0	Divide by 2
1	Divide by 4
DIVSELb	**Q2, Q3 Outputs**
0	Divide by 4
1	Divide by 6

Truth Table

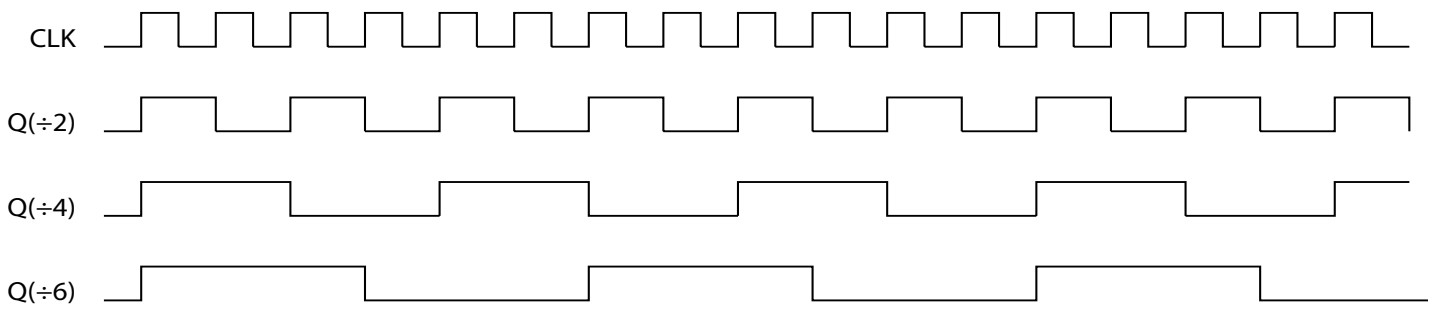
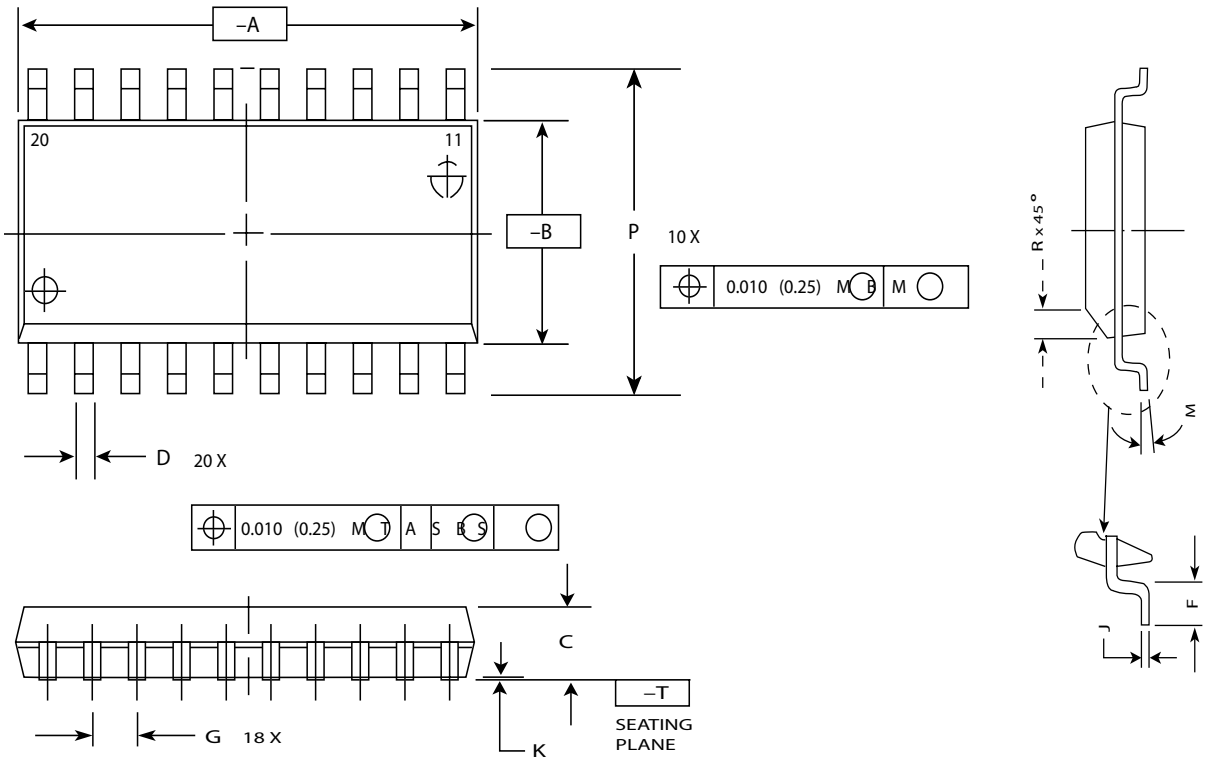


Figure 1. Timing Diagram

Package Information

20 Pin SOIC Package



DIM	Millimeters		Inches	
	MIN	MAX	MIN	MAX
A	12.65	12.95	0.499	0.510
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.23	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

NOTES:
1. Dimensioning and tolerancing per ANSI Y14.5M, 1982.
2. Controlling dimension: millimeter.
3. Dimensions A and B do not include mold protrusion.
4. Maximum mold protrusion 0.150 (0.006) per side.
5. Dimension D does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.13 (0.005) total in excess of d dimension at maximum material condition.

DC Characteristics

SK10/100EL39W DC Electrical Characteristics (Notes 1, 2)

(V_{CC} – V_{EE} = +3.0V to +5.5V ; V_{OUT} loaded 50Ω to V_{CC} – 2.0V)

Symbol	Characteristic	TA = –40°C			TA = 0°C			TA = +25°C			TA = +85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{IN}	Input Current (Diff) (SE)	-150		150 150	-150		150 150	-150		150 150	-150		150 150	µA µA
I_{EE}	Power Supply Current 10EL 100EL		50 51	71 73		50 51	71 73		50 51	71 73		50 51	71 73	mA mA
V_{BB}	Output Reference Voltage[5] 10EL 100EL	-1.43 -1.38		-1.30 -1.26	-1.38 -1.38		-1.27 -1.26	-1.35 -1.38		-1.25 -1.26	-1.31 -1.38		-1.19 -1.26	V V
V_{CC} – V_{EE}	Power Supply Voltage	3.0		5.5	3.0		5.5	3.0		5.5	3.0		5.5	V

AC Characteristics

SK10/100EL39W AC Electrical Characteristics

(V_{CC} – V_{EE} = +3.0V to +5.5V ; V_{OUT} loaded 50Ω to V_{CC} – 2.0V)

Symbol	Characteristic	TA = –40°C			TA = 0°C			TA = +25°C			TA = +85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{MAX}	Maximum Toggle Frequency	1000			1000			1000			1000			MHz
t_{PLH} t_{PHL}	Input to Output Delay CLK → Q (Diff) CLK → Q (SE) MR → Q	725 710 755		900 930 865	745 725 805		930 960 905	765 730 825		955 985 930	825 805 875		1030 1065 1000	ps ps ps
t_{SKEW}	Within-Device Skew (Q0-Q3)[6] Part-to-Part Skew (Q0-Q3 Diff)			50 200			50 200			50 200			50 200	ps ps
t_S	Setup Time EN* → CLK* DIVSEL → CLK	250 400			250 400			250 400			250 400			ps ps
t_H	Hold Time CLK* → EN* CLK → DIVSEL	100 150			100 150			100 150			100 150			ps ps
V_{PP}	Minimum Input Swing CLK[3]	250		1000	250		1000	250		1000	250		1000	mV
V_{CMR}	Common Mode Range [4]	VEE + 1.2		VCC –0.4	VEE + 1.2		VCC –0.4	VEE + 1.2		VCC –0.4	VEE + 1.2		VCC –0.4	V
t_{RR}	Reset Recovery Time			100			100			100			100	ps
t_{PW}	Minimum Pulse Width CLK MR	500 700			500 700			500 700			500 700			ps ps
t_r , t_f	Output Rise/Fall Times Q (20% to 80%)	280		410	285		430	290		445	305		480	ps

AC Characteristics *(continued)*

Notes:

1. 10EL circuits are designed to meet the DC specifications shown in the table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained. Outputs are terminated through a 50Ω resistor to VCC–2.0V.
2. 100K circuits are designed to meet the DC specification shown in the table where transverse airflow greater than 500 lfpm is maintained.
3. Minimum input swing for which AC parameters guaranteed.
4. CMR range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the high level falls within the specified range and the peak-to-peak voltage lies between $VPP_{(min)}$ and 1V. The lower end of the CMR range varies 1:1 with VEE and is equal to VEE + 1.2V.
5. Voltages referenced to VCC = 0V, ECL configuration.
6. The within device skew is defined as the worst case difference between any two similar delay paths within a single device.
7. For standard ECL DC specifications, refer to the ECL Logic Family Standard DC Specifications Data Sheet.
8. For part ordering description, see HPP Part Ordering Information Data Sheet.

Ordering Information

Ordering Code	Package ID	Temperature Range
SK10EL39WD	20-SOIC	Industrial
SK10EL39WDT	20-SOIC	Industrial
SK100EL39WD	20-SOIC	Industrial
SK100EL39WDT	20-SOIC	Industrial
SK10EL39WU	Die	
SK100EL39WU	Die	

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