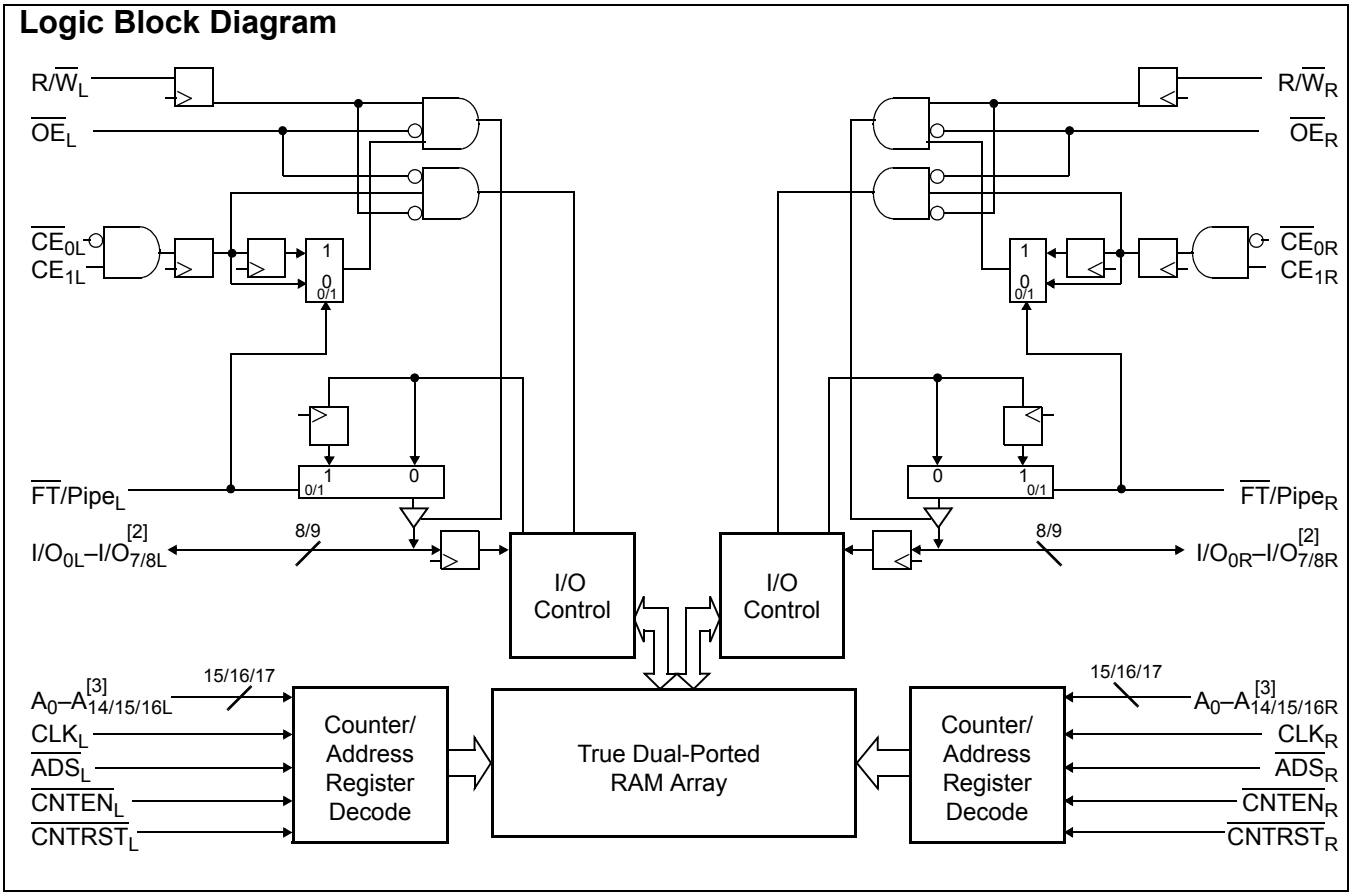
CY7C09079V/89V/99V
CY7C09179V/89V/99V

3.3V 32K/64K/128K x 8/9 Synchronous Dual-Port Static RAM

Features

- True Dual-Ported memory cells which enable simultaneous access of the same memory location
- 6 Flow-Through and Pipelined devices
- 32K x 8/9 organizations (CY7C09079V/179V)
- 64K x 8/9 organizations (CY7C09089V/189V)
- 128K x 8/9 organizations (CY7C09099V/199V)
- 3 Modes
- Flow-Through
- Pipelined
- Burst
- Pipelined output mode on both ports enables fast 100 MHz operation
- 0.35-micron CMOS for optimum speed and power
- High speed clock to data access 6.5[1]/7.5[1]/9/12 ns (max.)
- 3.3V low operating power
- Active= 115 mA (typical)
- Standby= 10 μA (typical)
- Fully synchronous interface for easier operation
- Burst counters increment addresses internally
- Shorten cycle times
- Minimize bus noise
- Supported in Flow-Through and Pipelined modes
- Dual Chip Enables for easy depth expansion
- Automatic power down
- Commercial and Industrial temperature ranges
- Available in 100-pin TQFP
- Pb-free packages available

Logic Block Diagram



Notes
1. See page 6 for Load Conditions.
2. I/O_0–I/O_7 for x8 devices, I/O_0–I/O_8 for x9 devices.
3. A_0–A_{14} for 32K, A_0–A_{15} for 64K, and A_0–A_{16} for 128K devices.

Functional Description

The CY7C09079V/89V/99V and CY7C09179V/89V/99V are high speed synchronous CMOS 32K, 64K, and 128K x 8/9 dual-port static RAMs. Two ports are provided, permitting independent, simultaneous access for reads and writes to any location in memory.[4] Registers on control, address, and data lines enable minimal setup and hold times. In pipelined output mode, data is registered for decreased cycle time. Clock to data valid t_{CD2} = 6.5 ns[1] (pipelined). Flow-through mode can also be used to bypass the pipelined output register to eliminate access latency. In flow-through mode, data is available t_{CD1} = 18 ns after the address is clocked into the device. Pipelined output or flow-through mode is selected via the $\overline{FT}$/Pipe pin.

Each port contains a burst counter on the input address register. The internal write pulse width is independent of the LOW-to-HIGH transition of the clock signal. The internal write pulse is self-timed to enable the shortest possible cycle times.

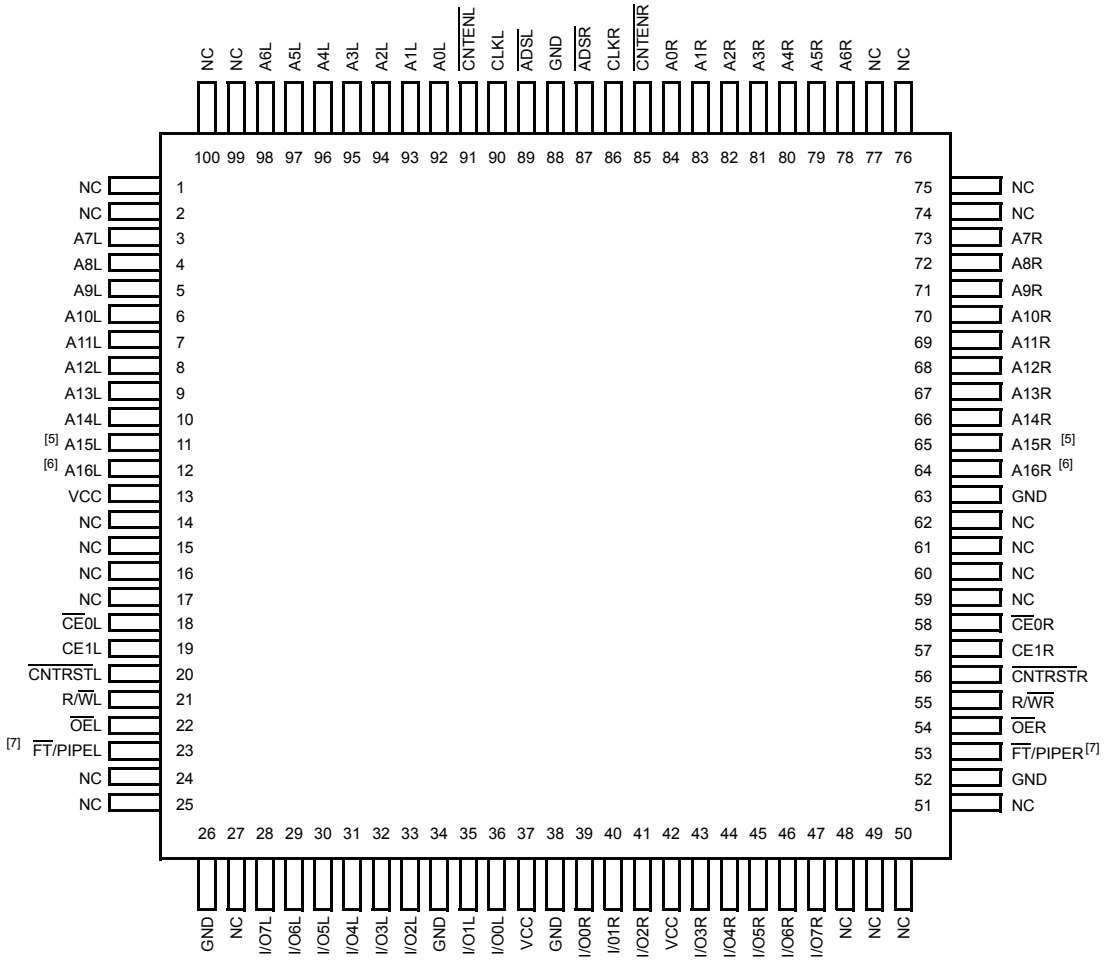
A HIGH on $\overline{CE}_0$ or LOW on CE_1 for one clock cycle powers down the internal circuitry to reduce the static power consumption. The use of multiple Chip Enables enables easier banking of multiple chips for depth expansion configurations. In the pipelined mode, one cycle is required with $\overline{CE}_0$ LOW and CE_1 HIGH to reactivate the outputs.

Counter enable inputs are provided to stall the operation of the address input and use the internal address generated by the internal counter for fast interleaved memory applications. A port's burst counter is loaded with the port's Address Strobe ($\overline{ADS}$). When the port's Count Enable ($\overline{CNTEN}$) is asserted, the address counter increments on each LOW-to-HIGH transition of that port's clock signal. This reads/writes one word from/into each successive address location until $\overline{CNTEN}$ is deasserted. The counter can address the entire memory array and loops back to the start. Counter Reset ($\overline{CNTRST}$) is used to reset the burst counter.

All parts are available in 100-pin Thin Quad Plastic Flatpack (TQFP) packages.

Pin Configurations

Figure 1. 100-Pin TQFP (Top View) - CY7C09099V (128K x 8), CY7C09089V (64K x 8),CY7C09079V (32K x 8)

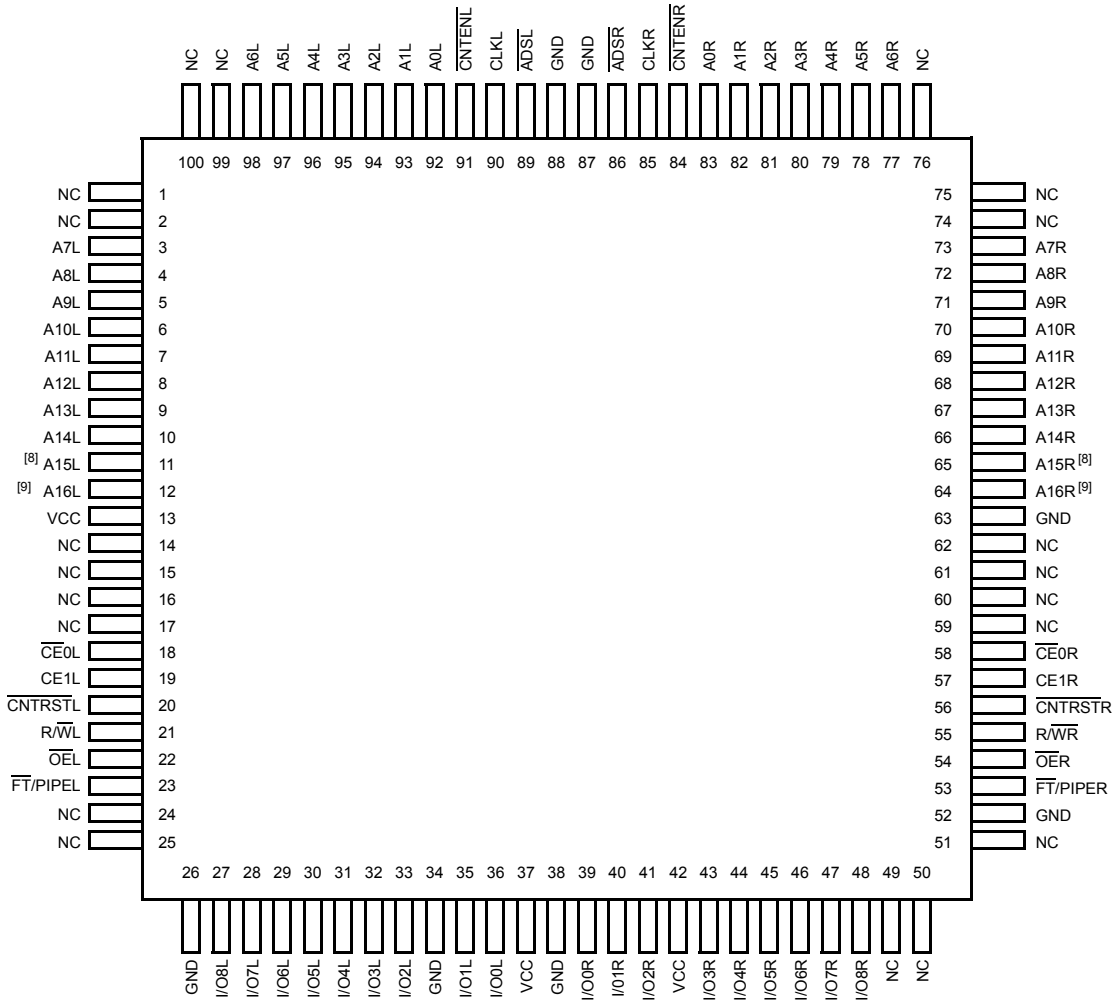


Notes

4. When writing simultaneously to the same location, the final value cannot be guaranteed.
5. This pin is NC for CY7C09079V.
6. This pin is NC for CY7C09079V and CY7C09089V.
7. For CY7C09079V and CY7C09089V, pin #23 connected to V_{CC} is pin compatible with an IDT 5V x8 pipelined device; connecting pin #23 and #53 to GND is pin compatible with an IDT 5V x16 flow-through device.

Pin Configurations (continued)

Figure 2. 100-Pin TQFP (Top View0 - CY7C09199V (128K x 9), CY7C09189V (64K x 9),CY7C09179V (32K x 9)



Selection Guide

Description	CY7C09079V/89V/99V CY7C09179V/89V/99V-6[1]	CY7C09079V/89V/99V CY7C09179V/89V/99V-7[1]	CY7C09079V/89V/99V CY7C09179V/89V/99V -9	CY7C09079V/89V/99V CY7C09179V/89V/99V -12
f_{MAX2} (MHz) (Pipelined)	100	83	67	50
Max. Access Time (ns) (Clock to Data, Pipelined)	6.5	7.5	9	12
Typical Operating Current I_{CC} (mA)	175	155	135	115
Typical Standby Current for I_{SB1} (mA) (Both Ports TTL Level)	25	25	20	20
Typical Standby Current for I_{SB3} (μA) (Both Ports CMOS Level)	10 μA	10 μA	10 μA	10 μA

Pin Definitions

Left Port	Right Port	Description
A_{0L}–A_{16L}	A_{0R}–A_{16R}	Address Inputs (A_0–A_{14} for 32K; A_0–A_{15} for 64K; and A_0–A_{16} for 128K devices).
ADS_L	ADS_R	Address Strobe Input. Used as an address qualifier. This signal should be asserted LOW to access the part using an externally supplied address. Asserting this signal LOW also loads the burst counter with the address present on the address pins.
$\overline{CE}_{0L}$,CE_{1L}	$\overline{CE}_{0R}$,CE_{1R}	Chip Enable Input. To select either the left or right port, both $\overline{CE}_0$ AND CE_1 must be asserted to their active states ($\overline{CE}_0 \le V_{IL}$ and $CE_1 \ge V_{IH}$).
CLK_L	CLK_R	Clock Signal. This input can be free running or strobed. Maximum clock input rate is f_{MAX}.
$CNTEN_L$	$CNTEN_R$	Counter Enable Input. Asserting this signal LOW increments the burst address counter of its respective port on each rising edge of CLK. CNTEN is disabled if ADS or CNTRST are asserted LOW.
$CNTRST_L$	$CNTRST_R$	Counter Reset Input. Asserting this signal LOW resets the burst address counter of its respective port to zero. CNTRST is not disabled by asserting ADS or CNTEN.
I/O_{0L}–I/O_{8L}	I/O_{0R}–I/O_{8R}	Data Bus Input/Output (I/O_0–I/O_7 for x8 devices; I/O_0–I/O_8 for x9 devices).
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable Input. This signal must be asserted LOW to enable the I/O data pins during read operations.
$R/\overline{W}_L$	$R/\overline{W}_R$	Read/Write Enable Input. This signal is asserted LOW to write to the dual port memory array. For read operations, assert this pin HIGH.
$\overline{FT}/PIPE_L$	$\overline{FT}/PIPE_R$	Flow-Through/Pipelined Select Input. For flow-through mode operation, assert this pin LOW. For pipelined mode operation, assert this pin HIGH.
GND		Ground Input.
NC		No Connect.
V_{CC}		Power Input.

Notes
8. This pin is NC for CY7C09179V.
9. This pin is NC for CY7C09179V and CY7C09189V

Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.[10]

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied.. –55°C to +125°C

Supply Voltage to Ground Potential.....–0.5V to +4.6V

DC Voltage Applied to Outputs in High Z State .....–0.5V to V_{CC}+0.5V

DC Input Voltage .....–0.5V to V_{CC}+0.5V

Output Current into Outputs (LOW)..... 20 mA

Static Discharge Voltage..... >2001V

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	3.3V ± 300 mV
Industrial[11]	–40°C to +85°C	3.3V ± 300 mV

Electrical Characteristics Over the Operating Range

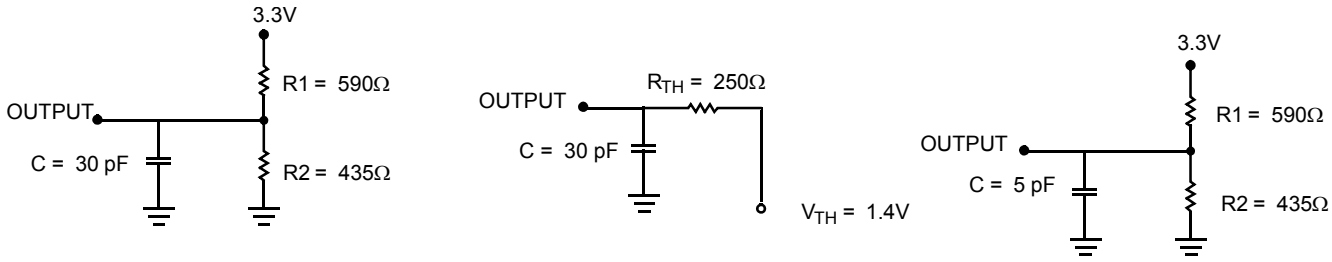
Parameter	Description		CY7C09079V/89V/99V CY7C09179V/89V/99V												Unit
			-6[1]			-7[1]			-9			-12			
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output HIGH Voltage (V_{CC} = Min. I_{OH} = –4.0 mA)		2.4			2.4			2.4			2.4			V
V_{OL}	Output LOW Voltage (V_{CC} = Min. I_{OH} = +4.0 mA)				0.4			0.4			0.4			0.4	V
V_{IH}	Input HIGH Voltage		2.0			2.0			2.0			2.0			V
V_{IL}	Input LOW Voltage				0.8			0.8			0.8			0.8	V
I_{OZ}	Output Leakage Current		–10		10	–10		10	–10		10	–10		10	µA
I_{CC}	Operating Current (V_{CC} = Max. I_{OUT} = 0 mA) Outputs Disabled	Commercial.		175	320		155	275		135	225		115	205	mA
		Industrial[11]					275	390		185	295				mA
I_{SB1}	Standby Current (Both Ports TTL Level)[12] $\overline{CE}_L$ & $\overline{CE}_R \geq V_{IH}$, f = f_{MAX}	Commercial.		25	95		25	85		20	65		20	50	mA
		Industrial[11]					85	120		35	75				mA
I_{SB2}	Standby Current (One Port TTL Level)[12] $\overline{CE}_L$ | $\overline{CE}_R \geq V_{IH}$, f = f_{MAX}	Commercial.		115	175		105	165		95	150		85	140	mA
		Industrial[11]					165	210		105	160				mA
I_{SB3}	Standby Current (Both Ports CMOS Level)[12] $\overline{CE}_L$ & $\overline{CE}_R \geq V_{CC}$ – 0.2V, f = 0	Commercial.		10	250		10	250		10	250		10	250	µA
		Industrial[11]					10	250		10	250				µA
I_{SB4}	Standby Current (One Port CMOS Level)[12] $\overline{CE}_L$ | $\overline{CE}_R \geq V_{IH}$, f = f_{MAX}	Commercial		105	135		95	125		85	115		75	100	mA
		Industrial[11]					125	170		95	125				mA

Capacitance

Parameter	Description	Test Conditions	Max	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 3.3V	10	pF
C_{OUT}	Output Capacitance		10	pF

Notes
10. The Voltage on any input or I/O pin cannot exceed the power pin during power-up.
11. Industrial parts are available in CY7C09099V and CY7C09199V only.
12. $\overline{CE}_L$ and $\overline{CE}_R$ are internal signals. To select either the left or right port, both $\overline{CE}_0$ AND CE_1 must be asserted to their active states ($\overline{CE}_0 \leq V_{IL}$ and $CE_1 \geq V_{IH}$).

Figure 3. AC Test Loads

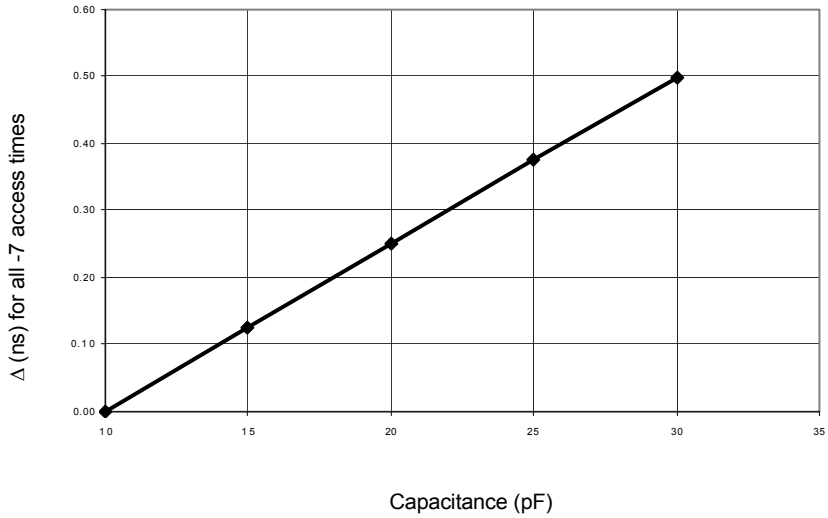


(a) Normal Load (Load 1) **(b) Thévenin Equivalent (Load 1)** **(c) Three-State Delay (Load 2)** (Used for t_{CKLZ}, t_{OLZ}, & t_{OHZ} including scope and jig)

Figure 4. AC Test Loads (Applicable to -6 and -7 only)[13]

(a) Load 1 (-6 and -7 only)

Figure 5. Load Derating Curve



Note
13. Test Conditions: C = 10 pF.

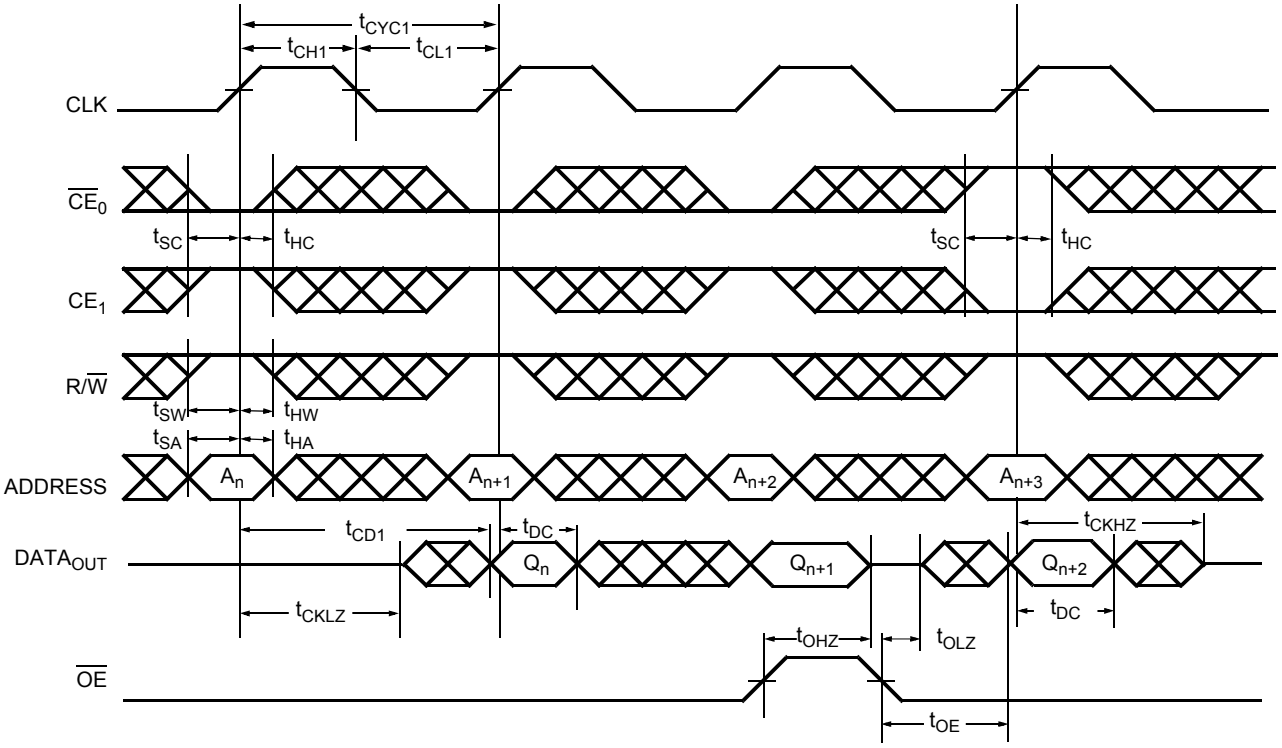
Switching Characteristics Over the Operating Range

Parameter	Description	CY7C09079V/89V/99V CY7C09179V/89V/99V								Unit
		-6[1]		-7[1]		-9		-12		
		Min	Max	Min	Max	Min	Max	Min	Max	
f_{MAX1}	f_{Max} Flow-Through		53		45		40		33	MHz
f_{MAX2}	f_{Max} Pipelined		100		83		67		50	MHz
t_{CYC1}	Clock Cycle Time - Flow-Through	19		22		25		30		ns
t_{CYC2}	Clock Cycle Time - Pipelined	10		12		15		20		ns
t_{CH1}	Clock HIGH Time - Flow-Through	6.5		7.5		12		12		ns
t_{CL1}	Clock LOW Time - Flow-Through	6.5		7.5		12		12		ns
t_{CH2}	Clock HIGH Time - Pipelined	4		5		6		8		ns
t_{CL2}	Clock LOW Time - Pipelined	4		5		6		8		ns
t_R	Clock Rise Time		3		3		3		3	ns
t_F	Clock Fall Time		3		3		3		3	ns
t_{SA}	Address Set-Up Time	3.5		4		4		4		ns
t_{HA}	Address Hold Time	0		0		1		1		ns
t_{SC}	Chip Enable Set-Up Time	3.5		4		4		4		ns
t_{HC}	Chip Enable Hold Time	0		0		1		1		ns
t_{SW}	R/$\overline{W}$ Set-Up Time	3.5		4		4		4		ns
t_{HW}	R/$\overline{W}$ Hold Time	0		0		1		1		ns
t_{SD}	Input Data Set-Up Time	3.5		4		4		4		ns
t_{HD}	Input Data Hold Time	0		0		1		1		ns
t_{SAD}	$\overline{ADS}$ Set-Up Time	3.5		4		4		4		ns
t_{HAD}	$\overline{ADS}$ Hold Time	0		0		1		1		ns
t_{SCN}	$\overline{CNTEN}$ Set-Up Time	3.5		4.5		5		5		ns
t_{HCN}	$\overline{CNTEN}$ Hold Time	0		0		1		1		ns
t_{SRST}	$\overline{CNTRST}$ Set-Up Time	3.5		4		4		4		ns
t_{HRST}	$\overline{CNTRST}$ Hold Time	0		0		1		1		ns
t_{OE}	Output Enable to Data Valid		8		9		10		12	ns
t_{OLZ}[14, 15]	$\overline{OE}$ to Low Z	2		2		2		2		ns
t_{OHZ}[14, 15]	$\overline{OE}$ to High Z	1	7	1	7	1	7	1	7	ns
t_{CD1}	Clock to Data Valid - Flow-Through		15		18		20		25	ns
t_{CD2}	Clock to Data Valid - Pipelined		6.5		7.5		9		12	ns
t_{DC}	Data Output Hold After Clock HIGH	2		2		2		2		ns
t_{CKHZ}[14, 15]	Clock HIGH to Output High Z	2	9	2	9	2	9	2	9	ns
t_{CKLZ}[14, 15]	Clock HIGH to Output Low Z	2		2		2		2		ns
Port to Port Delays										
t_{CWDD}	Write Port Clock HIGH to Read Data Delay		30		35		40		40	ns
t_{CCS}	Clock to Clock Set-Up Time		9		10		15		15	ns

Notes
14. Test conditions used are Load 2.
15. This parameter is guaranteed by design, but it is not production tested.

Switching Waveforms (continued)

Figure 6. Read Cycle for Flow-Through Output ($\overline{FT}$/PIPE = V_{IL})[16, 17, 18, 19]



Notes
16. $\overline{OE}$ is asynchronously controlled; all other inputs are synchronous to the rising clock edge.
17. $\overline{ADS}$ = V_{IL}, $\overline{CNTEN}$ and $\overline{CNTRST}$ = V_{IH}.
18. The output is disabled (high-impedance state) by $\overline{CE}_0$=V_{IH} or CE_1 = V_{IL} following the next rising edge of the clock.
19. Addresses do not have to be accessed sequentially since $\overline{ADS}$ = V_{IL} constantly loads the address on the rising edge of the CLK. Numbers are for reference only.

Switching Waveforms (continued)

Figure 7. Read Cycle for Pipelined Operation ($\overline{FT}$/PIPE = V_{IH})[16, 17, 18, 19]

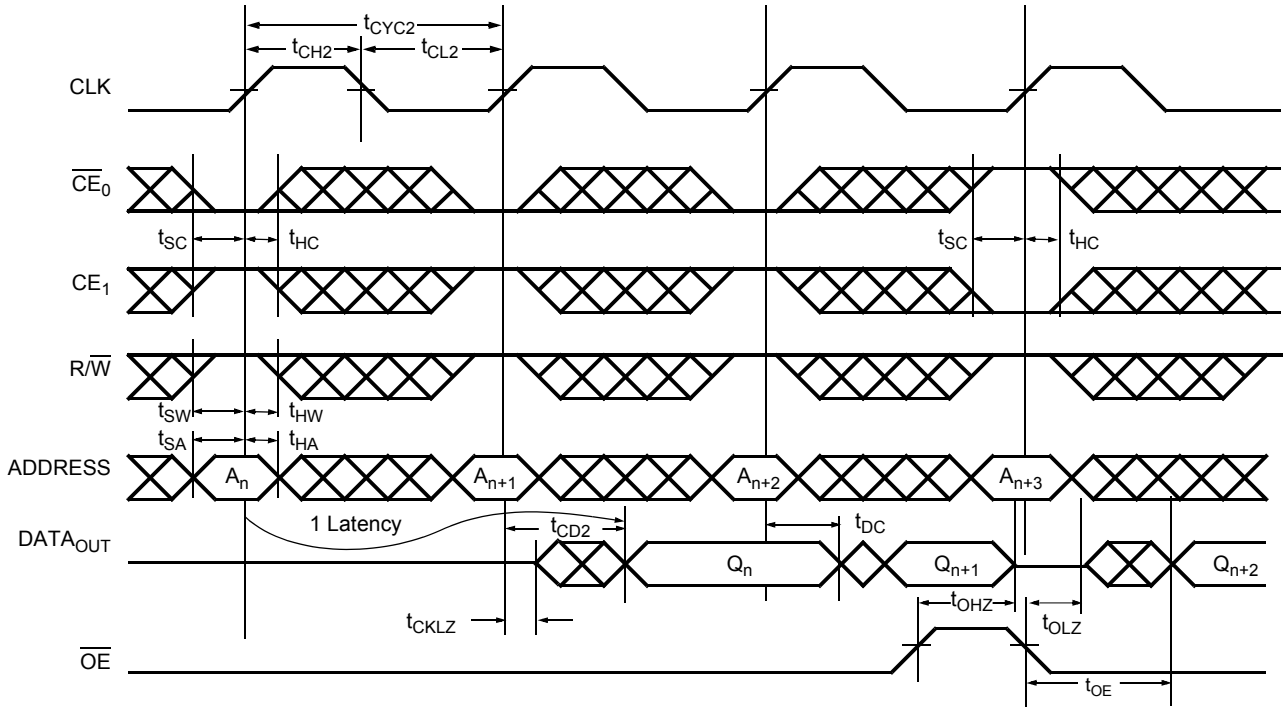
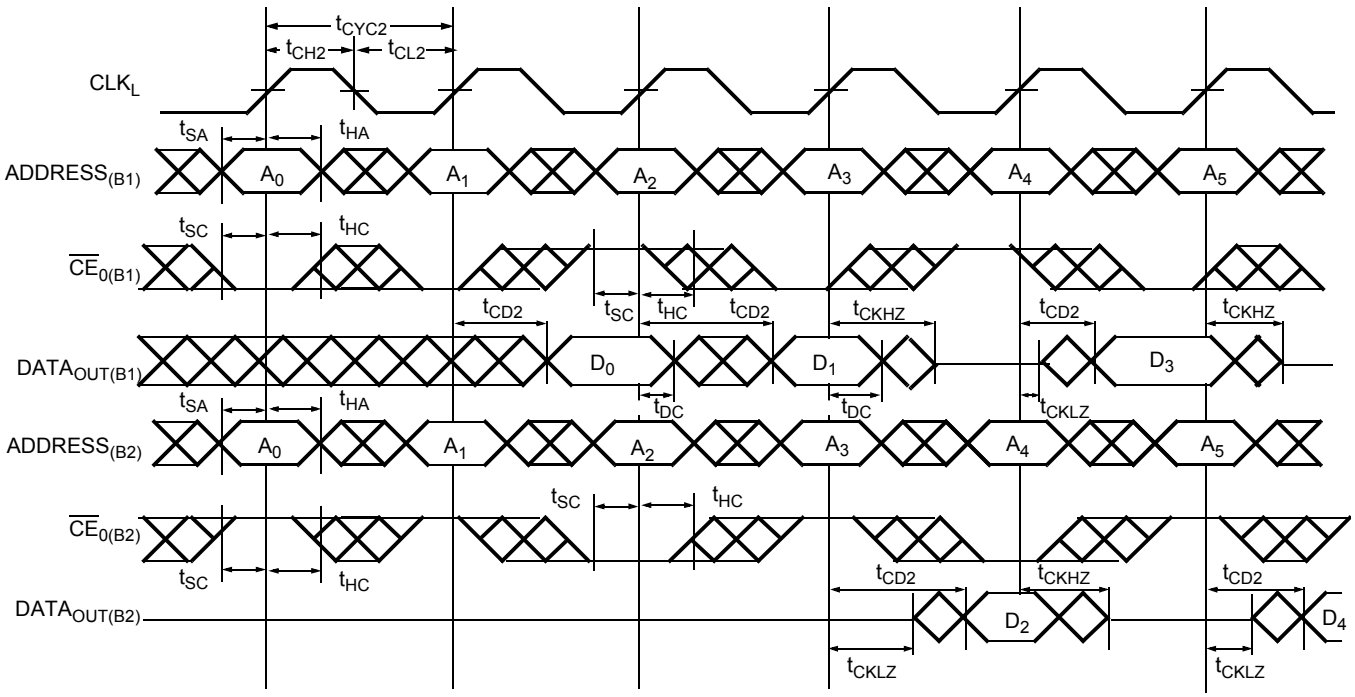
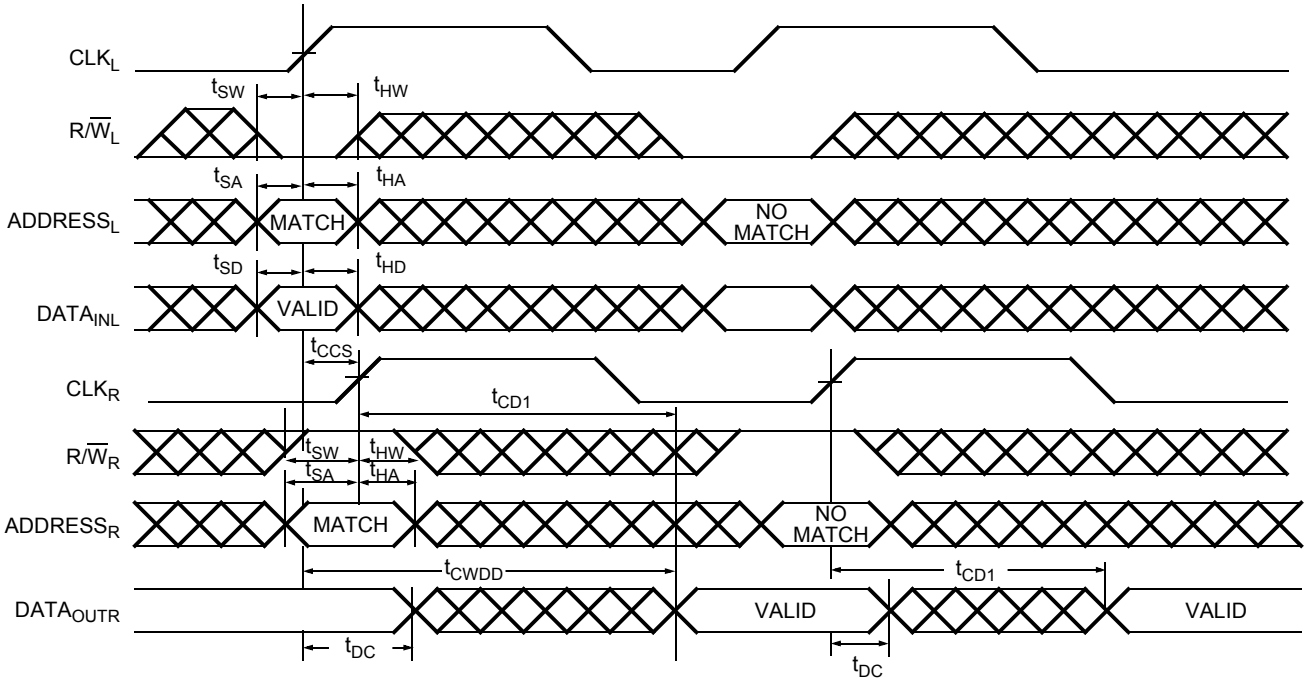


Figure 8. Bank Select Pipelined Read[20, 21]



Switching Waveforms (continued)

Figure 9. Left Port Write to Flow-Through Right Port Read[22, 23, 24, 25]

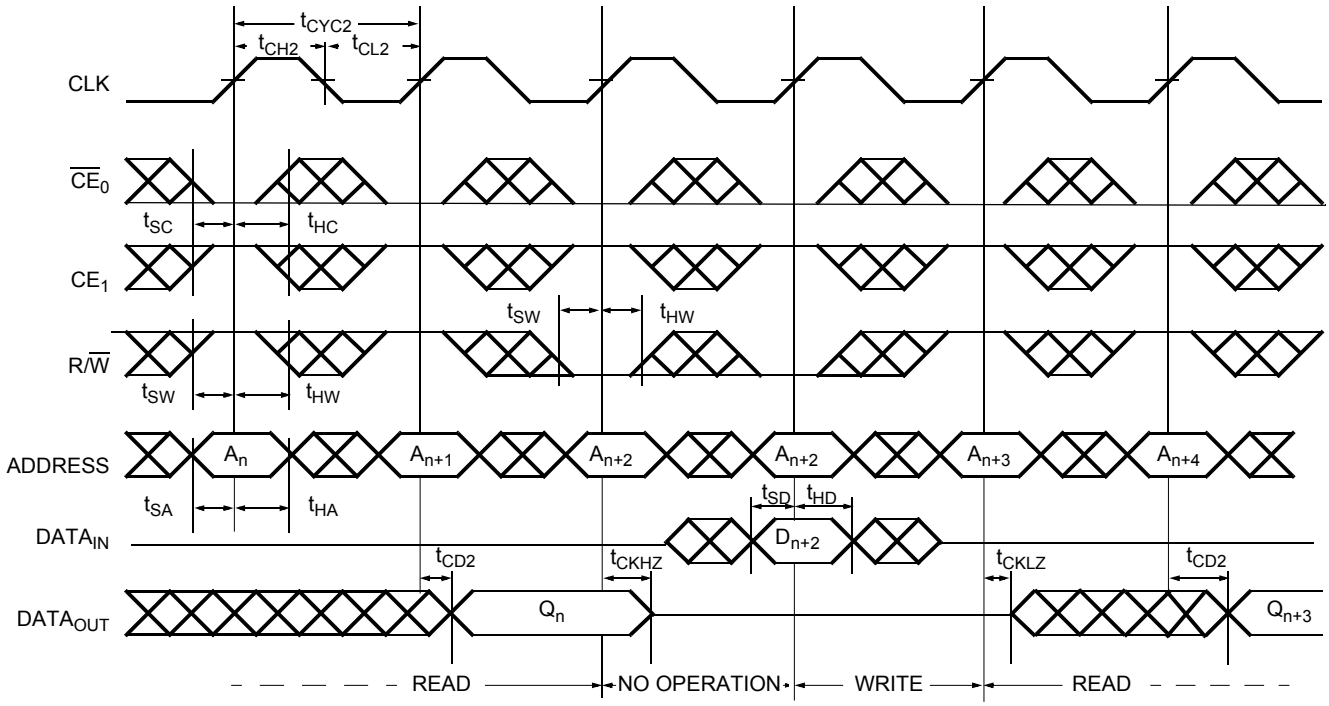


Notes

20. In this depth expansion example, B1 represents Bank #1 and B2 is Bank #2; Each Bank consists of one Cypress dual-port device from this datasheet. $ADDRESS_{(B1)} = ADDRESS_{(B2)}$.
21. $\overline{OE}$ and $\overline{ADS} = V_{IL}$; $CE_{1(B1)}$, $CE_{1(B2)}$, R/$\overline{W}$, $\overline{CNTEN}$, and $\overline{CNTRST} = V_{IH}$.
22. The same waveforms apply for a right port write to flow-through left port read.
23. $\overline{CE_0}$ and $\overline{ADS} = V_{IL}$; CE_1, $\overline{CNTEN}$, and $\overline{CNTRST} = V_{IH}$.
24. $\overline{OE} = V_{IL}$ for the right port, which is being read from. $\overline{OE} = V_{IH}$ for the left port, which is being written to.
25. It $t_{CCS} \leq$ maximum specified, then data from right port READ is not valid until the maximum specified for t_{CWDD}. If t_{CCS}>maximum specified, then data is not valid until $t_{CCS} + t_{CD1}$. t_{CWDD} does not apply in this case.

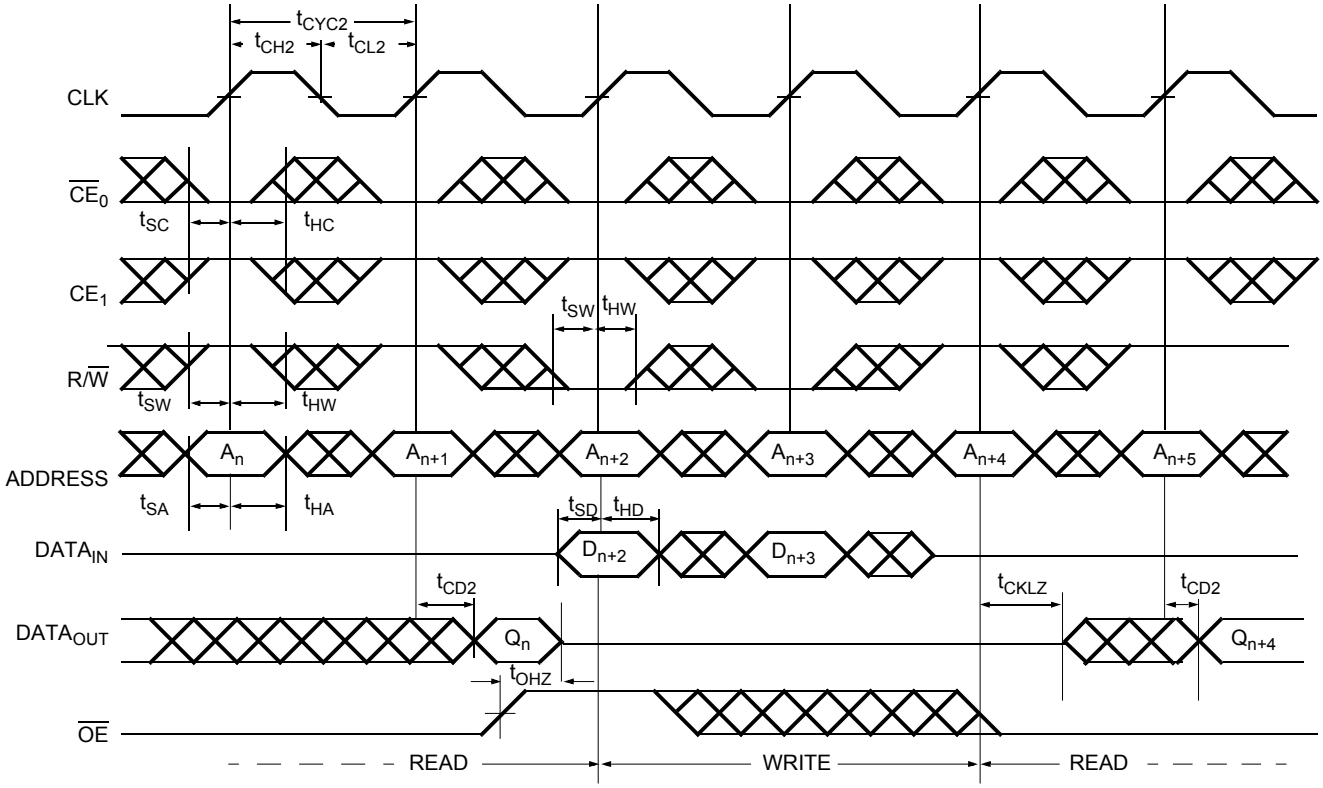
Switching Waveforms (continued)

Figure 10. Pipelined Read-to-Write-to-Read ($\overline{OE}$ = V_{IL})[19, 26, 27, 28]



Switching Waveforms (continued)

Figure 11. Pipelined Read-to-Write-to-Read ($\overline{OE}$ Controlled)[19, 26, 27, 28]



Notes
26. Output state (HIGH, LOW, or high-impedance) is determined by the previous cycle control signals.
27. $\overline{CE_0}$ and $\overline{ADS}$ = V_{IL}; CE_1, $\overline{CNTEN}$, and $\overline{CNTRST}$ = V_{IH}.
28. During “No Operation”, data in memory at the selected address may be corrupted and should be re-written to ensure data integrity.

Switching Waveforms (continued)

Figure 12. Flow-Through Read-to-Write-to-Read ($\overline{OE}$ = V_{IL})[17, 19, 26, 27, 28]

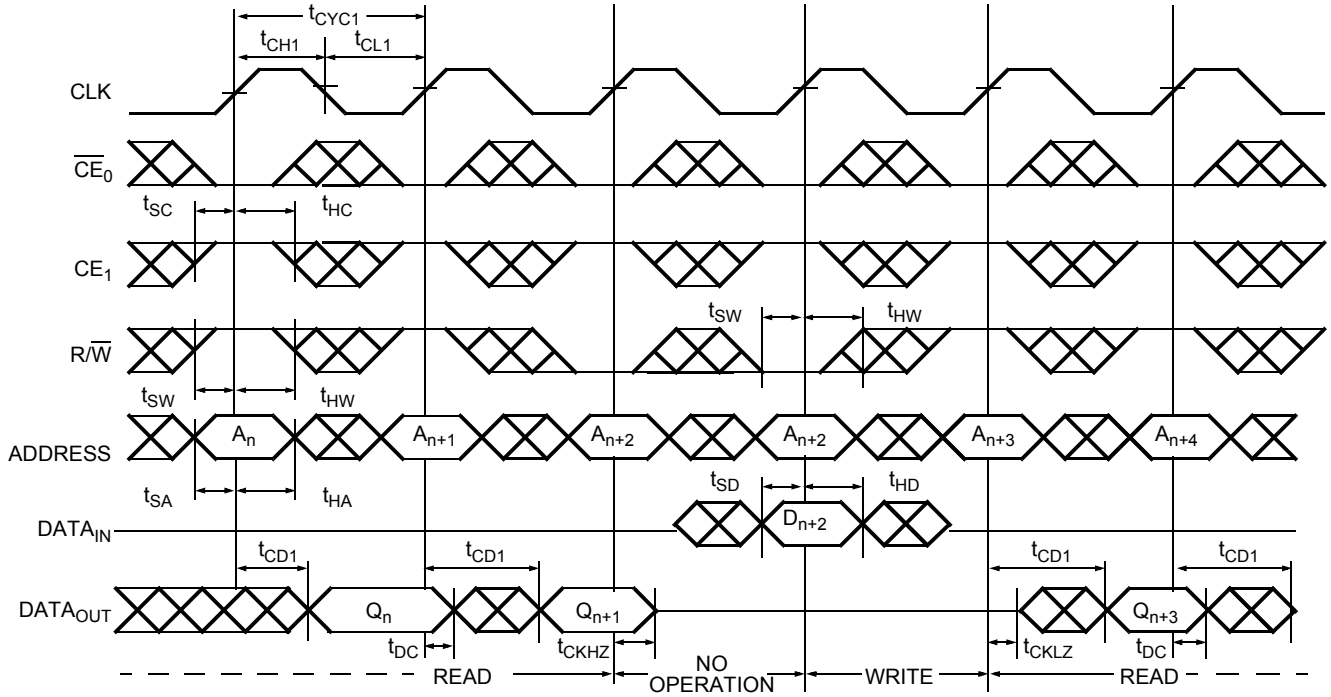
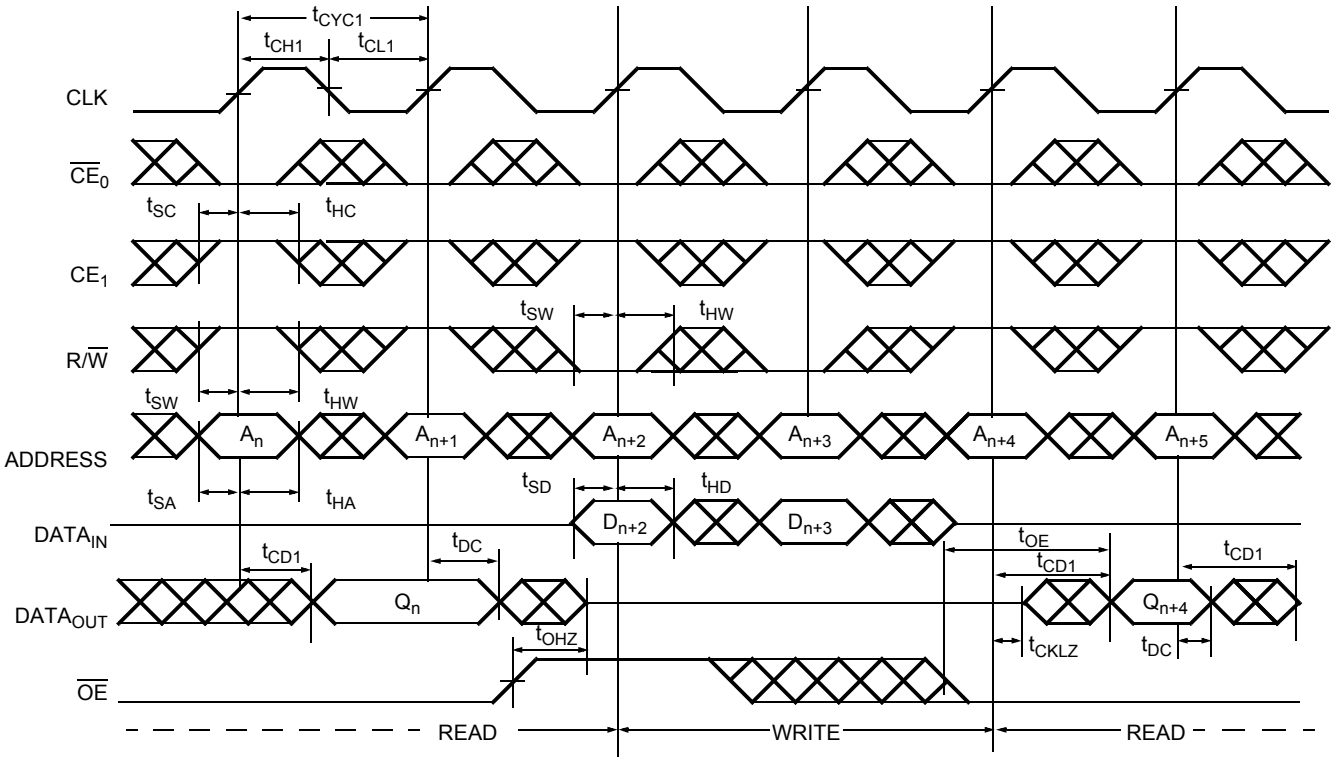


Figure 13. Flow-Through Read-to-Write-to-Read ($\overline{OE}$ Controlled)[17, 20, 26, 27, 28]



Switching Waveforms (continued)

Figure 14. Pipelined Read with Address Counter Advance[29]

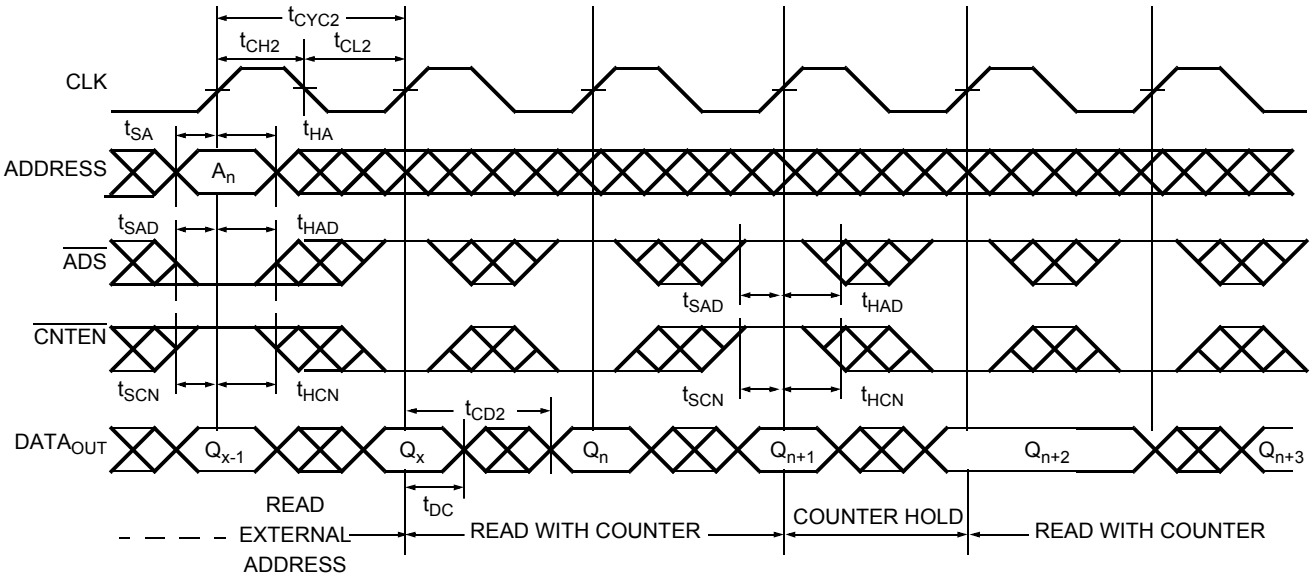
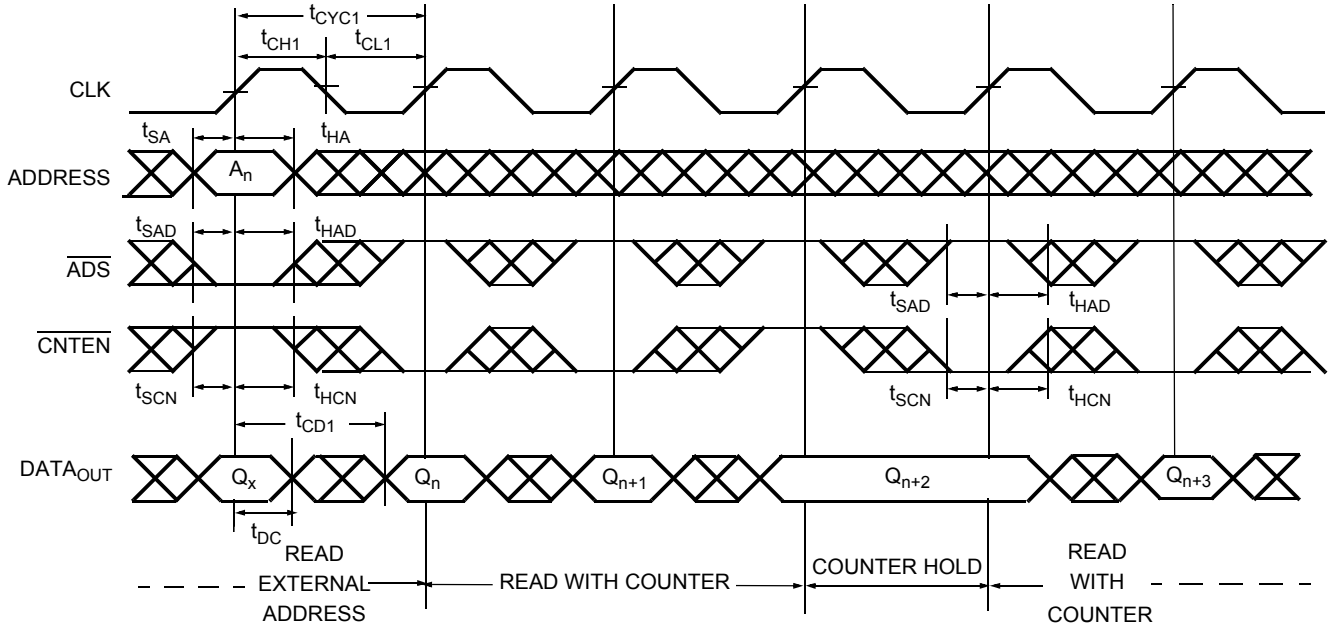


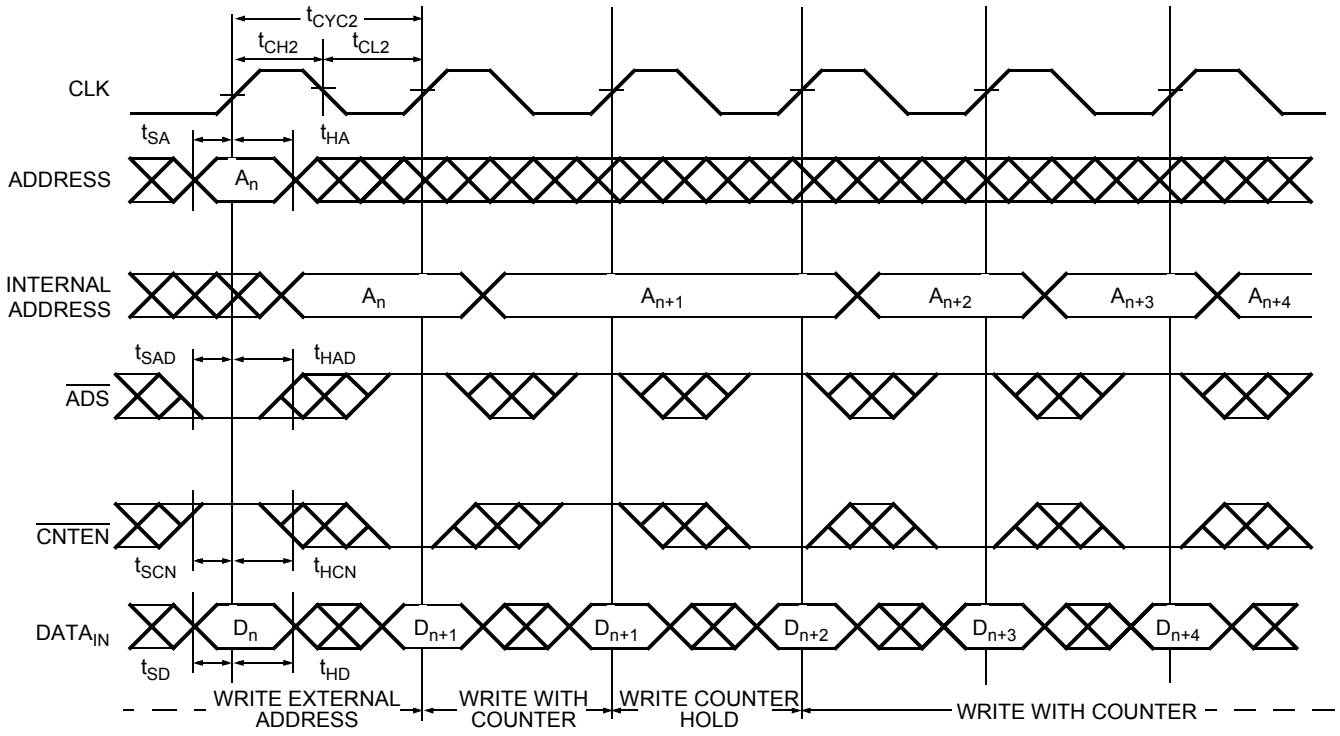
Figure 15. Flow-Through Read with Address Counter Advance[29]



Note
29. $\overline{CE_0}$ and $\overline{OE}$ = V_{IL}; CE_1, R/$\overline{W}$ and $\overline{CNTRST}$ = V_{IH}.

Switching Waveforms (continued)

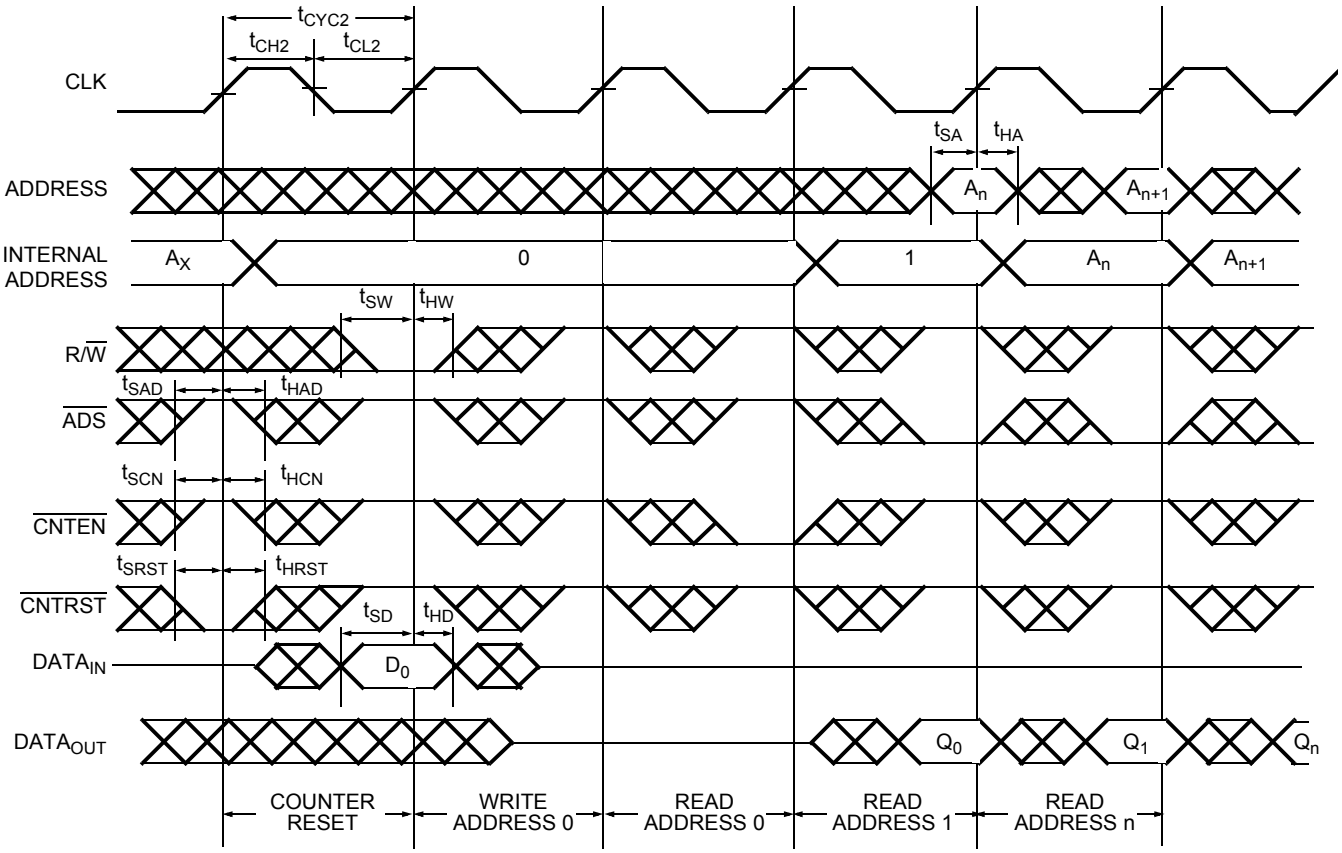
Figure 16. Write with Address Counter Advance (Flow-Through or Pipelined Outputs)[30, 31]



Notes
30. $\overline{CE_0}$ and R/$\overline{W}$ = V_{IL}; CE_1 and $\overline{CNTRST}$ = V_{IH}.
31. The “Internal Address” is equal to the “External Address” when $\overline{ADS}$ = V_{IL} and equals the counter output when $\overline{ADS}$ = V_{IH}.

Switching Waveforms (continued)

Figure 17. Counter Reset (Pipelined Outputs)[19, 26, 32, 33]



Notes
32. $\overline{CE_0} = V_{IL}$; $CE_1 = V_{IH}$.
33. No dead cycle exists during counter reset. A READ or WRITE cycle may be coincidental with the counter reset.

Table 1. Read/Write and Enable Operation[34, 35, 36]

Inputs					Outputs	
$\overline{OE}$	CLK	$\overline{CE_0}$	CE_1	R/$\overline{W}$	I/O_0–I/O_9	Operation
X	⎍	H	X	X	High-Z	Deselected[37]
X	⎍	X	L	X	High-Z	Deselected[37]
X	⎍	L	H	L	D_{IN}	Write
L	⎍	L	H	H	D_{OUT}	Read[37]
H	X	L	H	X	High-Z	Outputs Disabled

Table 2. Address Counter Control Operation[34, 38, 39, 40]

Address	Previous Address	CLK	$\overline{ADS}$	$\overline{CNTEN}$	CNTRST	I/O	Mode	Operation
X	X	⎍	X	X	L	$D_{out(0)}$	Reset	Counter Reset to Address 0
A_n	X	⎍	L	X	H	$D_{out(n)}$	Load	Address Load into Counter
X	A_n	⎍	H	H	H	$D_{out(n)}$	Hold	External Address Blocked—Counter Disabled
X	A_n	⎍	H	L	H	$D_{out(n+1)}$	Increment	Counter Enabled—Internal Address Generation

Notes
34. "X" = "Don't Care", "H" = V_{IH}, "L" = V_{IL}.
35. $\overline{ADS}$, $\overline{CNTEN}$, $\overline{CNTRST}$ = "Don't Care."
36. $\overline{OE}$ is an asynchronous input signal.
37. When $\overline{CE}$ changes state in the pipelined mode, deselection and read happen in the following clock cycle.
38. $\overline{CE_0}$ and $\overline{OE}$ = V_{IL}; CE_1 and R/$\overline{W}$ = V_{IH}.
39. Data shown for flow-through mode; pipelined mode output will be delayed by one cycle.
40. Counter operation is independent of $\overline{CE_0}$ and CE_1.

Ordering Information

32K x8 3.3V Synchronous Dual-Port SRAM

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
6.5[1]	CY7C09079V-6AC	A100	100-Pin Thin Quad Flat Pack	Commercial
7.5[1]	CY7C09079V-7AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C09079V-7AI	A100	100-Pin Thin Quad Flat Pack	Industrial
9	CY7C09079V-9AC	A100	100-Pin Thin Quad Flat Pack	Commercial
12	CY7C09079V-12AC	A100	100-Pin Thin Quad Flat Pack	Commercial

64K x8 3.3V Synchronous Dual-Port SRAM

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
6.5[1]	CY7C09089V-6AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C09089V-6AXC	A100	100-Pin Pb-Free Thin Quad Flat Pack	Commercial
7.5[1]	CY7C09089V-7AC	A100	100-Pin Thin Quad Flat Pack	Commercial
9	CY7C09089V-9AC	A100	100-Pin Thin Quad Flat Pack	Commercial
12	CY7C09089V-12AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C09089V-12AXC	A100	100-Pin Pb-Free Thin Quad Flat Pack	Commercial
	CY7C09089V-12AXI	A100	100-Pin Pb-Free Thin Quad Flat Pack	Industrial

128K x8 3.3V Synchronous Dual-Port SRAM

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
6.5[1]	CY7C09099V-6AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C09099V-6AXC	A100	100-Pin Pb-Free Thin Quad Flat Pack	Commercial
7.5[1]	CY7C09099V-7AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C09099V-7AI	A100	100-Pin Thin Quad Flat Pack	Industrial
	CY7C09099V-7AXI	A100	100-Pin Pb-Free Thin Quad Flat Pack	Industrial
9	CY7C09099V-9AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C09099V-9AI	A100	100-Pin Thin Quad Flat Pack	Industrial
12	CY7C09099V-12AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C09099V-12AXC	A100	100-Pin Pb-Free Thin Quad Flat Pack	Commercial

32K x9 3.3V Synchronous Dual-Port SRAM

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
6.5[1]	CY7C09179V-6AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C09179V-6AXC	A100	100-Pin Pb-Free Thin Quad Flat Pack	Commercial
7.5[1]	CY7C09179V-7AC	A100	100-Pin Thin Quad Flat Pack	Commercial
9	CY7C09179V-9C	A100	100-Pin Thin Quad Flat Pack	Commercial
12	CY7C09179V-12AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C09179V-12AXC	A100	100-Pin Pb-Free Thin Quad Flat Pack	Commercial

64K x9 3.3V Synchronous Dual-Port SRAM

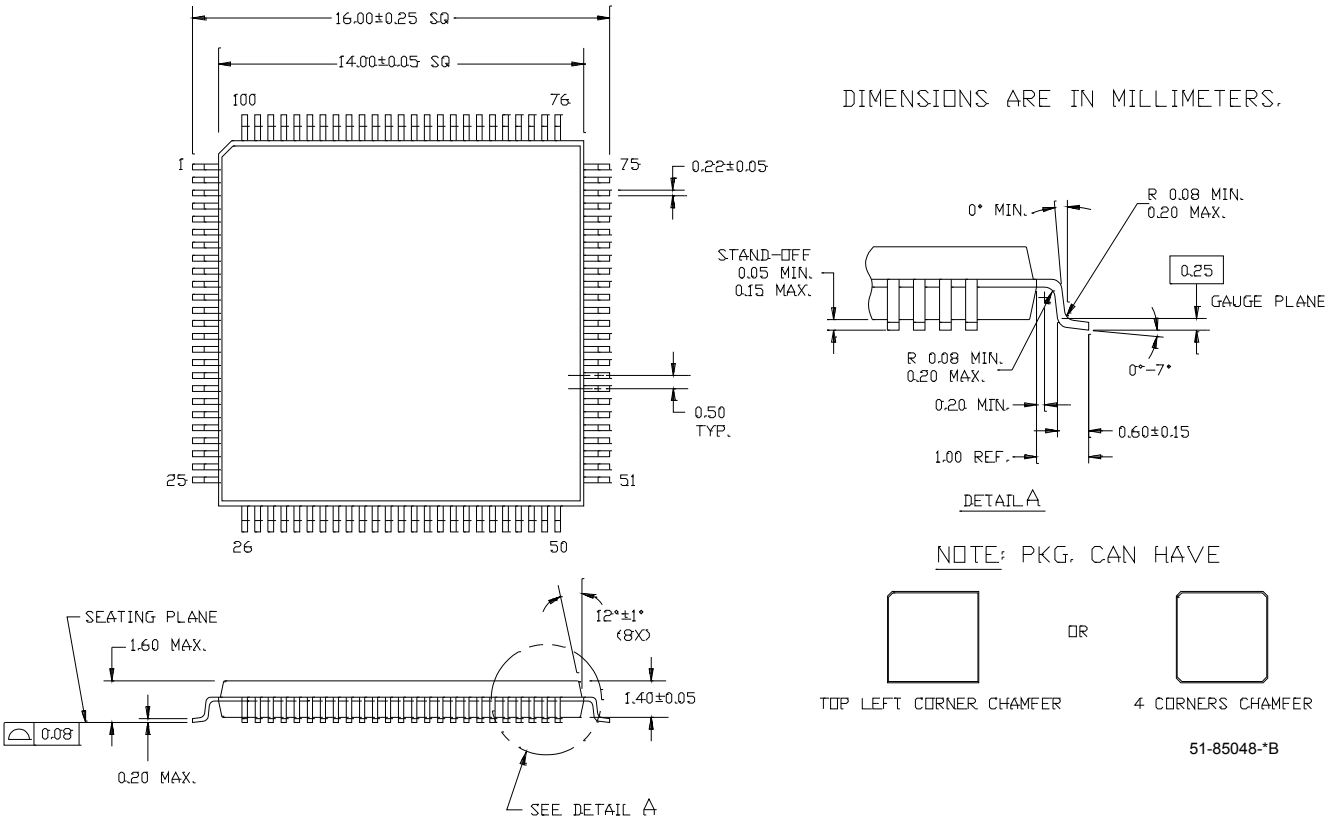
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
6.5[1]	CY7C09189V-6AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C09189V-6AXC	A100	100-Pin Pb-Free Thin Quad Flat Pack	Commercial
7.5[1]	CY7C09189V-7AC	A100	100-Pin Thin Quad Flat Pack	Commercial
9	CY7C09189V-9AC	A100	100-Pin Thin Quad Flat Pack	Commercial
12	CY7C09189V-12AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C09189V-12AXC	A100	100-Pin Pb-Free Thin Quad Flat Pack	Commercial

128K x9 3.3V Synchronous Dual-Port SRAM

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
6.5[1]	CY7C09199V-6AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C09199V-6AXC	A100	100-Pin Pb-Free Thin Quad Flat Pack	Commercial
7.5[1]	CY7C09199V-7AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C09199V-7AXC	A100	100-Pin Pb-Free Thin Quad Flat Pack	Commercial
9	CY7C09199V-9AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C09199V-9AXC	A100	100-Pin Pb-Free Thin Quad Flat Pack	Commercial
	CY7C09199V-9AI	A100	100-Pin Thin Quad Flat Pack	Industrial
	CY7C09199V-9AXI	A100	100-Pin Pb-Free Thin Quad Flat Pack	Industrial
12	CY7C09199V-12AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C09199V-12AXC	A100	100-Pin Pb-Free Thin Quad Flat Pack	Commercial

Package Diagram

Figure 18. 100-Pin Thin Plastic Quad Flat Pack (TQFP) A100 (51-85048)



Document History Page

Document Title: CY7C09079V/89V/99V, CY7C09179V/89V/99V 3.3V 32K/64K/128K x 8/9Synchronous Dual Port Static RAM Document Number: 38-06043				
Rev.	**ECN No.**	**Orig. of Change**	**Orig. of Change**	**Description of Change**
**	110191	SZV	09/29/01	Change from Spec number: 38-00667 to 38-06043
*A	122293	RBI	12/27/02	Power up requirements added to Operating Conditions Information
*B	365034	PCN	See ECN	Added Pb-Free Logo Added Pb-Free Part Ordering Information: CY7C09089V-6AXC, CY7C09089V-12AXC, CY7C09099V-6AXC, CY7C09099V-7AI, CY7C09099V-7AXI, CY7C09099V-12AXC, CY7C09179V-6AXC, CY7C09179V-12AXC, CY7C09189V-6AXC, CY7C09189V-12AXC, CY7C09199V-6AXC, CY7C09199V-7AXC, CY7C09199V-9AXC, CY7C09199V-9AXI, CY7C09199V-12AXC
*C	2623658	VKN/PYRS	12/17/08	Added CY7C09089V-12AXI part in the Ordering information table

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