



1pC Charge Injection, Low Leakage CMOS 4-Channel Multiplexer

Preliminary Technical Data

ADG604

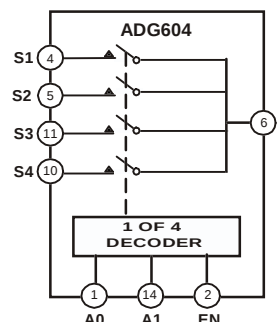
FEATURES

1 pC Charge Injection
 ± 2.7 V to ± 5.5 V Dual Supply
+2.7 V to +5.5 V Single Supply
Extended Temperature Range -40°C to +125°C
100pA Leakage Currents
85 Ω typ On Resistance
Rail-to-Rail Operation
Fast Switching Times
Typical Power Consumption (<0.1 μ W)
TTL/CMOS Compatible Inputs
14-Lead TSSOP Package

APPLICATIONS

Automatic Test Equipment
Data Acquisition Systems
Battery Powered Instruments
Communication Systems
Sample and Hold Systems
Remote Powered Equipment
Audio and Video Signal Routing
Relay Replacement
Avionics

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The ADG604 is a CMOS analog multiplexer, comprising of four single channels. It operates from a dual supply of ± 2.7 V to ± 5.5 V, or from a single supply of +2.7 V to +5.5 V.

The ADG604 switches one of four inputs to a common output, D, as determined by the 3-bit binary address lines, A0, A1 and EN. A Logic "0" on the EN pin disables the device.

The ADG604 offers ultra-low charge injection of 1pC and leakage currents of less than 250pA at 85°C. It offers on-resistance of 85 Ω typ, which is matched to within 8 Ω between channels. The ADG604 also has low power dissipation yet gives high switching speeds.

The ADG604 is available in a 14-lead TSSOP package.

PRODUCT HIGHLIGHTS

1. Ultra-Low Charge Injection (Q_{INJ} : 1.0 pC typ).
2. Leakage Current < 2 nA at 125°C
3. Dual ± 2.7 V to 5 V or Single 2.7 V to 5.5 V supply.
4. Fully Specified at 125°C.
5. Small 14-Lead TSSOP Package.

REV. PrB 08/01

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ADG604—SPECIFICATIONS

DUAL SUPPLY¹ ($V_{DD} = +5\text{ V} \pm 10\%$, $V_{SS} = -5\text{ V} \pm 10\%$, $GND = 0\text{ V}$. All specifications -40°C to $+125^{\circ}\text{C}$ unless noted)

Parameter	+25°C	-40°C to +85°C	-40°C to +125°C	Units	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			V_{SS} to V_{DD}	V	$V_{DD} = +4.5\text{ V}$, $V_{SS} = -4.5\text{ V}$ $V_S = \pm 3.3\text{ V}$, $I_S = -1\text{ mA}$, Test Circuit 1
On Resistance (R_{ON})	85 110	150	165	Ω typ Ω max	
On Resistance Match Between Channels (ΔR_{ON})	6 8		10	Ω typ Ω max	$V_S = \pm 3.3\text{ V}$, $I_S = -1\text{ mA}$
On-Resistance Flatness ($R_{FLAT(ON)}$)	25	60	65	Ω typ Ω max	$V_S = \pm 3.3\text{ V}$, $I_S = -1\text{ mA}$
LEAKAGE CURRENTS					
Source OFF Leakage I_S (OFF)	± 0.01 ± 0.1	± 0.25	2	nA typ nA max	$V_{DD} = +5.5\text{ V}$, $V_{SS} = -5.5\text{ V}$ $V_S = \pm 4.5\text{ V}$, $V_D = \mp 4.5\text{ V}$, nA max Test Circuit 2
Drain OFF Leakage I_D (OFF)	± 0.01 ± 0.1	± 0.25	4	nA typ nA max	$V_S = \pm 4.5\text{ V}$, $V_D = \mp 4.5\text{ V}$, Test Circuit 2
Channel ON Leakage I_D , I_S (ON)	± 0.01 ± 0.1	± 0.25	8	nA typ nA max	$V_S = V_D = \pm 4.5\text{ V}$, Test Circuit 3
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.4	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current I_{INL} or I_{INH}	0.005		± 0.1	μA typ μA max	$V_{IN} = V_{INL}$ or V_{INH}
C_{IN} , Digital Input Capacitance	5			pF typ	
DYNAMIC CHARACTERISTICS²					
Transition Time	120	135	150	ns typ ns max	$V_{S1} = +3\text{ V}$, $V_{S4} = -3\text{ V}$, $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$, Test Circuit 4
t_{ON} Enable	110 TBD	130	145	ns typ ns max	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ $V_S = 3.3\text{ V}$, Test Circuit 6
t_{OFF} Enable	40 TBD	50	55	ns typ ns max	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ $V_S = 3.3\text{ V}$, Test Circuit 6
Break-Before-Make Time Delay, t_{BBM}		85	100	ns typ ns min	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$, $V_{S1} = V_{S2} = 3.3\text{ V}$, Test Circuit 5
Charge Injection	± 1		± 1.5	pC typ pC Max	$V_S = -5.5\text{ V}$ to $+5.5\text{ V}$, $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$, Test Circuit 7
Off Isolation	TBD			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$, Test Circuit 8
Channel-to-Channel Crosstalk	TBD			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$, Test Circuit 10
Bandwidth-3 dB	TBD			MHz typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, Test Circuit 9
C_S (OFF)	2			pF typ	$f = 1\text{ MHz}$
C_D (OFF)	12			pF typ	$f = 1\text{ MHz}$
C_D , C_S (ON)	16			pF typ	$f = 1\text{ MHz}$
POWER REQUIREMENTS					
I_{DD}	0.001		1.0	μA typ μA max	$V_{DD} = +5.5\text{ V}$, $V_{SS} = -5.5\text{ V}$ Digital Inputs = 0 V or 5.5 V
I_{SS}	0.001		1.0	μA typ μA max	Digital Inputs = 0 V or 5.5 V

NOTES

¹Temperature ranges are as follows: Y Grade: -40°C to $+125^{\circ}\text{C}$.²Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

SINGLE SUPPLY¹ ($V_{DD} = +5\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, $GND = 0\text{ V}$. All specifications -40°C to $+125^{\circ}\text{C}$ unless otherwise noted.)

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Units	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 V to V _{DD}	V	V _{DD} = +4.5 V, V _{SS} = 0 V V _S = 3.3 V, I _S = −1 mA, Test Circuit 1
On Resistance (R _{ON})	140 200	255	275	Ω typ Ω max	
On Resistance Match Between Channels (ΔR _{ON})	6 8		10	Ω typ Ω max	
On-Resistance Flatness (R _{FLAT(ON)})	75	90	95	Ω typ Ω max	
LEAKAGE CURRENTS					
Source OFF Leakage I _S (OFF)	±0.01 ±0.1	±0.25	2	nA typ nA max	V _{DD} = +5.5 V V _S = 1 V/4.5 V, V _D = 4.5 V/1 V, Test Circuit 2
Drain OFF Leakage I _D (OFF)	±0.01 ±0.1	±0.25	4	nA typ nA max	V _S = 1 V/4.5 V, V _D = 4.5 V/1 V, Test Circuit 2
Channel ON Leakage I _D , I _S (ON)	±0.01 ±0.1	±0.25	8	nA typ nA max	V _S = V _D = +4.5 V/1 V, Test Circuit 3
DIGITAL INPUTS					
Input High Voltage, V _{INH}			2.4	V min	V _{IN} = V _{INL} or V _{INH}
Input Low Voltage, V _{INL}			0.8	V max	
Input Current I _{INL} or I _{INH}	0.005		±0.1	μA typ μA max	
C _{IN} , Digital Input Capacitance	5			pF typ	
DYNAMIC CHARACTERISTICS ²					
Transition Time	TBD	240	270	ns typ ns max	V _{S1} = +3 V, V _{S4} = 0 V, R _L = 300 Ω, C _L = 35 pF, Test Circuit 4
t _{ON} Enable	180 TBD	210	240	ns typ ns max	R _L = 300 Ω, C _L = 35 pF V _S = 3.3 V, Test Circuit 6
t _{OFF} Enable	65 TBD	70	80	ns typ ns max	R _L = 300 Ω, C _L = 35 pF V _S = 3.3 V, Test Circuit 6
Break-Before-Make Time Delay, t _{BBM}	40	170	195	ns typ ns min	R _L = 300 Ω, C _L = 35 pF, V _{S1} = V _{S2} = 3.3 V, Test Circuit 5
Charge Injection	±1		±1.5	pC typ pC max	V _S = 0 V to +5.5 V, R _S = 0 Ω, C _L = 1 nF, Test Circuit 7
Off Isolation	TBD			dB typ	R _L = 50 Ω, C _L = 5 pF, f = 1 MHz, Test Circuit 8
Channel-to-Channel Crosstalk	TBD			dB typ	R _L = 50 Ω, C _L = 5 pF, f = 1 MHz, Test Circuit 10
Bandwidth −3 dB	TBD			MHz typ	R _L = 50 Ω, C _L = 5 pF, Test Circuit 9
C _S (OFF)	3			pF typ	f = 1MHz
C _D (OFF)	13			pF typ	f = 1MHz
C _D , C _S (ON)	16			pF typ	f = 1MHz
POWER REQUIREMENTS					
I _{DD}	0.001		1.0	μA typ μA max	V _{DD} = +5.5 V Digital Inputs = 0 V or 5.5 V

NOTES¹Temperature ranges are as follows: Y Grade: -40°C to $+125^{\circ}\text{C}$.²Guaranteed by design, not subject to production test.

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ADG604—SPECIFICATIONS

SINGLE SUPPLY¹ ($V_{DD} = +3\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, $GND = 0\text{ V}$. All specifications -40°C to $+125^{\circ}\text{C}$ unless otherwise noted.)

Parameter	+25°C	-40°C to +85°C	-40°C to +125°C	Units	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 V to V_{DD}	V	
On Resistance (R_{ON})	220 300	365	380	Ω typ	$V_{DD} = 3\text{ V}$, $V_{SS} = 0\text{ V}$ $V_S = 1.5\text{ V}$, $I_S = -1\text{ mA}$, Ω max Test Circuit 1
On Resistance Match Between Channels (ΔR_{ON})	TBD		TBD	Ω typ Ω max	$V_S = 1.5\text{ V}$, $I_S = -1\text{ mA}$
LEAKAGE CURRENTS					
Source OFF Leakage I_S (OFF)	± 0.01 ± 0.1	± 0.25	2	nA typ nA max	$V_{DD} = +3.3\text{ V}$ $V_S = 1\text{ V}/3\text{ V}$, $V_D = 3\text{ V}/1\text{ V}$, Test Circuit 2
Drain OFF Leakage I_D (OFF)	± 0.01 ± 0.1	± 0.25	4	nA typ nA max	$V_S = 1\text{ V}/3\text{ V}$, $V_D = 3\text{ V}/1\text{ V}$, Test Circuit 2
Channel ON Leakage I_D , I_S (ON)	± 0.01 ± 0.1	± 0.25	8	nA typ nA max	$V_S = V_D = 1\text{ V}/3\text{ V}$, Test Circuit 3
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current I_{INL} or I_{INH}	0.005		± 0.1	μA typ	$V_{IN} = V_{INL}$ or V_{INH} μA max
C_{IN} , Digital Input Capacitance	5			pF typ	
DYNAMIC CHARACTERISTICS²					
Transition Time	420	480	530	ns typ ns max	$V_{S1} = +1.5\text{ V}$, $V_{S4} = 0\text{ V}$, $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$, Test Circuit 4
t_{ON} Enable	390 TBD	415	460	ns typ ns max	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ $V_S = 1.5\text{ V}$, Test Circuit 6
t_{OFF} Enable	76 TBD	TBD	165	ns typ ns max	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ $V_S = 1.5\text{ V}$, Test Circuit 6
Break-Before-Make Time Delay, t_{BBM}	120	155	380	ns typ ns min	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$, $V_{S1} = V_{S2} = 1.5\text{ V}$, Test Circuit 5
Charge Injection	± 1		± 1.5	pC typ pC max	$V_S = 0\text{ V}$ to $+3.3\text{ V}$, $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$, Test Circuit 7
Off Isolation	TBD			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$, Test Circuit 8
Channel-to-Channel Crosstalk	TBD			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$, Test Circuit 10
Bandwidth-3 dB	TBD			MHz typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, Test Circuit 9
C_S (OFF)	3			pF typ	$f = 1\text{ MHz}$
C_D (OFF)	13			pF typ	$f = 1\text{ MHz}$
C_D , C_S (ON)	16			pF typ	$f = 1\text{ MHz}$
POWER REQUIREMENTS					
I_{DD}	0.001		1.0	μA typ μA max	$V_{DD} = +3.3\text{ V}$ Digital Inputs = 0 V or 3.3 V

NOTES

¹Temperature ranges are as follows: Y Grade: -40°C to $+125^{\circ}\text{C}$.²Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS¹(T_A = +25°C unless otherwise noted)

V _{DD} to V _{SS}	13 V
V _{DD} to GND	−0.3 V to +6.5 V
V _{SS} to GND	+0.3 V to −6.5 V
Analog Inputs ²	V _{SS} −0.3 V to V _{DD} + 0.3 V
Digital Inputs ²	−0.3 V to V _{DD} + 0.3 V or 30 mA, Whichever Occurs First
Peak Current, S or D	20 mA (Pulsed at 1 ms, 10% Duty Cycle max)
Continuous Current, S or D	10 mA
Operating Temperature Range Extended (Y Grade)	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	+150°C

TSSOP Package, Power Dissipation	430 mW
θ _{JA} Thermal Impedance	150°C/W
θ _{JC} Thermal Impedance	27°C/W
Lead Temperature, Soldering (10 seconds)	300°C
IR Reflow, Peak Temperature	+220°C

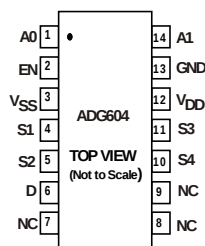
NOTES

¹Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

²Overvoltages at EN, A0, A1, S or D will be clamped by internal diodes. Current should be limited to the maximum ratings given.

ORDERING GUIDE

Model Option	Temperature Range	Package Description	Package
ADG604YRU	−40°C to +125°C	Thin Shrink Small Outline (TSSOP)	RU-14

PIN CONFIGURATION
14-Lead TSSOP
(RU-14)
**Table I. Truth Table for the ADG604**

A1	A0	EN	ON Switch
X	X	0	NONE
0	0	1	1
0	1	1	2
1	0	1	3
1	1	1	4

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADG604 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



TERMINOLOGY

V_{DD}	Most Positive Power Supply Potential.
V_{SS}	Most Negative Power Supply in a Dual Supply Application. In single supply applications, this should be tied to ground at the device.
GND	Ground (0 V) Reference.
I_{DD}	Positive Supply Current.
I_{SS}	Negative Supply Current.
S	Source Terminal. May be an input or output.
D	Drain Terminal. May be an input or output.
R_{ON}	Ohmic resistance between D and S.
ΔR_{ON}	On resistance match between any two Channels i.e., $R_{ON} \text{ max} - R_{ON} \text{ min}$.
$R_{FLAT(ON)}$	Flatness is defined as the difference between the maximum and minimum value of on resistance as measured over the specified analog signal range.
I_S (OFF)	Source Leakage Current with the switch "OFF."
I_D (OFF)	Drain Leakage Current with the switch "OFF."
I_D, I_S (ON)	Channel Leakage Current with the switch "ON."
V_D, V_S	Analog Voltage on Terminals D, S.
V_{INL}	Maximum Input Voltage for Logic "0".
V_{INH}	Minimum Input Voltage for Logic "1".
$I_{INL}(I_{INH})$	Input Current of the digital Input.
C_S (OFF)	Channel input capacitance for "OFF" condition.
C_D (OFF)	Channel output capacitance for "OFF" condition.
C_D, C_S (ON)	"ON" Switch Capacitance.
C_{IN}	Digital Input Capacitance.
$t_{ON(EN)}$	Delay time between the 50% and 90% points of the digital input and switch "ON" condition.
$t_{OFF(EN)}$	Delay time between the 50% and 90% points of the digital input and switch "OFF" condition.
$t_{TRANSITION}$	Delay time between the 50% and 90% points of the digital input and switch "ON" condition when switching from one address state to another.
t_{BBM}	"OFF" time or "ON" time measured between the 80% points of both switches, when switching from one address state to another.
Charge Injection	A measure of the Glitch Impulse transferred from the Digital input to the Analog output during switching.
Crosstalk	A measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.
Off Isolation	A measure of unwanted signal coupling through an "OFF" switch.
Bandwidth	The frequency response of the "ON" switch.
Insertion Loss	The Loss due to the ON resistance of the Switch.

Typical Performance Characteristics

ADG604

TBD

TPC 1.

TBD

TPC 2.

TBD

TPC 3.

TBD

TPC 4.

TBD

TPC 5.

TBD

TPC 6.

TBD

TPC 7.

TBD

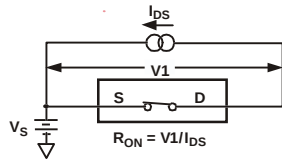
TPC 8.

TBD

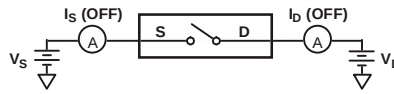
TPC 9.

ADG604

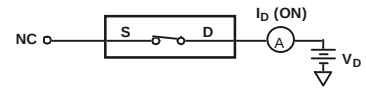
Test Circuits



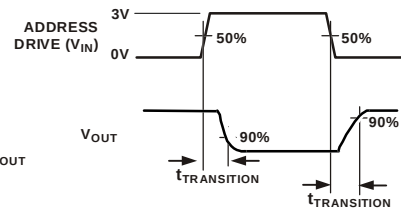
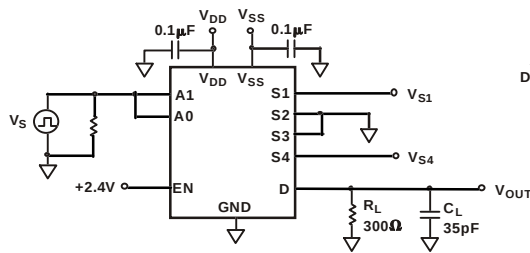
Test Circuit 1. On Resistance



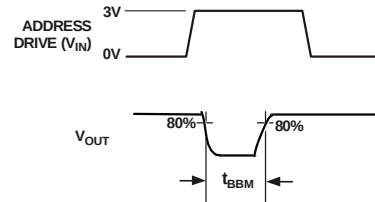
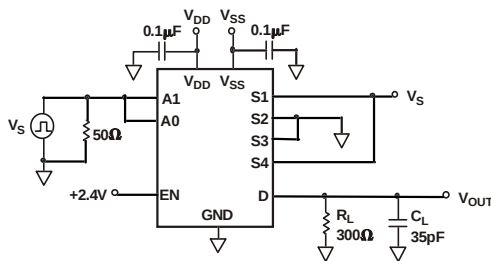
Test Circuit 2. Off Leakage



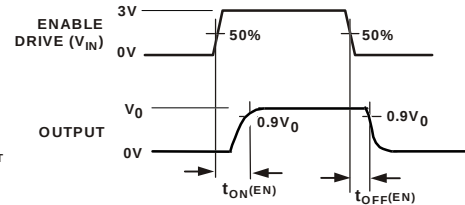
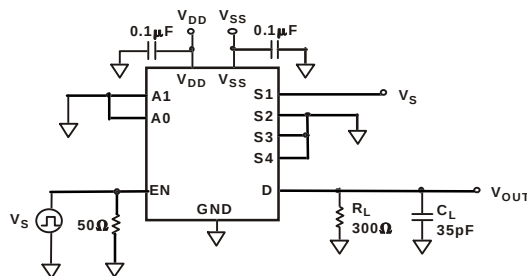
Test Circuit 3. On Leakage



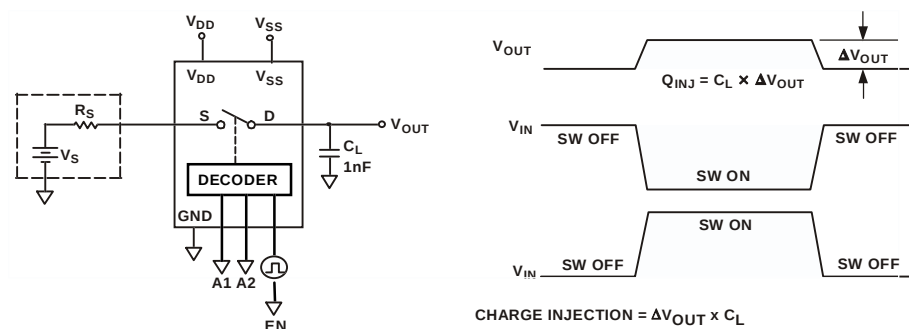
Test Circuit 4. Switching Time of Multiplexer, $t_{\text{TRANSITION}}$



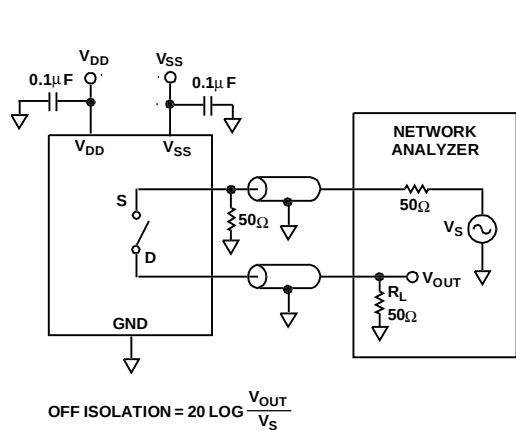
Test Circuit 5. Break-Before-Make Delay, t_{BBM}



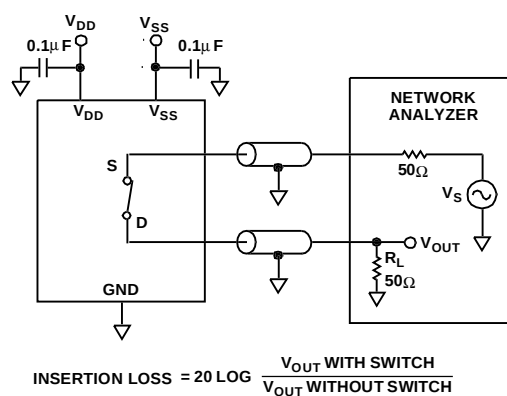
Test Circuit 6. Enable Delay, $t_{\text{ON}}(\text{EN})$, $t_{\text{OFF}}(\text{EN})$



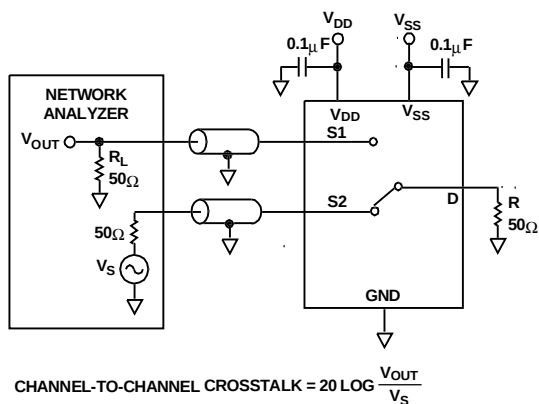
Test Circuit 7. Charge Injection



Test Circuit 8. Off Isolation



Test Circuit 9. Bandwidth



Test Circuit 10. Channel-to-Channel Crosstalk

ADG604

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

14-Lead TSSOP Package (RU-14)

