Dual-Channel High-Speed ESD Protection Device

Check for Samples: TPD2E2U06

FEATURES

- **Provides System-Level ESD Protection for Low-Voltage IO Interface**
- **IEC 61000-4-2 Level 4**
  - **±25 kV (contact discharge)**
  - **±30 kV (air-gap discharge)**
- **IO Capacitance 1.5 pF (Typ)**
- **DC Breakdown Voltage 6.5 V (Min)**
- **Ultra-Low Leakage Current 10 nA (Max)**
- **Low ESD Clamping Voltage**
- **Industrial Temperature Range: –40°C to +125°C**
- **Small Easy-to-Route DRL Package**

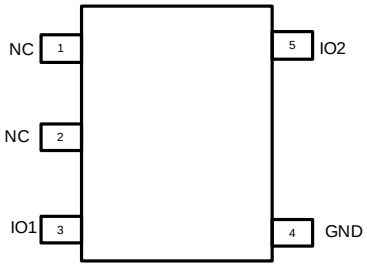
APPLICATIONS

- **Gaming Machines**
- **eBook**
- **Portable Media Players**
- **Digital Camera**

DESCRIPTION

The TPD2E2U06 is a dual-channel ultra-low capacitance ESD-protection device. The device offers ±25-KV IEC contact and ±30-KV IEC air-gap ESD protection. The 1.5-pF line capacitance of the TPD2E2U06 makes the device suitable for a wide range of applications. Typical application interfaces are USB 2.0, LVDS, and I^{2}C™.

DRL
1.65 mm × 1.2 mm × 0.6 mm
(0.5-mm PITCH)



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I^{2}C is a trademark of NXP Semiconductors.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
I_{PP}	Peak pulse current (tp = 8/20 µs)		5.5 (1)	A
P_{PP}	Peak pulse power (tp = 8/20 µs)		85 (1)	W
	IEC 61000-4-2 air-gap ESD		±30 (1)	kV
	IEC 61000-4-2 contact ESD		±25 (1)	kV
	Operating temperature	–40	125	°C
	Storage temperature	–65	155	°C

(1) Measured at 25°C.

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{RWM}	Reverse stand-off voltage	I_{IO} < 10 µA			5.5	V
V_{CLAMP}	IO to GND	I_{PP} = 1 A, TLP (1)		9.7		V
		I_{PP} = 5 A, TLP (1)		12.4		
V_{CLAMP}	GND to IO	I_{PP} = 1 A, TLP (1)		1.9		V
		I_{PP} = 5 A, TLP (1)		4		
R_{DYN}	Dynamic resistance	IO to GND (2)		0.5		Ω
R_{DYN}	Dynamic resistance	GND to IO (2)		0.25		Ω
CL	Line capacitance	f = 1 MHz, V_{BIAS} = 2.5 V (3)		1.5	1.9	pF
C_{CROSS}	Channel-to-channel input capacitance	Pin 4 = 0 V, f = 1 MHz, V_{BIAS} = 2.5 V, between channel pins (3)		0.02	0.03	pF
$\Delta_{CIO-TO-GND}$	Variation of channel input capacitance	Pin 4 = 0 V, f = 1 MHz, V_{BIAS} = 2.5 V, channel_x pin to GND – channel_y pin to GND (3)		0.03	0.1	pF
V_{BR}	Break-down voltage	I_{IO} = 1 mA	6.5		8.5	V
I_{LEAK}	Leakage current	V_{IO} = 2.5 V		1	10	nA

(1) Transmission Line Pulse with 10-ns rise time, 100-ns width.
(2) Extraction of RDYN Using least squares fit of TLP characteristics between I = 20 A and I = 30 A.
(3) Measured at 25°C.

DEVICE INFORMATION

FUNCTIONAL BLOCK DIAGRAM

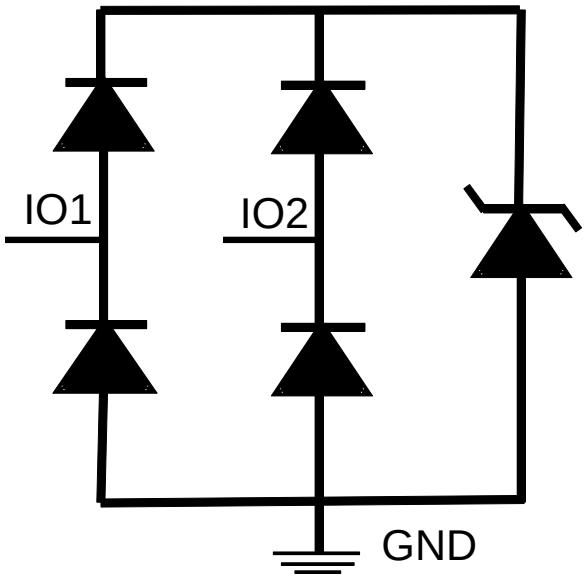


Figure 1. CIRCUIT SCHEMATIC DIAGRAM

PIN FUNCTIONS

PIN		I/O	DESCRIPTION
NAME	NO.		
IO1	3	I/O	The IO1 and IO2 pins are an ESD protected channel. Connect these pins to the data line as close to the connector as possible.
IO2	5	I/O	
NC	1, 2	-	This pin is not connected and is left floating, grounded, or connected to VCC.
GND	4	-	The GND (ground) pin is connected to ground.

TYPICAL CHARACTERISTICS

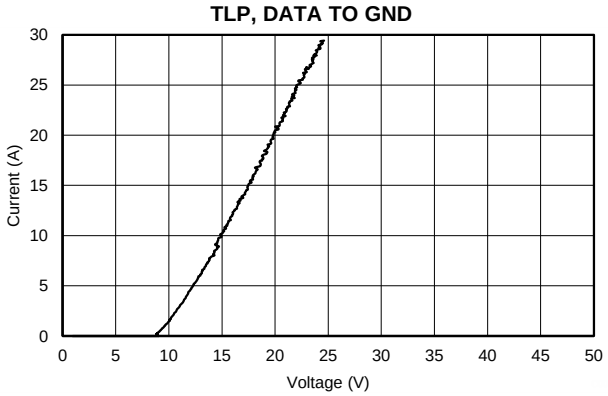


Figure 2.

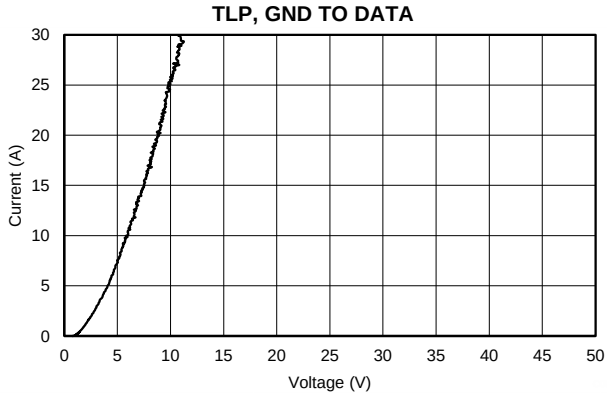


Figure 3.

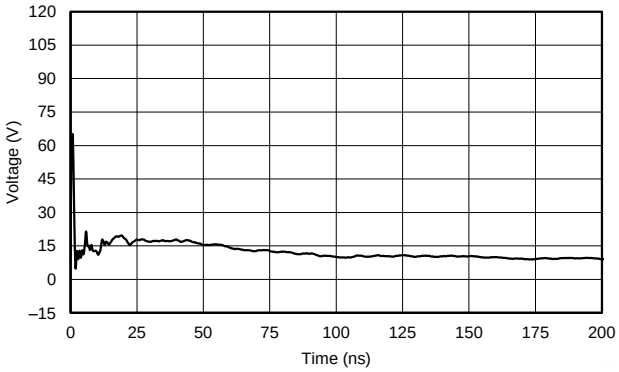


Figure 4.

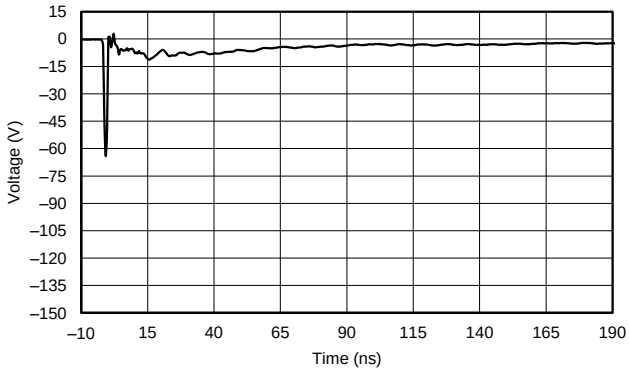


Figure 5.

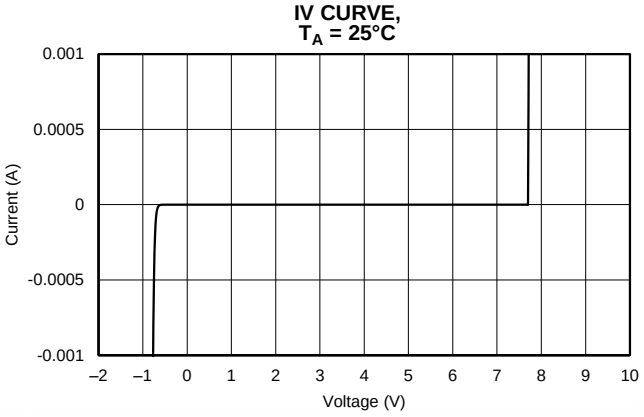


Figure 6.

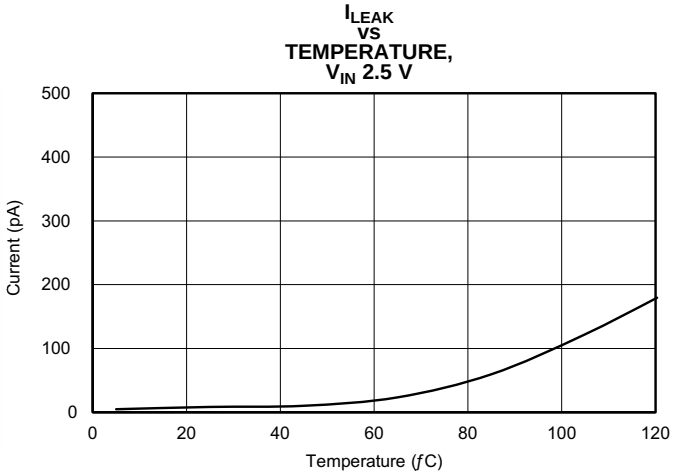


Figure 7.

TYPICAL CHARACTERISTICS (continued)

CAPACITANCE ACROSS V_{BIAS}
f = 1 mHZ

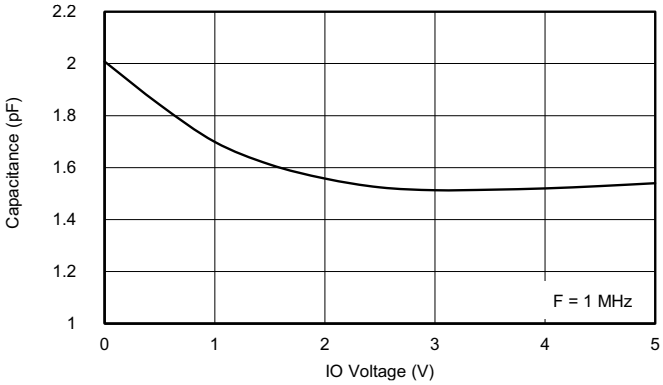


Figure 8.

SURGE CURVE (tp = 8/20 µs)
IO TO GND

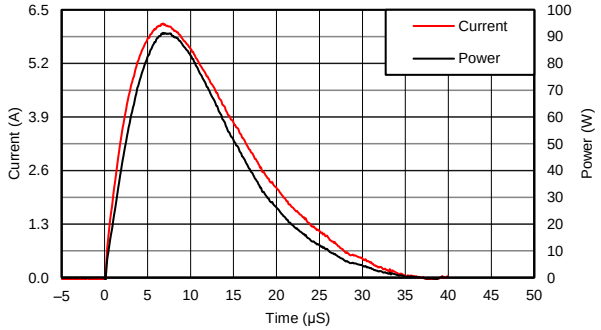


Figure 9.

INSERTION LOSS

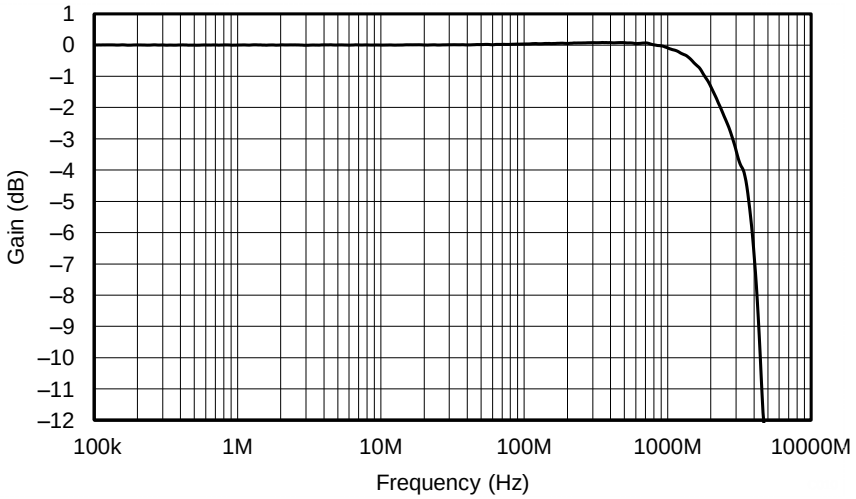


Figure 10.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPD2E2U06DRLR	ACTIVE	SOT	DRL	5	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	DT	Samples
TPD2E2U06DRLR-P	ACTIVE	SOT	DRL	5	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	DT6	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

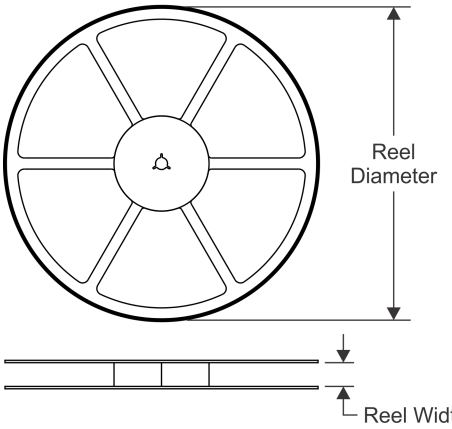
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

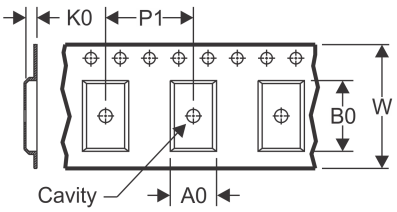
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

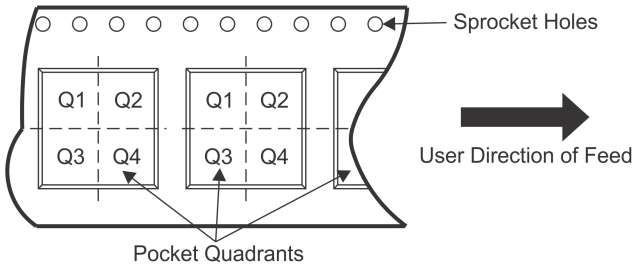


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

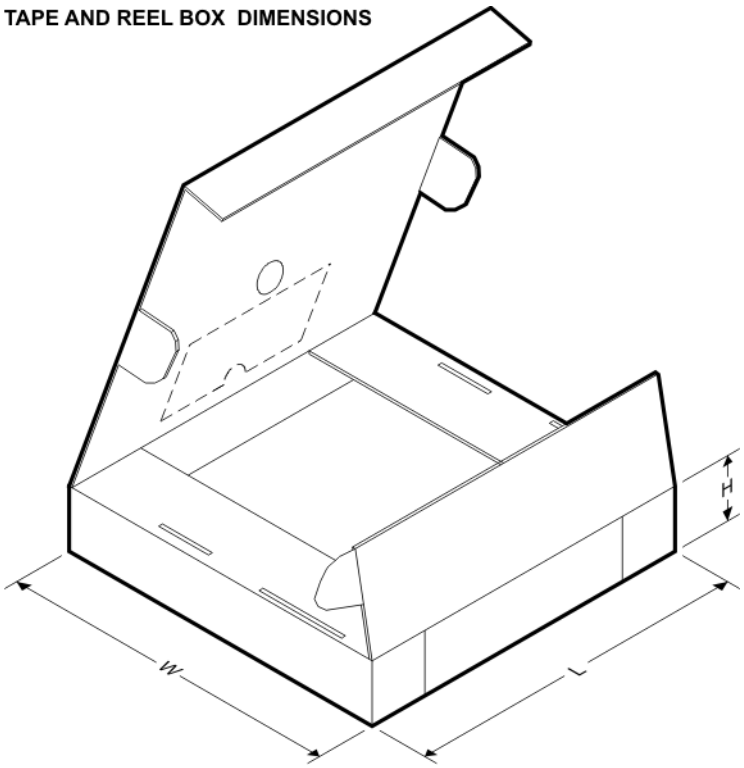
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

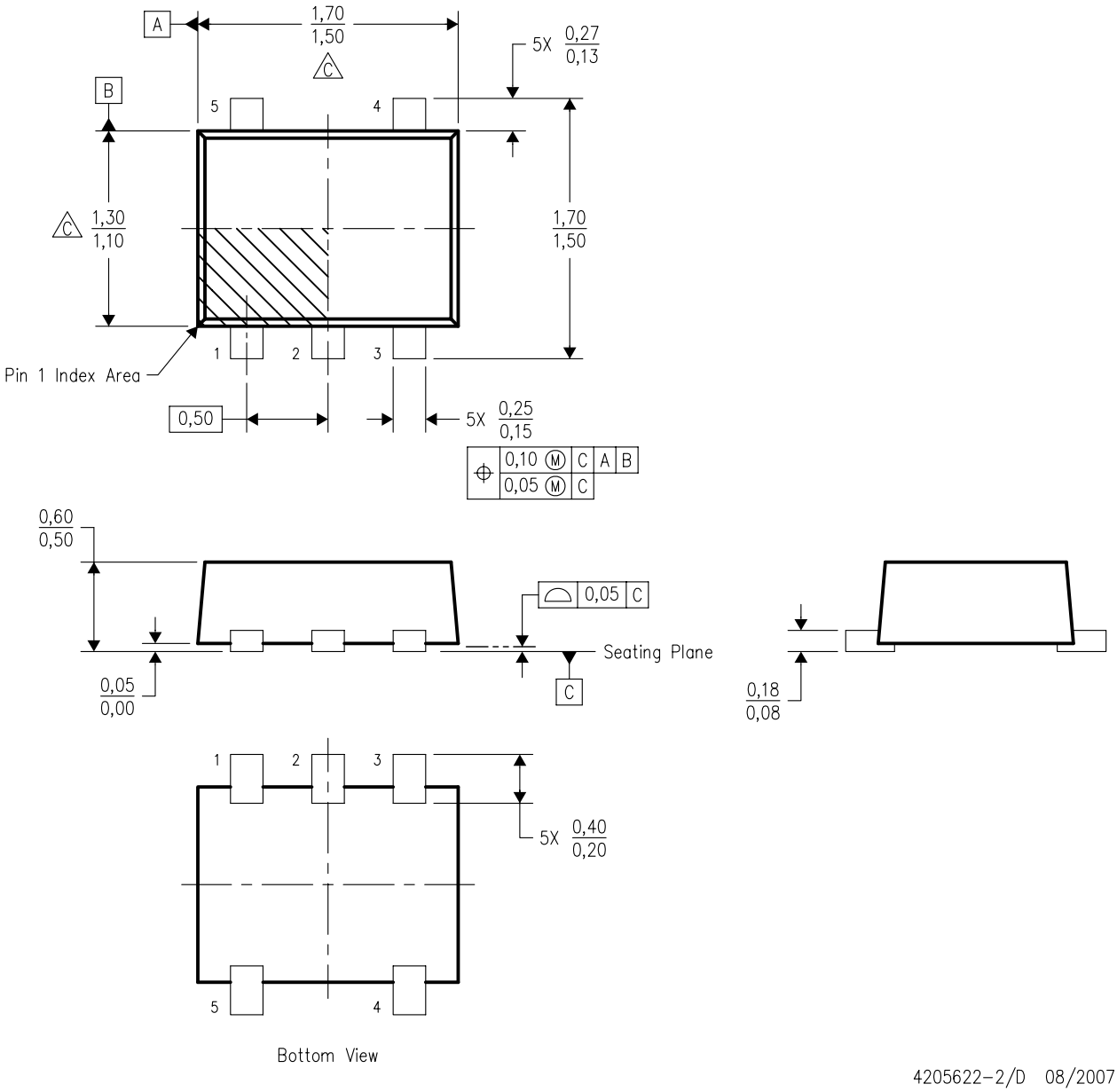
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD2E2U06DRLR	SOT	DRL	5	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
TPD2E2U06DRLR-P	SOT	DRL	5	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD2E2U06DRLR	SOT	DRL	5	4000	202.0	201.0	28.0
TPD2E2U06DRLR-P	SOT	DRL	5	4000	202.0	201.0	28.0



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash, interlead flash, protrusions, or gate burrs. Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0,15 per end or side.
D. JEDEC package registration is pending.

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