CY7C1365CV33

9-Mbit (256K × 32) Flow-Through Sync SRAM

Features

- 256K × 32 common I/O
- 3.3 V core power supply (V_{DD})
- 2.5 V/3.3 V I/O power supply (V_{DDQ})
- Fast clock-to-output times
  - 6.5 ns (133-MHz version)
- Provide high-performance 2-1-1-1 access rate
- User-selectable burst counter supporting Intel® Pentium® interleaved or linear burst sequences
- Separate processor and controller address strobes
- Synchronous self-timed write
- Asynchronous output enable
- Supports 3.3 V I/O level
- Available in JEDEC-standard lead-free 100-pin TQFP package
- TQFP Available with 3-Chip Enable
- "ZZ" Sleep Mode option

Functional Description

The CY7C1365CV33 is a 256K × 32 synchronous cache RAM designed to interface with high-speed microprocessors with minimum glue logic. Maximum access delay from clock rise is 6.5 ns (133-MHz version). A 2-bit on-chip counter captures the first address in a burst and increments the address automatically for the rest of the burst access. All synchronous inputs are gated by registers controlled by a positive-edge-triggered Clock Input (CLK). The synchronous inputs include all addresses, all data inputs, address-pipelining Chip Enable ($\overline{CE}_1$), depth-expansion Chip Enables (CE_2 and $\overline{CE}_3$), Burst Control inputs ($\overline{ADSC}$, $\overline{ADSP}$, and $\overline{ADV}$), Write Enables (BW[A:D], and $\overline{BWE}$), and Global Write ($\overline{GW}$). Asynchronous inputs include the Output Enable ($\overline{OE}$) and the ZZ pin.

The CY7C1365CV33 allows either interleaved or linear burst sequences, selected by the MODE input pin. A HIGH selects an interleaved burst sequence, while a LOW selects a linear burst sequence. Burst accesses can be initiated with the Processor Address Strobe ($\overline{ADSP}$) or the cache Controller Address Strobe ($\overline{ADSC}$) inputs. Address advancement is controlled by the Address Advancement ($\overline{ADV}$) input.

Addresses and Chip Enables are registered at rising edge of clock when either Address Strobe Processor ($\overline{ADSP}$) or Address Strobe Controller ($\overline{ADSC}$) are active. Subsequent burst addresses can be internally generated as controlled by the Advance pin ($\overline{ADV}$).

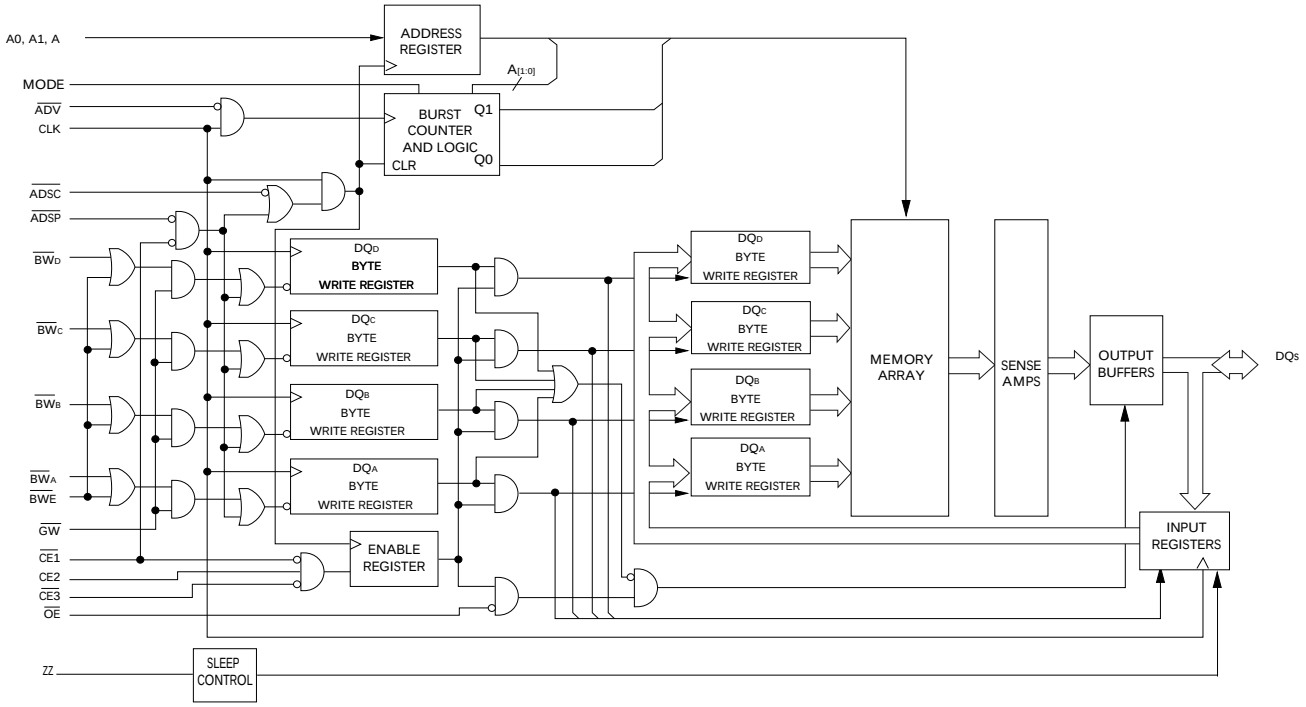
The CY7C1365CV33 operates from a +3.3 V core power supply while all outputs may operate with either a +2.5 or +3.3 V supply. All inputs and outputs are JEDEC-standard JESD8-5-compatible.

For a complete list of related documentation, click here.

Selection Guide

Description	133 MHz	Unit
Maximum Access Time	6.5	ns
Maximum Operating Current	250	mA
Maximum Standby Current	40	mA

Logic Block Diagram – CY7C1365CV33



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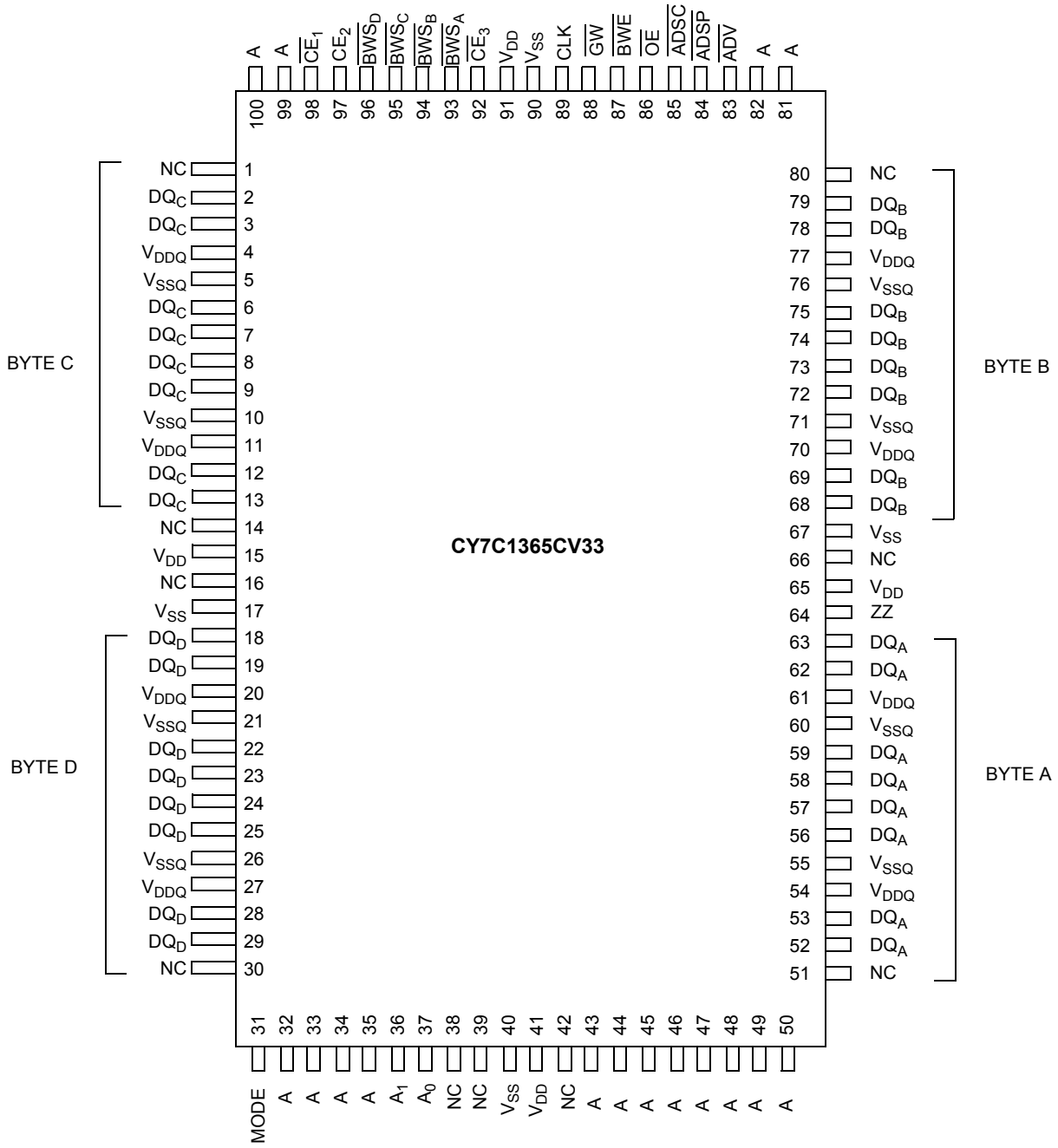
Pin Configurations

Figure 1. 100-pin TQFP (14 × 20 × 1.4 mm) pinout (3 Chip Enable) (A version)



Pin Descriptions

Name	100-pin TQFP	I/O	Description
A0, A1, A	37, 36, 32, 33, 34, 35, 44, 45, 46, 47, 48, 49, 50, 81, 82, 99, 100, 92 (for 2 Chip Enable Version), 43 (for 3 Chip Enable Version)	Input-Synchronous	**Address Inputs used to select one of the 256K address locations**. Sampled at the rising edge of the CLK if $\overline{ADSP}$ or $\overline{ADSC}$ is active LOW, and $\overline{CE_1}$, CE_2, and $\overline{CE_3}$ are sampled active. $A_{[1:0]}$ feed the 2-bit counter.
$\overline{BW_A}$, $\overline{BW_B}$, $\overline{BW_C}$, $\overline{BW_D}$	93, 94, 95, 96	Input-Synchronous	**Byte Write Select Inputs, active LOW**. Qualified with $\overline{BWE}$ to conduct Byte Writes to the SRAM. Sampled on the rising edge of CLK.
$\overline{GW}$	88	Input-Synchronous	**Global Write Enable Input, active LOW**. When asserted LOW on the rising edge of CLK, a global write is conducted (ALL bytes are written, regardless of the values on $\overline{BW_{[A:D]}}$ and $\overline{BWE}$).
$\overline{BWE}$	87	Input-Synchronous	**Byte Write Enable Input, active LOW**. Sampled on the rising edge of CLK. This signal must be asserted LOW to conduct a Byte Write.
CLK	89	Input-Clock	**Clock Input**. Used to capture all synchronous inputs to the device. Also used to increment the burst counter when $\overline{ADV}$ is asserted LOW, during a burst operation.
$\overline{CE_1}$	98	Input-Synchronous	**Chip Enable 1 Input, active LOW**. Sampled on the rising edge of CLK. Used in conjunction with CE_2 and $\overline{CE_3}$ to select/deselect the device. $\overline{ADSP}$ is ignored if $\overline{CE_1}$ is HIGH. $\overline{CE_1}$ is sampled only when a new external address is loaded.
CE_2	97	Input-Synchronous	**Chip Enable 2 Input, active HIGH**. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE_1}$ and $\overline{CE_3}$ to select/deselect the device. CE_2 is sampled only when a new external address is loaded.
$\overline{CE_3}$	92 (for 3 Chip Enable Version)	Input-Synchronous	**Chip Enable 3 Input, active LOW**. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE_1}$ and CE_2 to select/deselect the device. $\overline{CE_3}$ is sampled only when a new external address is loaded.
$\overline{OE}$	86	Input-Asynchronous	**Output Enable, asynchronous input, active LOW**. Controls the direction of the I/O pins. When LOW, the I/O pins behave as outputs. When deasserted HIGH, I/O pins are tri-stated, and act as input data pins. $\overline{OE}$ is masked during the first clock of a Read cycle when emerging from a deselected state.
$\overline{ADV}$	83	Input-Synchronous	**Advance Input signal, sampled on the rising edge of CLK**. When asserted, it automatically increments the address in a burst cycle.
$\overline{ADSP}$	84	Input-Synchronous	**Address Strobe from Processor, sampled on the rising edge of CLK, active LOW**. When asserted LOW, addresses presented to the device are captured in the address registers. $A_{[1:0]}$ are also loaded into the burst counter. When $\overline{ADSP}$ and $\overline{ADSC}$ are both asserted, only $\overline{ADSP}$ is recognized. $\overline{ASDP}$ is ignored when $\overline{CE_1}$ is deasserted HIGH.
$\overline{ADSC}$	85	Input-Synchronous	**Address Strobe from Controller, sampled on the rising edge of CLK, active LOW**. When asserted LOW, addresses presented to the device are captured in the address registers. $A_{[1:0]}$ are also loaded into the burst counter. When $\overline{ADSP}$ and $\overline{ADSC}$ are both asserted, only $\overline{ADSP}$ is recognized.
ZZ	64	Input-Asynchronous	**ZZ "sleep" Input, active HIGH**. When asserted HIGH places the device in a non-time-critical "sleep" condition with data integrity preserved. For normal operation, this pin has to be LOW or left floating. ZZ pin has an internal pull-down.

Pin Descriptions (continued)

Name	100-pin TQFP	I/O	Description
DQs	52, 53, 56, 57, 58, 59, 62, 63, 68, 69, 72, 73, 74, 75, 78, 79, 2, 3, 6, 7, 8, 9, 12, 13, 18, 19, 22, 23, 24, 25, 28, 29	I/O-Synchronous	**Bidirectional Data I/O lines**. As inputs, they feed into an on-chip data register that is triggered by the rising edge of CLK. As outputs, they deliver the data contained in the memory location specified by the addresses presented during the previous clock rise of the read cycle. The direction of the pins is controlled by $\overline{OE}$. When $\overline{OE}$ is asserted LOW, the pins behave as outputs. When HIGH, DQs are placed in a tri-state condition.
V_{DD}	15, 41, 65, 91	Power Supply	**Power supply inputs to the core of the device**.
V_{SS}	17, 40, 67, 90	Ground	**Ground for the core of the device**.
V_{DDQ}	4, 11, 20, 27, 54, 61, 70, 77	I/O Power Supply	**Power supply for the I/O circuitry**.
V_{SSQ}	5, 10, 21, 26, 55, 60, 71, 76	I/O Ground	**Ground for the I/O circuitry**.
MODE	31	Input-Static	**Selects Burst Order**. When tied to GND selects linear burst sequence. When tied to V_{DD} or left floating selects interleaved burst sequence. This is a strap pin and should remain static during device operation. Mode Pin has an internal pull-up.
NC	1, 30, 51, 80, 14, 16, 38, 39, 42, 66, 43 (for 2 Chip Enable Version)		**No Connects**. Not Internally connected to the die.

Functional Overview

All synchronous inputs pass through input registers controlled by the rising edge of the clock. Maximum access delay from the clock rise (t_{CDV}) is 6.5 ns (133-MHz device).

The CY7C1365CV33 supports secondary cache in systems utilizing either a linear or interleaved burst sequence. The interleaved burst order supports Pentium and i486 processors. The linear burst sequence is suited for processors that utilize a linear burst sequence. The burst order is user-selectable, and is determined by sampling the MODE input. Accesses can be initiated with either the Processor Address Strobe ($\overline{ADSP}$) or the Controller Address Strobe ($\overline{ADSC}$). Address advancement through the burst sequence is controlled by the $\overline{ADV}$ input. A two-bit on-chip wraparound burst counter captures the first address in a burst sequence and automatically increments the address for the rest of the burst access.

Byte write operations are qualified with the Byte Write Enable ($\overline{BWE}$) and Byte Write Select ($\overline{BW}$[A:D]) inputs. A Global Write Enable ($\overline{GW}$) overrides all byte write inputs and writes data to all four bytes. All writes are simplified with on-chip synchronous self-timed write circuitry.

Three synchronous Chip Selects ($\overline{CE_1}$, CE_2, $\overline{CE_3}$) and an asynchronous Output Enable ($\overline{OE}$) provide for easy bank selection and output tri-state control. $\overline{ADSP}$ is ignored if $\overline{CE_1}$ is HIGH.

Single Read Accesses

A single read access is initiated when the following conditions are satisfied at clock rise: (1) $\overline{CE_1}$, CE_2, and $\overline{CE_3}$ are all asserted active, and (2) $\overline{ADSP}$ or $\overline{ADSC}$ is asserted LOW (if the access is initiated by $\overline{ADSC}$, the write inputs must be deasserted during this first cycle). The address presented to the address inputs is latched into the address register and the burst counter/control logic and presented to the memory core. If the $\overline{OE}$ input is asserted LOW, the requested data will be available at the data outputs a maximum to t_{CDV} after clock rise. $\overline{ADSP}$ is ignored if $\overline{CE_1}$ is HIGH.

Single Write Accesses Initiated by $\overline{ADSP}$

This access is initiated when the following conditions are satisfied at clock rise: (1) $\overline{CE_1}$, CE_2, $\overline{CE_3}$ are all asserted active, and (2) $\overline{ADSP}$ is asserted LOW. The addresses presented are loaded into the address register and the burst inputs ($\overline{GW}$, $\overline{BWE}$, and $\overline{BW}$[A:D]) are ignored during this first clock cycle. If the write inputs are asserted active (see Write Cycle Descriptions table for appropriate states that indicate a write) on the next clock rise, the appropriate data will be latched and written into the device.Byte writes are allowed. During byte writes, $\overline{BWA}$ controls DQA and $\overline{BWB}$ controls DQB, $\overline{BWC}$ controls DQC, and $\overline{BWD}$ controls DQD. All I/Os are tri-stated during a byte write.Since this is a common I/O device, the asynchronous $\overline{OE}$ input signal must be deasserted and the I/Os must be tri-stated prior to the presentation of data to DQs. As a safety precaution, the data lines are tri-stated once a write cycle is detected, regardless of the state of $\overline{OE}$.

Single Write Accesses Initiated by $\overline{ADSC}$

This write access is initiated when the following conditions are satisfied at clock rise: (1) $\overline{CE_1}$, CE_2, and $\overline{CE_3}$ are all asserted active, (2) $\overline{ADSC}$ is asserted LOW, (3) $\overline{ADSP}$ is deasserted HIGH, and (4) the write input signals ($\overline{GW}$, $\overline{BWE}$, and $\overline{BW}$[A:D]) indicate a write access. $\overline{ADSC}$ is ignored if $\overline{ADSP}$ is active LOW.

The addresses presented are loaded into the address register and the burst counter/control logic and delivered to the memory core. The information presented to DQ[D:A] will be written into the specified address location. Byte writes are allowed. During byte writes, BWA controls DQA, BWB controls DQB, BWC controls DQC, and BWD controls DQD. All I/Os are tri-stated when a write is detected, even a byte write. Since this is a common I/O device, the asynchronous OE input signal must be deasserted and the I/Os must be tri-stated prior to the presentation of data to DQs. As a safety precaution, the data lines are tri-stated once a write cycle is detected, regardless of the state of OE.

Burst Sequences

The CY7C1365CV33 provides an on-chip two-bit wraparound burst counter inside the SRAM. The burst counter is fed by A[1:0], and can follow either a linear or interleaved burst order. The burst order is determined by the state of the MODE input. A LOW on MODE will select a linear burst sequence. A HIGH on MODE will select an interleaved burst order. Leaving MODE unconnected will cause the device to default to a interleaved burst sequence.

Sleep Mode

The ZZ input pin is an asynchronous input. Asserting ZZ places the SRAM in a power conservation “sleep” mode. Two clock cycles are required to enter into or exit from this “sleep” mode. While in this mode, data integrity is guaranteed. Accesses pending when entering the “sleep” mode are not considered valid nor is the completion of the operation guaranteed. The device must be deselected prior to entering the “sleep” mode. CEs, ADSP, and ADSC must remain inactive for the duration of t_{ZZREC} after the ZZ input returns LOW.

Interleaved Burst Address Table

(MODE = Floating or V_{DD})

First Address A1:A0	Second Address A1:A0	Third Address A1:A0	Fourth Address A1:A0
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

Linear Burst Address Table

(MODE = GND)

First Address A1:A0	Second Address A1:A0	Third Address A1:A0	Fourth Address A1:A0
00	01	10	11
01	10	11	00
10	11	00	01
11	00	01	10

ZZ Mode Electrical Characteristics

Parameter	Description	Test Conditions	Min	Max	Unit
I_{DDZZ}	Sleep mode standby current	ZZ ≥ V_{DD} – 0.2 V	–	50	mA
t_{ZZS}	Device operation to ZZ	ZZ ≥ V_{DD} – 0.2 V	–	$2t_{CYC}$	ns
t_{ZZREC}	ZZ recovery time	ZZ ≤ 0.2 V	$2t_{CYC}$	–	ns
t_{ZZI}	ZZ Active to Sleep current	This parameter is sampled	–	$2t_{CYC}$	ns
t_{RZZI}	ZZ Inactive to exit Sleep current	This parameter is sampled	0	–	ns

Truth Table

The truth table for CY7C1365CV33 follows. [1, 2, 3, 4, 5]

Cycle Description	Address Used	$\overline{CE_1}$	$\overline{CE_3}$	CE_2	ZZ	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$	$\overline{OE}$	CLK	DQ
Deselected Cycle, Power-down	None	H	X	X	L	X	L	X	X	X	L–H	Tri-State
Deselected Cycle, Power-down	None	L	X	L	L	L	X	X	X	X	L–H	Tri-State
Deselected Cycle, Power-down	None	L	H	X	L	L	X	X	X	X	L–H	Tri-State
Deselected Cycle, Power-down	None	L	X	L	L	H	L	X	X	X	L–H	Tri-State
Deselected Cycle, Power-down	None	X	X	H	L	H	L	X	X	X	L–H	Tri-State
Sleep Mode, Power-down	None	X	X	X	H	X	X	X	X	X	X	Tri-State
Read Cycle, Begin Burst	External	L	L	H	L	L	X	X	X	L	L–H	Q
Read Cycle, Begin Burst	External	L	L	H	L	L	X	X	X	H	L–H	Tri-State
Write Cycle, Begin Burst	External	L	L	H	L	H	L	X	L	X	L–H	D
Read Cycle, Begin Burst	External	L	L	H	L	H	L	X	H	L	L–H	Q
Read Cycle, Begin Burst	External	L	L	H	L	H	L	X	H	H	L–H	Tri-State
Read Cycle, Continue Burst	Next	X	X	X	L	H	H	L	H	L	L–H	Q
Read Cycle, Continue Burst	Next	X	X	X	L	H	H	L	H	H	L–H	Tri-State
Read Cycle, Continue Burst	Next	H	X	X	L	X	H	L	H	L	L–H	Q
Read Cycle, Continue Burst	Next	H	X	X	L	X	H	L	H	H	L–H	Tri-State
Write Cycle, Continue Burst	Next	X	X	X	L	H	H	L	L	X	L–H	D
Write Cycle, Continue Burst	Next	H	X	X	L	X	H	L	L	X	L–H	D
Read Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	H	L	L–H	Q
Read Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	H	H	L–H	Tri-State
Read Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	H	L	L–H	Q
Read Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	H	H	L–H	Tri-State
Write Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	L	X	L–H	D
Write Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	L	X	L–H	D

Notes

1. X = "Don't Care." H = Logic HIGH, L = Logic LOW.
2. $\overline{WRITE}$ = L when any one or more Byte Write Enable signals ($\overline{BW_A}$, $\overline{BW_B}$, $\overline{BW_C}$, $\overline{BW_D}$) and $\overline{BWE}$ = L or $\overline{GW}$ = L. $\overline{WRITE}$ = H when all Byte Write Enable signals ($\overline{BW_A}$, $\overline{BW_B}$, $\overline{BW_C}$, $\overline{BW_D}$), $\overline{BWE}$, $\overline{GW}$ = H.
3. The DQ pins are controlled by the current cycle and the $\overline{OE}$ signal. $\overline{OE}$ is asynchronous and is not sampled with the clock.
4. The SRAM always initiates a Read cycle when $\overline{ADSP}$ is asserted, regardless of the state of $\overline{GW}$, $\overline{BWE}$, or $\overline{BW_{[A:D]}}$. Writes may occur only on subsequent clocks after the $\overline{ADSP}$ or with the assertion of $\overline{ADSC}$. As a result, $\overline{OE}$ must be driven HIGH prior to the start of the write cycle to allow the outputs to tri-state. $\overline{OE}$ is a don't care for the remainder of the Write cycle.
5. $\overline{OE}$ is asynchronous and is not sampled with the clock rise. It is masked internally during Write cycles. During a read cycle all data bits are Tri-State when $\overline{OE}$ is inactive or when the device is deselected, and all data bits behave as output when $\overline{OE}$ is active (LOW).

Truth Table for Read/Write

The Truth Table for Read/Write for CY7C1365CV33 follows. [6, 7]

Function	$\overline{GW}$	$\overline{BWE}$	$\overline{BW_D}$	$\overline{BW_C}$	$\overline{BW_B}$	$\overline{BW_A}$
Read	H	H	X	X	X	X
Read	H	L	H	H	H	H
Write Byte (A, DQP_A)	H	L	H	H	H	L
Write Byte (B, DQP_B)	H	L	H	H	L	H
Write Bytes (B, A, DQP_A, DQP_B)	H	L	H	H	L	L
Write Byte (C, DQP_C)	H	L	H	L	H	H
Write Bytes (C, A, DQP_C, DQP_A)	H	L	H	L	H	L
Write Bytes (C, B, DQP_C, DQP_B)	H	L	H	L	L	H
Write Bytes (C, B, A, DQP_C, DQP_B, DQP_A)	H	L	H	L	L	L
Write Byte (D, DQP_D)	H	L	L	H	H	H
Write Bytes (D, A, DQP_D, DQP_A)	H	L	L	H	H	L
Write Bytes (D, B, DQP_D, DQP_A)	H	L	L	H	L	H
Write Bytes (D, B, A, DQP_D, DQP_B, DQP_A)	H	L	L	H	L	L
Write Bytes (D, B, DQP_D, DQP_B)	H	L	L	L	H	H
Write Bytes (D, B, A, DQP_D, DQP_C, DQP_A)	H	L	L	L	H	L
Write Bytes (D, C, A, DQP_D, DQP_B, DQP_A)	H	L	L	L	L	H
Write All Bytes	H	L	L	L	L	L
Write All Bytes	L	X	X	X	X	X

Notes

6. X = "Don't Care." H = Logic HIGH, L = Logic LOW.
7. $\overline{WRITE}$ = L when any one or more Byte Write Enable signals ($\overline{BW_A}$, $\overline{BW_B}$, $\overline{BW_C}$, $\overline{BW_D}$) and $\overline{BWE}$ = L or $\overline{GW}$ = L. $\overline{WRITE}$ = H when all Byte Write Enable signals ($\overline{BW_A}$, $\overline{BW_B}$, $\overline{BW_C}$, $\overline{BW_D}$), $\overline{BWE}$, $\overline{GW}$ = H.

Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. User guidelines are not tested.

Storage Temperature ..... –65 °C to +150 °C

Ambient Temperature with Power Applied ..... –55 °C to +125 °C

Supply Voltage on V_{DD} Relative to GND .....–0.5 V to +4.6 V

Supply Voltage on V_{DDQ} Relative to GND .... –0.5 V to +V_{DD}

DC Voltage Applied to Outputs in Tri-State .....–0.5 V to V_{DDQ} + 0.5 V

DC Input Voltage .....–0.5 V to V_{DD} + 0.5 V

Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage (per MIL-STD-883, Method 3015) .....>2001 V

Latch-up Current .....>200 mA

Operating Range

Range	Ambient Temperature	V_{DD}	V_{DDQ}
Commercial	0 °C to +70 °C	3.3 V – 5% / + 10%	2.5 V – 5% to V_{DD}

Electrical Characteristics

Over the Operating Range

Parameter [8, 9]	Description	Test Conditions		CY7C1365CV33		Unit
				Min	Max	
V_{DD}	Power Supply Voltage			3.135	3.6	V
V_{DDQ}	I/O Supply Voltage	for 3.3 V I/O		3.135	3.6	V
		for 2.5 V I/O		2.375	2.625	V
V_{OH}	Output HIGH Voltage	for 3.3 V I/O, I_{OH} = –4.0 mA		2.4	–	V
		for 2.5 V I/O, I_{OH} = –1.0 mA		2.0	–	V
V_{OL}	Output LOW Voltage	for 3.3 V I/O, I_{OL} = 8.0 mA		–	0.4	V
		for 2.5 V I/O, I_{OL} = 1.0 mA		–	0.4	V
V_{IH}	Input HIGH Voltage	for 3.3 V I/O		2.0	V_{DD} + 0.3	V
		for 2.5 V I/O		1.7	V_{DD} + 0.3	V
V_{IL}	Input LOW Voltage [8]	for 3.3 V I/O		–0.3	0.8	V
		for 2.5 V I/O		–0.3	0.7	V
I_X	Input Leakage Current except ZZ and MODE	GND ≤ V_I ≤ V_{DDQ}		–5	5	µA
	Input Current of MODE	Input = V_{SS}		–30	–	µA
		Input = V_{DD}		–	5	µA
	Input Current of ZZ	Input = V_{SS}		–5	–	µA
		Input = V_{DD}		–	30	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{DDQ}, Output Disabled		–5	5	µA
I_{DD}	V_{DD} Operating Supply Current	V_{DD} = Max, I_{OUT} = 0 mA, f = f_{MAX} = 1/t_{CYC}	7.5-ns cycle, 133 MHz	–	250	mA
I_{SB1}	Automatic CE Power-Down Current – TTL Inputs	Max. V_{DD}, Device Deselected, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}, inputs switching	7.5-ns cycle, 133 MHz	100	110	mA
I_{SB2}	Automatic CE Power-Down Current – CMOS Inputs	Max. V_{DD}, Device Deselected, V_{IN} ≥ V_{DD} – 0.3 V or V_{IN} ≤ 0.3 V, f = 0, inputs static	7.5-ns cycle, 133 MHz	–	40	mA

Notes

8. Overshoot: $V_{IH(AC)}$ < V_{DD} + 1.5 V (Pulse width less than t_{CYC}/2), undershoot: $V_{IL(AC)}$ > –2 V (Pulse width less than t_{CYC}/2).
9. $T_{Power\text{-}up}$: Assumes a linear ramp from 0 V to $V_{DD(min)}$ within 200 ms. During this time V_{IH} < V_{DD} and V_{DDQ} ≤ V_{DD}.

Electrical Characteristics (continued)

Over the Operating Range

Parameter [8, 9]	Description	Test Conditions		CY7C1365CV33		Unit
				Min	Max	
I_{SB3}	Automatic CE Power-Down Current – CMOS Inputs	Max. V_{DD}, Device Deselected, $V_{IN} \geq V_{DDQ} - 0.3$ V or $V_{IN} \leq 0.3$ V, f = f_{MAX}, inputs switching	7.5-ns cycle, 133 MHz	–	100	mA
I_{SB4}	Automatic CE Power-Down Current – TTL Inputs	Max. V_{DD}, Device Deselected, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, f = 0, inputs static.	7.5-ns cycle, 133 MHz	–	40	mA

Capacitance

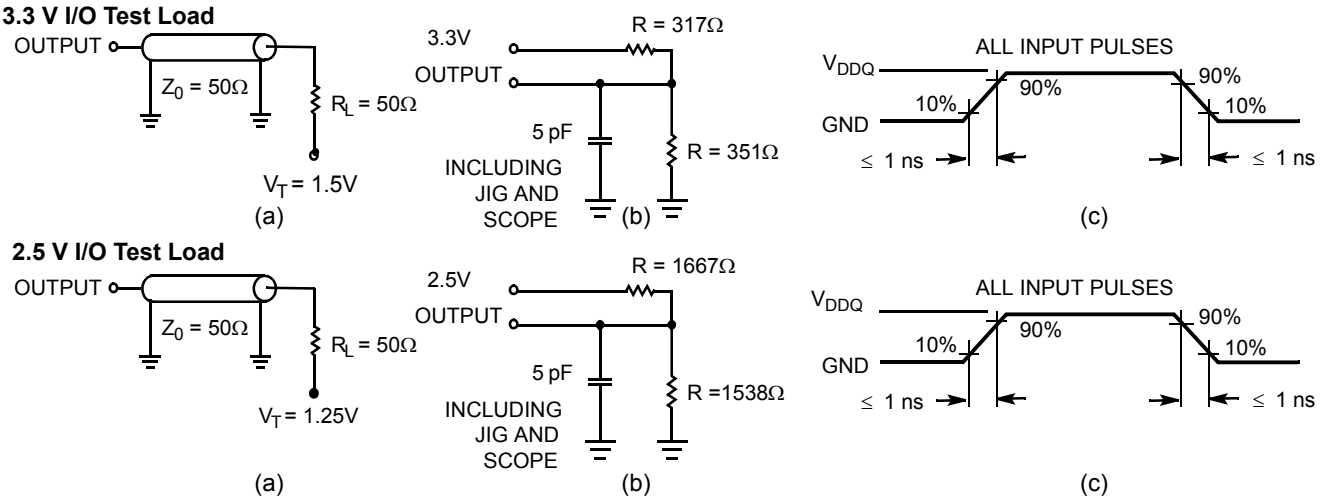
Parameter [10]	Description	Test Conditions	100-pin TQFP Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{DD} = 3.3 V, V_{DDQ} = 2.5 V	5	pF
C_{CLK}	Clock input capacitance		5	pF
$C_{I/O}$	Input/Output capacitance		5	pF

Thermal Resistance

Parameter [10]	Description	Test Conditions	100-pin TQFP Package	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51	29.41	°C/W
Θ_{JC}	Thermal resistance (junction to case)		6.13	°C/W

AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms



Note
10. Tested initially and after any design or process change that may affect these parameters.

Switching Characteristics

Over the Operating Range

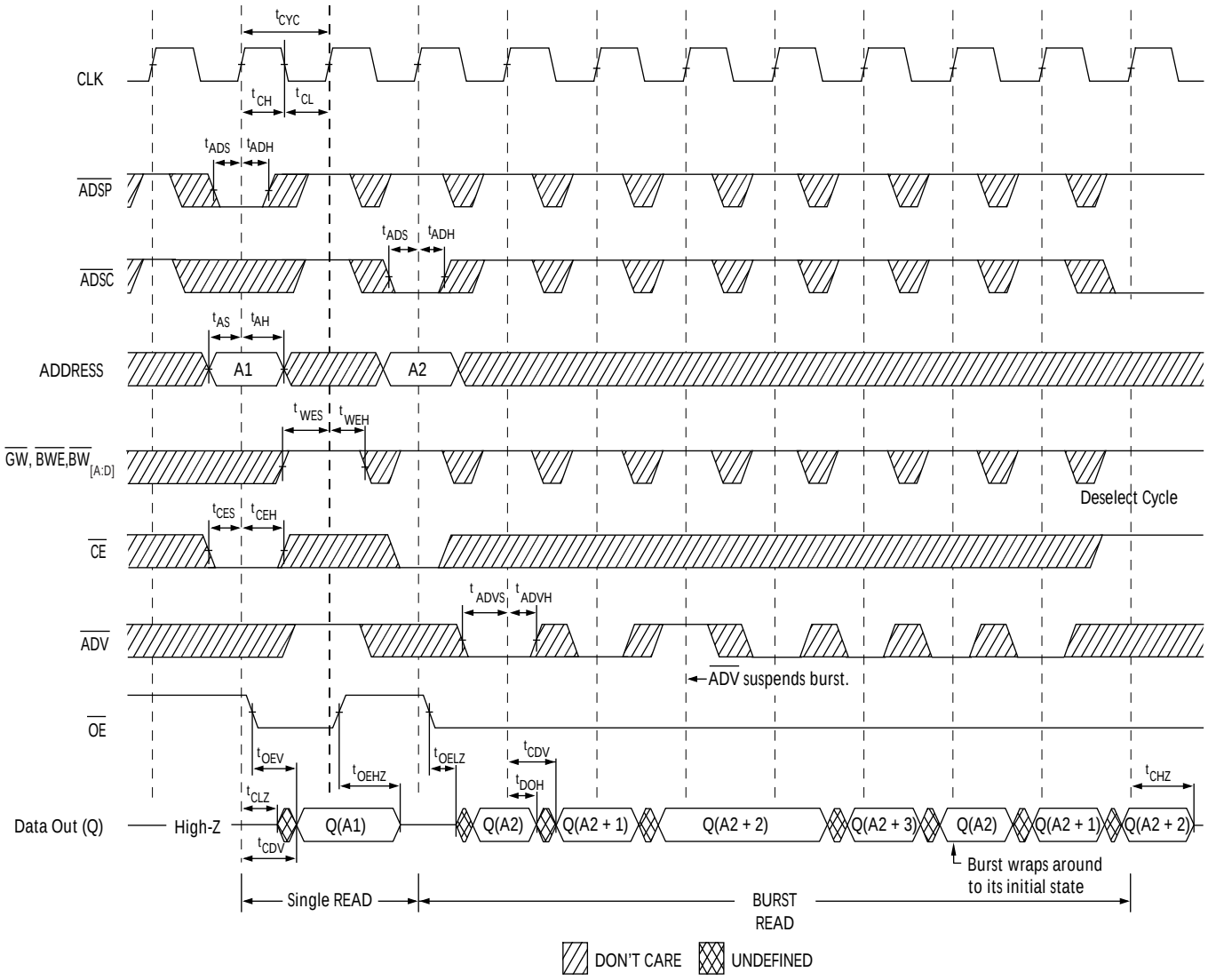
Parameter [11, 12]	Description	-133		Unit
		Min	Max	
t_{POWER}	V_{DD}(typical) to the first access [13]	1	–	ms
Clock				
t_{CYC}	Clock cycle time	7.5	–	ns
t_{CH}	Clock HIGH	3.0	–	ns
t_{CL}	Clock LOW	3.0	–	ns
Output Times				
t_{CDV}	Data output valid after CLK rise	–	6.5	ns
t_{DOH}	Data output hold after CLK rise	2.0	–	ns
t_{CLZ}	Clock to low Z [14, 15, 16]	0	–	ns
t_{CHZ}	Clock to high Z [14, 15, 16]	–	3.5	ns
t_{OEV}	$\overline{OE}$ LOW to output valid	–	3.5	ns
t_{OELZ}	$\overline{OE}$ LOW to output low Z [14, 15, 16]	0	–	ns
t_{OEHZ}	$\overline{OE}$ HIGH to output high Z [14, 15, 16]	–	3.5	ns
Set-up Times				
t_{AS}	Address set-up before CLK rise	1.5	–	ns
t_{ADS}	$\overline{ADSP}$, $\overline{ADSC}$ set-up before CLK rise	1.5	–	ns
t_{ADVS}	$\overline{ADV}$ set-up before CLK rise	1.5	–	ns
t_{WES}	$\overline{GW}$, $\overline{BWE}$, $\overline{BW}_{[A:D]}$ set-up before CLK rise	1.5	–	ns
t_{DS}	Data input set-up before CLK rise	1.5	–	ns
t_{CES}	Chip enable set-up	1.5	–	ns
Hold Times				
t_{AH}	Address hold after CLK rise	0.5	–	ns
t_{ADH}	$\overline{ADSP}$, $\overline{ADSC}$ hold after CLK rise	0.5	–	ns
t_{WEH}	$\overline{GW}$, $\overline{BWE}$, $\overline{BW}_{[A:D]}$ hold after CLK rise	0.5	–	ns
t_{ADVH}	$\overline{ADV}$ hold after CLK rise	0.5	–	ns
t_{DH}	Data input hold after CLK rise	0.5	–	ns
t_{CEH}	Chip enable hold after CLK rise	0.5	–	ns

Notes

11. Timing reference level is 1.5 V when V_{DDQ} = 3.3 V and is 1.25 V when V_{DDQ} = 2.5 V.
12. Test conditions shown in (a) of Figure 2 on page 11 unless otherwise noted.
13. This part has a voltage regulator internally; t_{POWER} is the time that the power needs to be supplied above $V_{DD(minimum)}$ initially before a Read or Write operation can be initiated.
14. t_{CHZ}, t_{CLZ},t_{OELZ}, and t_{OEHZ} are specified with AC test conditions shown in part (b) of Figure 2 on page 11. Transition is measured ±200 mV from steady-state voltage.
15. At any given voltage and temperature, t_{OEHZ} is less than t_{OELZ} and t_{CHZ} is less than t_{CLZ} to eliminate bus contention between SRAMs when sharing the same data bus. These specifications do not imply a bus contention condition, but reflect parameters guaranteed over worst case user conditions. Device is designed to achieve High Z prior to Low Z under the same system conditions.
16. This parameter is sampled and not 100% tested.

Timing Diagrams

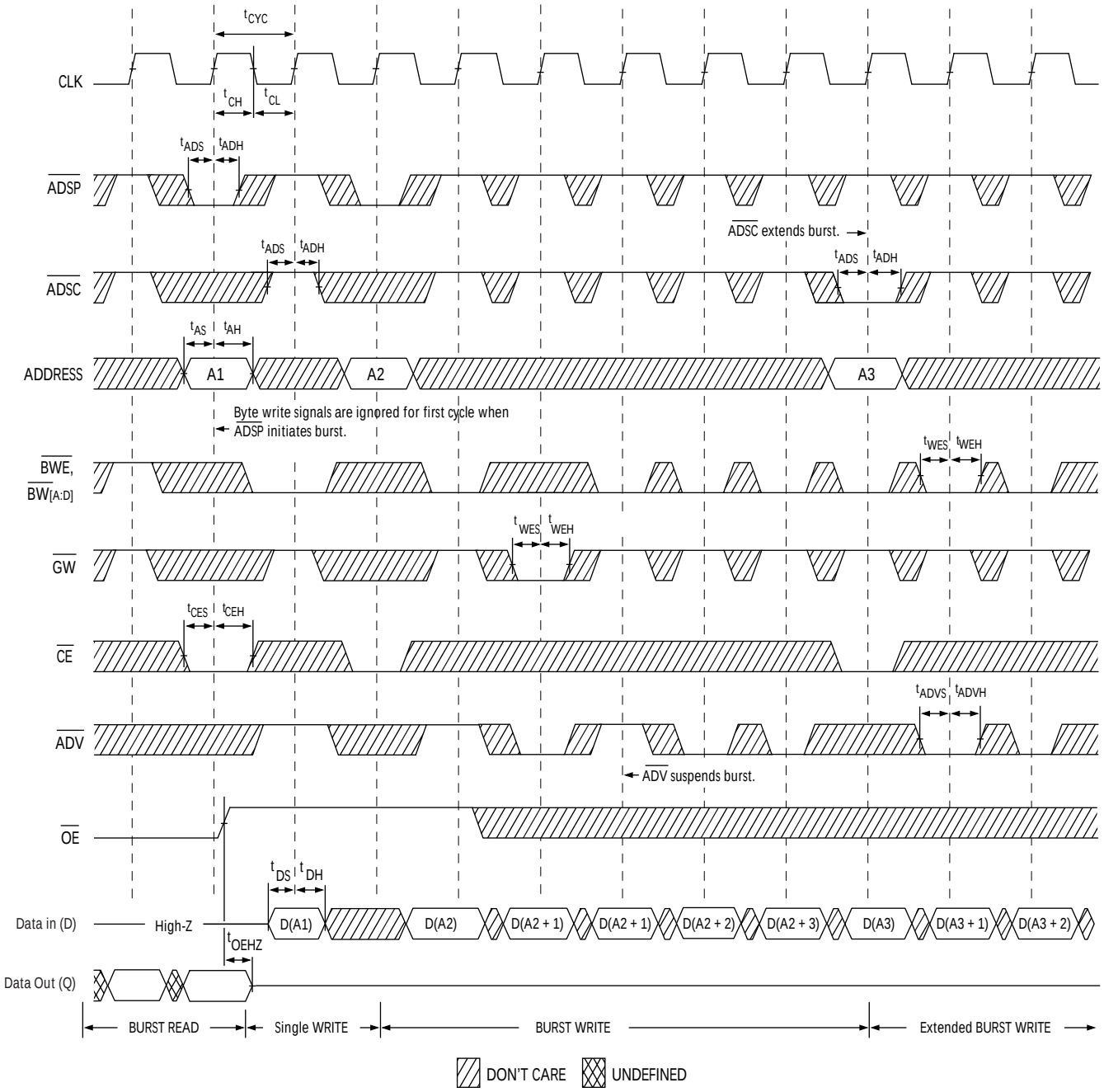
Figure 3. Read Cycle Timing [17]



Note
17. On this diagram, when $\overline{CE}$ is LOW, $\overline{CE}_1$ is LOW, CE_2 is HIGH and $\overline{CE}_3$ is LOW. When $\overline{CE}$ is HIGH, $\overline{CE}_1$ is HIGH or CE_2 is LOW or $\overline{CE}_3$ is HIGH.

Timing Diagrams (continued)

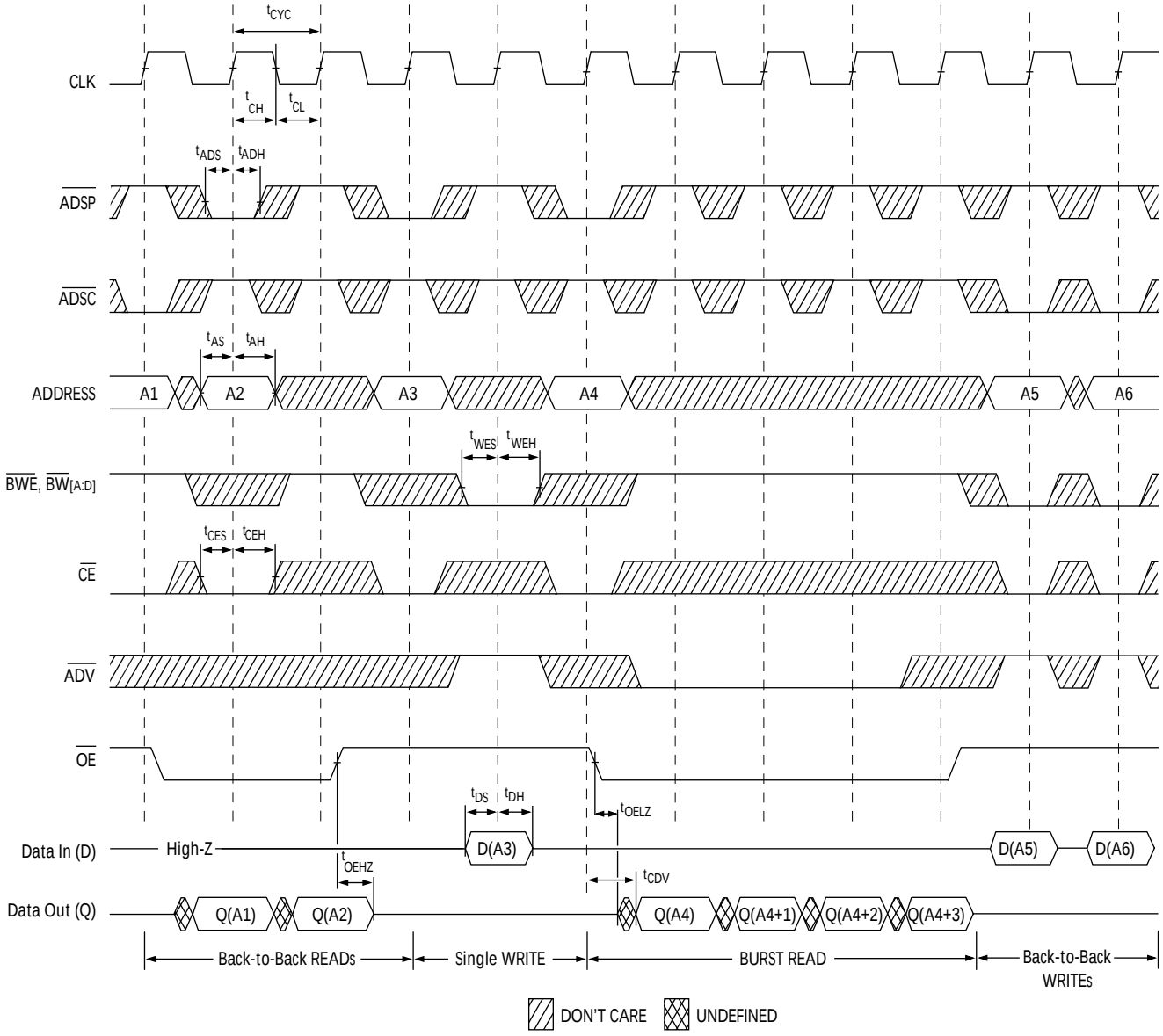
Figure 4. Write Cycle Timing [18, 19]



Notes
18. Full width write can be initiated by either $\overline{GW}$ LOW; or by $\overline{GW}$ HIGH, $\overline{BWE}$ LOW and $\overline{BW}$[A:D] LOW.
19. The data bus (Q) remains in High Z following a Write cycle unless an $\overline{ADSP}$, $\overline{ADSC}$, or $\overline{ADV}$ cycle is performed.

Timing Diagrams (continued)

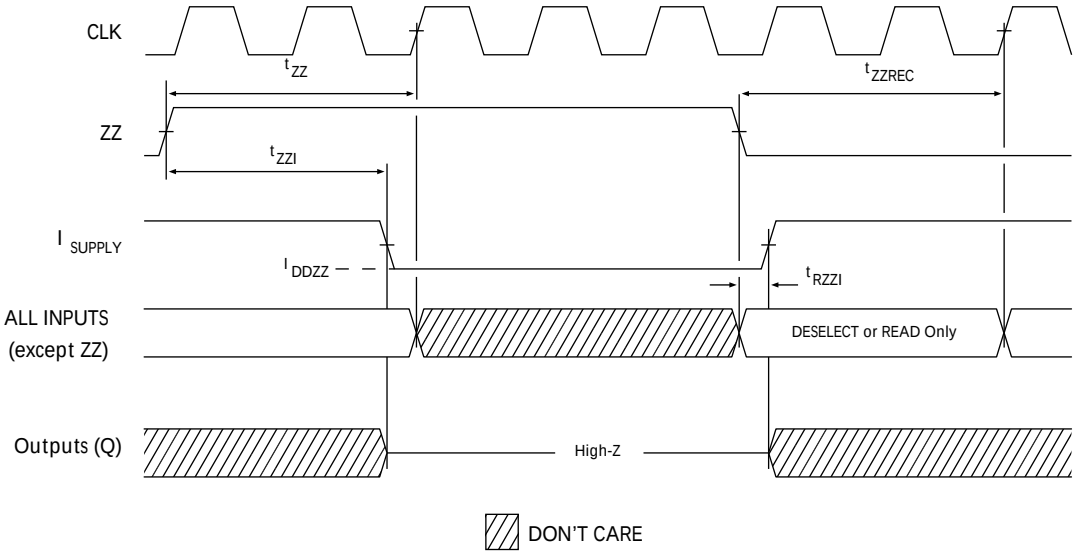
Figure 5. Read/Write Timing [20, 21, 22]



Notes
20. On this diagram, when $\overline{CE}$ is LOW, $\overline{CE}_1$ is LOW, CE_2 is HIGH and $\overline{CE}_3$ is LOW. When $\overline{CE}$ is HIGH, $\overline{CE}_1$ is HIGH or CE_2 is LOW or $\overline{CE}_3$ is HIGH.
21. The data bus (Q) remains in High Z following a Write cycle unless an ADSP, ADSC, or ADV cycle is performed.
22. $\overline{GW}$ is HIGH.

Timing Diagrams (continued)

Figure 6. ZZ Mode Timing [23, 24]



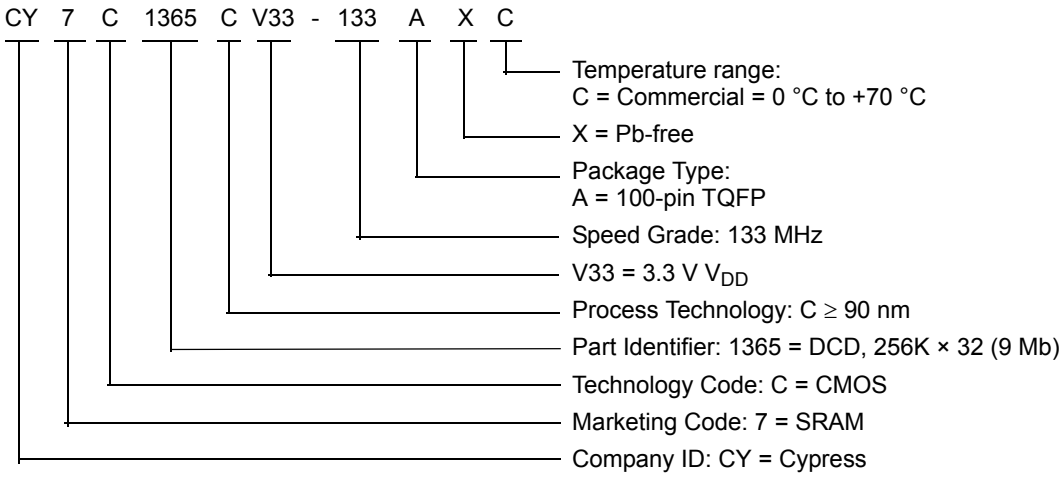
Notes
23. Device must be deselected when entering ZZ mode. See Cycle Descriptions table for all possible signal conditions to deselect the device.
24. DQs are in High Z when exiting ZZ sleep mode.

Ordering Information

Not all of the speed, package and temperature ranges are available. Please contact your local sales representative or visit www.cypress.com for actual products offered.

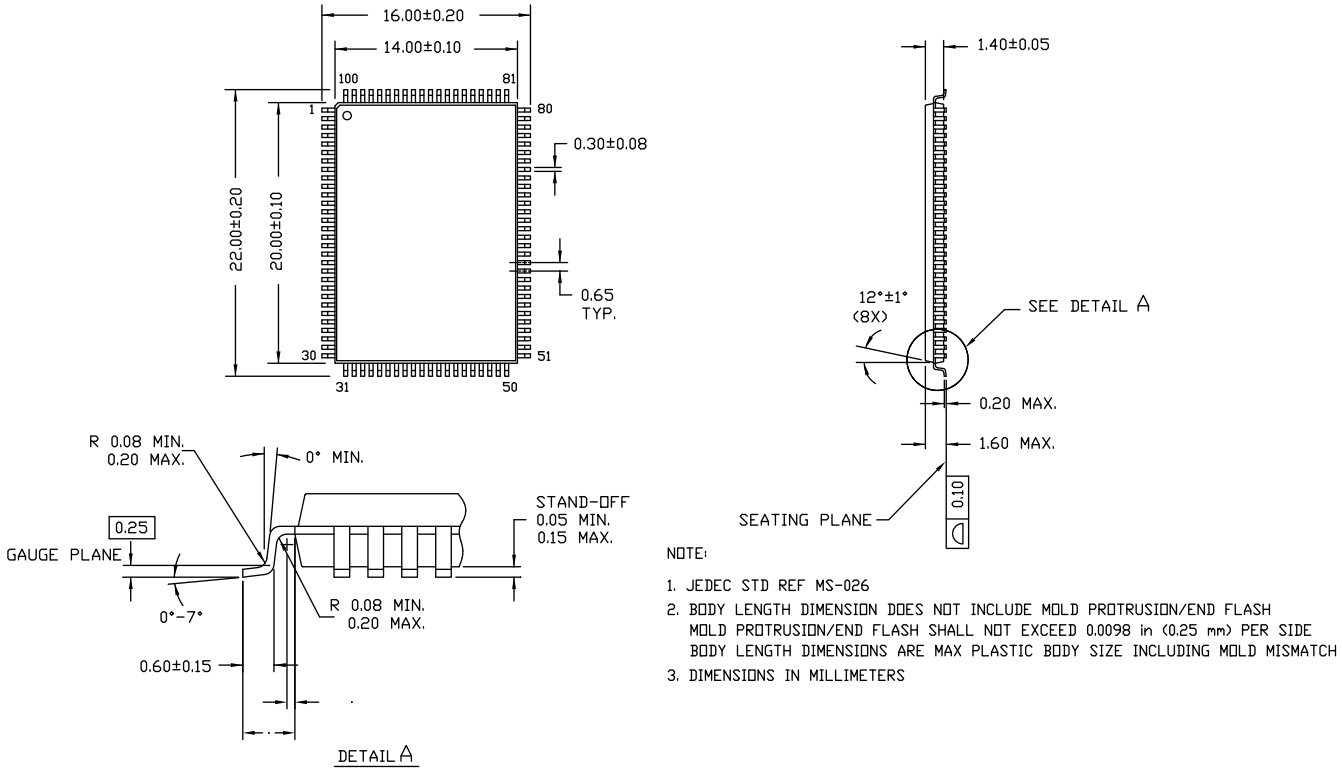
Speed (MHz)	Ordering Code	Package Diagram	Package Type	Operating Range
133	CY7C1365CV33-133AXC	51-85050	100-pin TQFP (14 × 20 × 1.4 mm) Pb-free (3 Chip Enable)	Commercial

Ordering Code Definitions



Package Diagram

Figure 7. 100-pin TQFP (14 × 20 × 1.4 mm) A100RA Package Outline, 51-85050



NOTE:

1. JEDEC STD REF MS-026
2. BODY LENGTH DIMENSION DOES NOT INCLUDE MOLD PROTRUSION/END FLASH MOLD PROTRUSION/END FLASH SHALL NOT EXCEED 0.0098 in (0.25 mm) PER SIDE BODY LENGTH DIMENSIONS ARE MAX PLASTIC BODY SIZE INCLUDING MOLD MISMATCH
3. DIMENSIONS IN MILLIMETERS

51-85050 *E

Acronyms

Acronym	Description
$\overline{CE}$	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
EIA	Electronic Industries Alliance
I/O	Input/Output
JEDEC	Joint Electron Devices Engineering Council
$\overline{OE}$	Output Enable
SRAM	Static Random Access Memory
TQFP	Thin Quad Flat Pack
TTL	Transistor-Transistor Logic

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microampere
mA	milliampere
mm	millimeter
ms	millisecond
mV	millivolt
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY7C1365CV33, 9-Mbit (256K × 32) Flow-Through Sync SRAM Document Number: 001-74473				
Rev.	**ECN No.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	3459992	01/09/2012	PRIT	New data sheet.
*A	3608159	05/04/2012	PRIT	Changed status from Preliminary to Final. Updated Operating Range (Removed Industrial Temperature Range).
*B	3794817	10/26/2012	PRIT	No technical updates. Completing Sunset Review.
*C	4573182	11/18/2014	PRIT	Updated Functional Description: Added “For a complete list of related documentation, click here.” at the end. Updated Package Diagram: spec 51-85050 – Changed revision from *D to *E.
*D	5069042	12/31/2015	PRIT	Updated to new template. Completing Sunset Review.
*E	5309766	06/15/2016	PRIT	Updated Truth Table. Updated to new template.

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