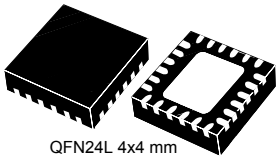
STUSB1600

Datasheet

Standalone USB Type-C™ controller with high voltage protections



QFN24L 4x4 mm

Features

- Type-C attach and cable orientation detection
- Power role support: source / sink / DRP
- Configurable start-up profiles
- Integrated power switch for V_{CONN} supply:
  - Programmable current limit up to 600 mA
  - Overcurrent, overvoltage and thermal protections
  - Undervoltage lockout
- I^2C interface and interrupt (optional connection to MCU)
- Integrated V_{BUS} voltage monitoring
- Integrated V_{BUS} and V_{CONN} discharge path
- Short-to-VBUS protection on CC pins (22 V) and VBUS pins (28 V)
- Dead-battery mode support
- Accessory mode support
- High and/or low voltage power supply:
  - V_{SYS} = [3.0 V; 5.5 V]
  - V_{DD} = [4.1 V; 22 V]
- ESD: 4 kV HBM - 1.5 kV CDM
- Temperature range: -40 °C up to 105 °C
- Certification test ID: 1000100

Product status link
STUSB1600

Device summary	
Order code	STUSB1600AQTR
Description	Standalone USB Type-C™ controller with high voltage protections
Package	QFN24 EP 4x4 mm
Marking	1600A

Applications

- Smart plugs, wall adapters, chargers
- Power hubs and docking stations
- Smartphones and tablets
- Gaming and PNDs
- Displays
- Wearable and Internet of Things (IoT)
- Cameras, camcorders, MP3 players
- Any Type-C source or sink device

Description

The STUSB1600 is an IC controller, fully compliant with the USB Type-C cable and connector specification (rev. 1.2), which addresses 5 V USB Type-C port management both on the host and/or device side. It is designed for a broad range of applications and can handle the following USB Type-C functions: attach detection, plug orientation detection, host to device connection, VCONN support, and V_{BUS} configuration. Thanks to its 20 V technology, it implements high voltage protection features against short-circuits to V_{BUS} up to 28 V. The device supports dead battery mode and is fully customizable thanks to an integrated non-volatile memory.

1 Functional description

The STUSB1600 is a USB Type-C controller IC. It is designed to interface with the Type-C receptacle both on host and/or device sides. It is used to establish and manage the source-to-sink connection between two USB Type-C host and device ports.

The STUSB1600 major role is to:

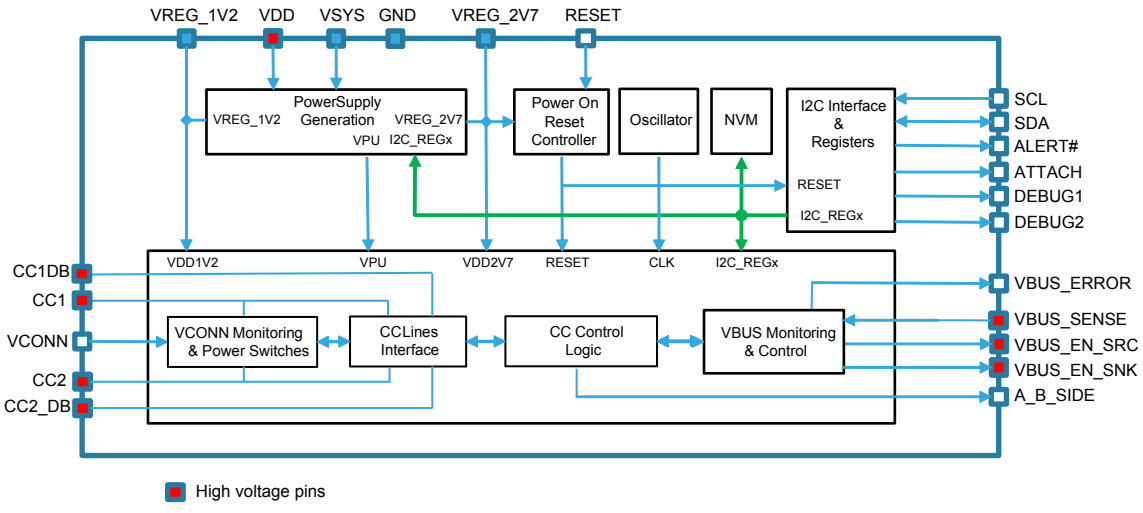
1. Detect the connection between two USB Type-C ports (attach detection)
2. Establish a valid source-to-sink connection
3. Determine the attached device mode: source, sink or accessory
4. Resolve cable orientation and twist connections to establish USB data routing (MUX control)
5. Configure and monitor V_{BUS} power path
6. Manage V_{BUS} power capability: USB Default, Type-C medium or Type-C high current mode
7. Configure V_{CONN} when required

The STUSB1600 also provides:

1. Low power standby mode
2. Dead-battery mode
3. I^2C interface and interrupt (optional connection to MCU)
4. Start-up configuration customization: static through NVM or/and dynamic through I^2C
5. High voltage protection
6. Accessory modes detection

1.1 Block overview

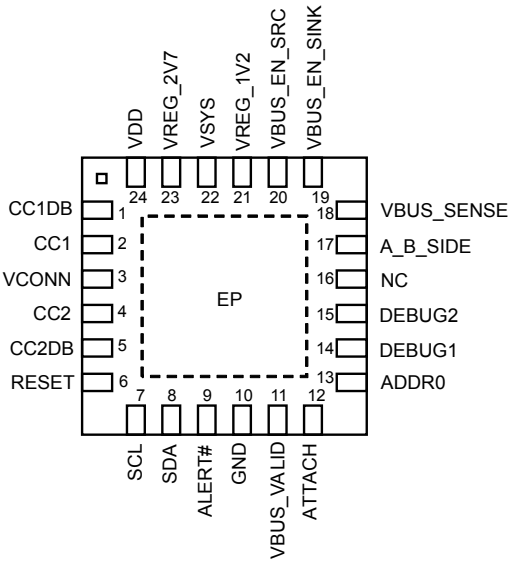
Figure 1. Functional block diagram



2 Inputs / outputs

2.1 Pinout

Figure 2. **STUSB1600 pin connections**



2.2 Pin list

Table 1. Pin functions list

Pin	Name	Type	Description	Typical connection
1	CC1DB	HV AIO	Dead-battery enable on CC1 pin	CC1 pin if used or ground
2	CC1	HV AIO	Type-C configuration channel 1	Type-C receptacle A5
3	VCONN	PWR	Power input for active plug	5 V power source
4	CC2	HV AIO	Type-C Configuration Channel 2	Type-C receptacle B5
5	CC2DB	HV AIO	Dead-battery enable on CC2 pin	CC2 pin if used or ground
6	RESET	DI	Reset input (active high)	
7	SCL	DI	I^2C clock input	To I²C master, ext. pull-up
8	SDA	DI/OD	I^2C data input/output – active low open-drain	To I²C master, ext. pull-up
9	ALERT#	OD	I^2C interrupt – active low open-drain	To I²C master, ext. pull-up
10	GND	GND	Ground	Ground
11	VBUS_VALID	OD	V_{BUS} detection, active low open-drain	To MCU if any, ext. pull-up
12	ATTACH	OD	Attachment detection, active low open-drain	To MCU if any, ext. pull-up
13	ADDR0	DI	I²C device address setting (see Section 4 I²C interface)	Static
14	DEBUG1	OD	Debug accessory device detection in sink power role, active low open-drain	To MCU if any, ext. pull-up
15	DEBUG2	OD	Debug accessory device detection in source power role, active low open-drain	To MCU if any, ext. pull-up
16	NC	-	-	Floating
17	A_B_SIDE	OD	Cable orientation, active low open-drain	USB SuperSpeed mux select – Ext. pull-up
18	VBUS_SENSE	HV AI	V_{BUS} voltage monitoring and discharge path	From V_{BUS}
19	VBUS_EN_SNK	HV OD	V_{BUS} sink power path enable, active low open-drain	To switch or power system, ext. pull-up
20	VBUS_EN_SRC	HV OD	V_{BUS} source power path enable, active low open-drain	To switch or power system, ext. pull-up
21	VREG_1V2	PWR	1.2 V internal regulator output	1 µF typ. decoupling capacitor
22	VSYS	PWR	Power supply from system	From power system, connect to ground if not used
23	VREG_2V7	PWR	2.7 V internal regulator output	1 µF typ. decoupling capacitor
24	VDD	HV PWR	Power supply from USB power line	From V_{BUS}
	EP	GND	Exposed pad is connected to ground	To ground

Table 2. **Legend**

Type	Description
D	Digital
A	Analog
O	Output pad
I	Input pad
IO	Bidirectional pad
OD	Open-drain output
PD	Pull-down
PU	Pull-up
HV	HIGH VOLTAGE
PWR	Power
GND	Ground

2.3 Pin description

2.3.1 CC1 / CC2

CC1 and CC2 are the configuration channel pins used for the connection and attachment detection, plug orientation determination and system configuration management across USB Type-C cable.

2.3.2 CC1DB / CC2DB

CC1DB and CC2DB are used for dead-battery mode when the STUSB1600 is configured in sink power role or dual power role. This mode is enabled by connecting CC1DB and CC2DB respectively to CC1 and CC2. Thanks to this connection, the pull-down terminations on the CC pins are present by default even if the device is not supplied (see Section 3.5 Dead-battery mode).

Note: CC1DB and CC2DB must be connected to ground when the STUSB1600 is configured in source power role or when the dead-battery mode is not supported.

2.3.3 VCONN

This power input is connected to a power source that can be a 5 V power supply, or a lithium battery. It is used to provide power supply to the local plug. It is internally connected to power switches that are protected against short-circuit and overvoltage. This does not require any protection on the input side. When a valid source-to-sink connection is determined and V_{CONN} power switches are enabled, V_{CONN} is provided by the source to the unused CC pin (see Section 3.3 VCONN supply).

2.3.4 RESET

Active high reset.

2.3.5 I²C interface pins

Table 3. I²C interface pin list

Name	Description
SCL	I²C clock, need external pull-up
SDA	I²C data, need external pull-up
ALERT#	I²C interrupt, need external pull-up
ADDR0	I²C device address bit (see Section 4 I²C interface)

2.3.6 GND

Ground.

2.3.7 VBUS_VALID

This pin is asserted during attachment when V_{BUS} is detected on VBUS_SENSE pin and V_{BUS} voltage is within the valid operating range. The V_{BUS} valid state is also advertised in a dedicated I^2C register bit (see Section 5.1 Register description).

2.3.8 ATTACH

This pin is asserted when a valid source-to-sink connection is established. It is also asserted when a connection to an accessory device is detected. The attachment state is also advertised in a dedicated I^2C register bit (see Section 5.1 Register description).

2.3.9 DEBUG pins

These pins are asserted when a debug accessory device is detected according to the running power role.

Table 4. Debug pin list

Name	Description
DEBUG1	Asserted when Type-C FSM is in DebugAccessory.SNK state in sink power role
DEBUG2	Asserted when Type-C FSM is in UnorientedDebugAccessory. SRC or OrientedDebugAccessory.SRC states in source power role

2.3.10 A_B_SIDE

This output pin provides cable orientation. It is used to establish USB SuperSpeed signal routing. The cable orientation is also advertised in a dedicated I^2C register bit. (see Section 5.1 Register description). This signal is not required in case of USB 2.0 support.

Table 5. USB data MUX select

Value	CC pin position
HiZ	CC1 pin is attached to CC line
0	CC2 pin is attached to CC line

2.3.11 VBUS_SENSE

This input pin is used to sense V_{BUS} presence, monitor V_{BUS} voltage and discharge V_{BUS} on USB Type-C receptacle side.

2.3.12 VBUS_EN_SNK

In sink power role, this pin allows the incoming V_{BUS} power to be enabled when the connection to a source is established and V_{BUS} is in the valid operating range. The open-drain output allows a PMOS transistor to be driven directly. The logic value of the pin is also advertised in a dedicated I^2C register bit (see Section 5.1 Register description).

2.3.13 VBUS_EN_SRC

In source power role, this pin allows the outgoing V_{BUS} power to be enabled when the connection to a sink is established and V_{BUS} is in the valid operating range. The open-drain output allows a PMOS transistor to be driven directly. The logic value of the pin is also advertised in a dedicated I^2C register bit (see Section 5.1 Register description).

2.3.14 VREG_1V2

This pin is used only for external decoupling of 1.2 V internal regulator. The recommended decoupling capacitor: 1 µF typ. (0.5 µF min.; 10 µF max.).

2.3.15 VSYS

This is the low power supply from the system, if any. It can be connected directly to a single cell lithium battery or to the system power supply delivering 3.3 V or 5 V. It is recommended to connect the pin to ground when it is not used.

2.3.16 VREG_2V7

This pin is used only for external decoupling of 2.7 V internal regulator. The recommended decoupling capacitor: 1 µF typ. (0.5 µF min.; 10 µF max.).

2.3.17 VDD

This is the main power supply for applications powered by V_{BUS}.

In source power role, this pin can be used to sense the voltage level of the main power supply providing V_{BUS}. It allows UVLO and OVLO thresholds to be considered independently on VDD pin as additional conditions to enable the V_{BUS} power path through VBUS_EN_SRC pin (see Section 3.2.3 VBUS power path assertion). When UVLO threshold detection is enabled, the VDD pin must be connected to the main power supply to establish the connection and to assert the V_{BUS} power path.

3 Features description

3.1 CC interface

The STUSB1600 controls the connection to the configuration channel (CC) pins, CC1 and CC2, through two main blocks, the CC lines interface block and the CC control logic block.

The CC line interface block is used to:

- Configure the termination mode on the CC pins relative to the power mode supported, i.e. pull-up for source power role and pull-down for sink power role
- Monitor the CC pin voltage values relative to the attachment detection thresholds
- Configure V_{CONN} on the unconnected CC pin when required
- Protect the CC pins against overvoltage

The CC control logic block is used to:

- Execute the Type-C FSM relative to the Type-C power mode supported
- Determine the electrical state for each CC pin relative to the detected thresholds
- Evaluate the conditions relative to the CC pin states and V_{BUS} voltage value to transition from one state to another in the Type-C FSM
- Detect and establish a valid source-to-sink connection
- Determine the attached device mode: source, sink or accessory
- Determine cable orientation to allow external routing of the USB data
- Manage V_{BUS} power capability: USB default, Type-C medium or Type-C high current mode
- Handle hardware faults

The CC control logic block implements the Type-C FSMs corresponding to the following Type-C power modes:

- Source power role with accessory support
- Sink power role with accessory support
- Sink power role without accessory support
- Dual power role with accessory support
- Dual power role with accessory and Try.SRC support
- Dual power role with accessory and Try.SNK support

The default Type-C power mode is selected through NVM programming (see Section 6 Start-up configuration) and can be changed by software during operation through I^2C interface (see Section 5.1 Register description).

3.2 V_{BUS} power path control

3.2.1 V_{BUS} monitoring

The V_{BUS} monitoring block supervises (from the VBUS_SENSE pin) the V_{BUS} voltage on the USB Type-C receptacle side.

It is used to check that V_{BUS} is within a valid voltage range:

- To establish a valid source-to-sink connection according to USB Type-C standard specifications
- To enable safely the V_{BUS} power path through VBUS_EN_SRC pin or VBUS_EN_SNK pin depending on the power role

It allows detection of unexpected V_{BUS} voltage conditions such as: undervoltage or overvoltage relative to the valid V_{BUS} voltage range. When such conditions occurs, the STUSB1600 behaves as follows:

- At attachment, it prevents the source-to-sink connection and the V_{BUS} power path assertion

- After attachment, it deactivates the source-to-sink connection and disables the V_{BUS} power path. In source power role, the device goes into error recovery state. In sink power role the device goes into unattached state

The valid V_{BUS} voltage range is defined from V_{BUS} nominal voltage by a high threshold voltage and a low threshold voltage whose nominal values are respectively V_{BUS}+5% and V_{BUS}-5%. The nominal threshold limits can be shifted by a fraction of V_{BUS} from +1% to +15% for the high threshold voltage and from -1% to -15% for the low threshold voltage. It means the threshold limits can vary from V_{BUS}+5% to V_{BUS}+20% for the high limit and from V_{BUS}-5% to V_{BUS}-20% for the low limit.

The threshold limits are preset by default in the NVM with different shift coefficients depending on whether the device operates in source power role or sink power role (see Section 8.3 Electrical and timing characteristics). The threshold limits can be changed independently through NVM programming (see Section 6 Start-up configuration) and also by software during attachment through I^2C interface (see Section 5.1 Section 4.4: Register description).

3.2.2 V_{BUS} discharge

The monitoring block handles also the internal V_{BUS} discharge path connected to the VBUS_SENSE pin. The discharge path is activated at detachment, or when the device goes into the error recovery state whatever the power role (see Section 3.7 Hardware fault management).

The V_{BUS} discharge path is enabled by default in the NVM and can be disabled through NVM programming only (see Section 6 Start-up configuration). The discharge time duration is also preset by default in the NVM (see Section 8.3 Electrical and timing characteristics). The discharge time duration can be modified through NVM programming (see Section 6 Start-up configuration) and also by software through the I^2C interface (see Section 5.1 Register description).

3.2.3 V_{BUS} power path assertion

The STUSB1600 can control the assertion of the V_{BUS} power path on USB Type-C port, directly or indirectly, through VBUS_EN_SRC pin and VBUS_EN_SNK pins according to the system power role.

The following tables summarize the configurations of the STUSB1600 and the operation conditions that determine the electrical value of VBUS_EN_SRC pin and VBUS_EN_SNK pins during the system operation.

Table 6. Conditions for V_{BUS} power path assertion in source power role

Pin	Electrical value	Operation conditions			Comment
		Type-C attached state	VDD pin monitoring	VBUS_SENSE pin monitoring	
VBUS_EN_SRC	0	Attached.SRC or UnorientedDebug Accessory.SRC or OrientedDebug Accessory.SRC	$V_{DD} > V_{DDUVLO}$ if UVLO threshold detection enabled and/or $V_{DD} < V_{DDOVLO}$ if OVLO threshold detection enabled	$V_{BUS} < V_{MONUSBH}$ and $V_{BUS} > V_{MONUSBL}$ if V_{BUS}voltage range detection enabled or $V_{BUS} > V_{THUSB}$ if V_{BUS} voltage range detection disabled	The signal is asserted only if all the valid operation conditions are met
	HiZ	Any other state	$V_{DD} < V_{DDUVLO}$ if UVLO threshold detection enabled and/or $V_{DD} > V_{DDOVLO}$ if OVLO threshold detection enabled	$V_{BUS} > V_{MONUSBH}$ or $V_{BUS} < V_{MONUSBL}$ if V_{BUS} voltage range detection enabled or $V_{BUS} < V_{THUSB}$ if V_{BUS} voltage range detection disabled	The signal is de-asserted when at least one non-valid operation condition is met

As specified in the USB Type-C standard specification, the attached state "Attached.SRC" is reached only if the voltage on V_{BUS} receptacle side is at vSafe0V condition when a connection is detected.

Table 7. Conditions for V_{BUS} power path assertion in sink power role

Pin	Electrical value	Operation conditions			Comment
		Type-C attached state	VDD pin monitoring	VBUS_SENSE pin monitoring	
VBUS_EN_SNK	0	Attached.SNK or DebugAccessory.SNK	Not applicable	$V_{BUS} < V_{MONUSBH}$ and $V_{BUS} > V_{MONUSBL}$ if V_{BUS} voltage range detection enabled or $V_{BUS} > V_{THUSB}$ if V_{BUS} voltage range detection disabled	The signal is asserted only if all the valid operation conditions are met
	HiZ	Any other state	Not applicable	$V_{BUS} > V_{MONUSBH}$ or $V_{BUS} < V_{MONUSBL}$ if V_{BUS} voltage range detection enabled or $V_{BUS} < V_{THUSB}$ if V_{BUS} voltage range detection disabled	The signal is de-asserted when at least one non-valid operation condition is met

"Type-C attached state" refers to the Type-C FSM states as defined in the USB Type-C standard specification and as described in I^2C register CC_OPERATION_STATUS (see Section 5.1 Register description).

"VDD pin monitoring" is valid in source power role only. The activation of the UVLO and OVLO threshold detections can be done through NVM programming (see Section 6 Start-up configuration) and also by software through I^2C interface (see Section 5.1 Register description). When UVLO and/or OVLO threshold detection is activated, VBUS_EN_SRC pin is asserted only if the device is attached and the valid threshold conditions on VDD are met. Once VBUS_EN_SRC pin is asserted, the V_{BUS} monitoring is done on VBUS_SENSE pin instead of VDD pin.

"VBUS_SENSE pin monitoring" relies by default on the valid V_{BUS} voltage range defined by a high limit $V_{MONUSBH}$ and a low limit $V_{MONUSBL}$. The voltage range conditions can be disabled to consider UVLO threshold detection instead. The monitoring conditions of V_{BUS} voltage can be changed through NVM programming (see Section 6 Start-up configuration) and also by software through I^2C interface (see Section 5.1 Register description).

See Section 8.3 Electrical and timing characteristics for the threshold voltage description and value on VDD and VBUS_SENSE pins.

3.3 V_{CONN} supply

3.3.1 V_{CONN} input voltage

V_{CONN} is a regulated supply used to power circuits in the plug of USB3.1 full-featured cables and other accessories. V_{CONN} nominal operating voltage is 5.0 V ± 5%.

3.3.2 V_{CONN} application conditions

The V_{CONN} pin of the STUSB1600 is connected to each CC pin (CC1 and CC2) across independent power switches.

The STUSB1600 applies V_{CONN} only to the CC pin not connected to the CC wire when all below conditions are met:

- The device is configured in source power role or dual power role
- V_{CONN} power switches are enabled
- A valid connection to a sink is achieved
- Ra presence is detected on the unwired CC pin
- A valid power source is applied on V_{CONN} pin with respect to a predefined UVLO threshold

The STUSB1600 does not provide V_{CONN} when it works in sink power role.

3.3.3 V_{CONN} monitoring

The V_{CONN} monitoring block detects if V_{CONN} power supply is available on the VCONN pin. It is used to check that V_{CONN} voltage is above a predefined undervoltage lockout (UVLO) threshold to allow V_{CONN} power switches to be enabled.

The default value of the UVLO threshold is 4.65 V typical for powered cables operating at 5 V. It can be changed by software to 2.65 V typical to support V_{CONN}-powered accessories that are operating down to 2.7 V (see Section 5.1 Register description).

3.3.4 V_{CONN} discharge

The behavior of Type-C FSMs is extended with an internal V_{CONN} discharge path capability on CC pins in source power mode only. The discharge path is activated during 250 ms from sink detachment detection. This feature is disabled by default and can be activated through NVM programming (see Section 6 Start-up configuration) and also by software through I^2C interface (see Section 5.1 Register description).

3.3.5 V_{CONN} control and status

The supplying conditions of V_{CONN} across the STUSB1600 are managed through the I^2C interface. Different I^2C registers and bits are used specifically for this purpose (see Section 5.1 Register description).

3.3.6 VCONN power switches

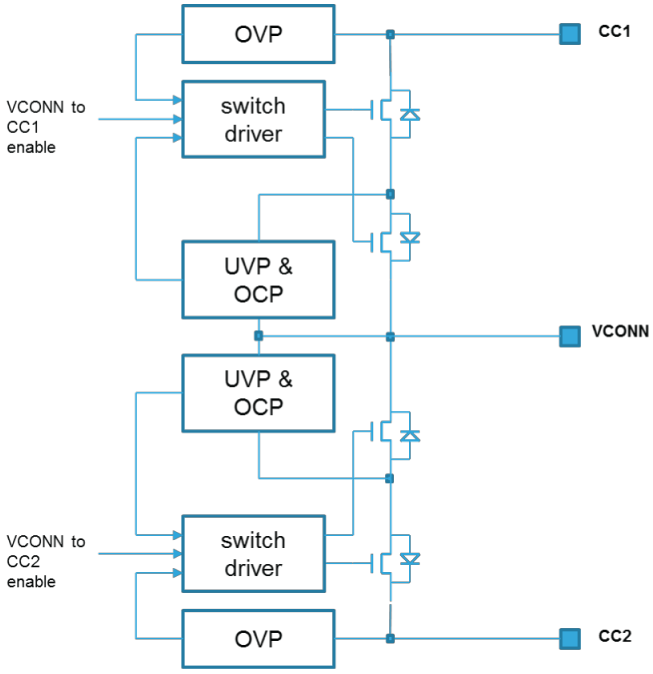
Features

The STUSB1600 integrates two current limited high-side power switches with protections that tolerate high voltage up to 22 V on the CC pins.

Each V_{CONN} power switch presents the following features:

- Soft-start to limit inrush current
- Constant current mode overcurrent protection
- Adjustable current limit
- Thermal protection
- Undervoltage and overvoltage protection
- Reverse current and reverse voltage protections

Figure 3. V_{CONN} to CC1 and CC2 power switch protections



Current limit programming

The current limit can be set within the range 100 mA to 600 mA by step of 50 mA. The default current limit is programmed through NVM programming (see Section 6 Start-up configuration) and can be changed by software through I²C interface (see Section 5.1 Register description). At power-on or after a reset, the current limit takes the default value preset in the NVM.

Fault management

The table below summarizes the different fault conditions that could occur during the operation of the switch and the associated responses. An I²C alert is generated when a fault condition happens (see Section 5.1 Register description).

Table 8. Fault management conditions

Fault types	Fault conditions	Expected actions
Short-circuit	CC output pin shorted to ground via very low resistive path causing rapid current surge	Power switch limits the current and reduces the output voltage. I²C alert is asserted immediately thanks to VCONN_SW_OCP_FAULT bits
Overcurrent	CC output pin connected to a load that sinks current above programmed limit	Power switch limits the current and reduces the output voltage. I²C alert is asserted immediately thanks to VCONN_SW_OCP_FAULT bits
Overheating	Junction temperature exceeding 145 °C due to any reason	Power switch is disabled immediately until the temperature falls below 145 ° minus hysteresis of 15 °C. I²C alert is asserted immediately thanks to THERMAL_FAULT bit. The STUSB1600 goes into transient error recovery state
Undervoltage	V_{CONN} input voltage drops below UVLO threshold minus hysteresis	Power switch is disabled immediately until the input voltage rises above the UVLO threshold. I²C alert is asserted immediately thanks to VCONN_PRESENCE bit

Fault types	Fault conditions	Expected actions
Overvoltage	CC output pin voltage exceeds maximum operating limit of 6.0 V	Power switch is opened immediately until the voltage falls below the voltage limit. I^2C alert is asserted immediately thanks to VCONN_SW_OVP_FAULT bits
Reverse current	CC output pin voltage exceeds V_{CONN} input voltage when the power switch is turned off	The reverse biased body diode of the back-to-back MOS switches is naturally disabled preventing current to flow from the CC output pin to the input
Reverse voltage	CC output pin voltage exceeds V_{CONN} input voltage of more than 0.35 V for 5 V when the power switch is turned on	Power switch is opened immediately until the voltage difference falls below the voltage limit. I^2C alert is asserted immediately thanks to VCONN_SW_RVP_FAULT bits

3.4 Low power standby mode

The STUSB1600 proposes a standby mode to reduce the device power consumption when no device is connected to the USB Type-C port. It is disabled by default and can be activated through NVM programming (see Section 6 Start-up configuration).

When activated, the STUSB1600 enters standby mode at power-up, or after a reset, after a reset or after a disconnection. In this mode, the CC interface and the voltages monitoring blocks are turned off. Only a monitoring circuitry is maintained active on the CC pins to detect a connection. When the connection is detected, all the internal circuits are turned on to allow normal operations.

The standby mode does not operate when the device is configured in sink power role with accessory support (see Section 6 Start-up configuration).

3.5 Dead-battery mode

The dead-battery mode allows systems powered by a battery to be supplied by V_{BUS} when the battery is discharged and to start the battery charging process. It is also used in systems that are powered through V_{BUS} only.

This mode is only supported in sink power role and dual power role configurations. It operates only if the CC1DB and CC2DB pins are connected respectively to the CC1 and CC2 pins. Thanks to these connections, the STUSB1600 presents a pull-down termination on its CC pins and advertises itself as a sink even if the device is not supplied.

When a source system connects to a USB Type-C port with the STUSB1600 configured in dead-battery mode, it can detect the pull-down termination, establish the source-to-sink connection, and provide the V_{BUS}. The STUSB1600 is then supplied thanks to the VDD pin connected to the V_{BUS} on the USB Type-C receptacle side. The STUSB1600 can finalize the source-to-sink connection and enable the power path on the V_{BUS} thanks to the VBUS_EN_SNK pin which allows the system to be powered.

3.6 High voltage protection

The STUSB1600 can be used safely in systems or connected to systems that handle high voltage on the V_{BUS} power path. The device integrates an internal circuitry on the CC pins that tolerates high voltages and ensures a protection up to 22 V in case of unexpected short-circuit with V_{BUS} or in case of connection to a device supplying high voltage on V_{BUS}.

3.7 Hardware fault management

The STUSB1600 handles hardware fault conditions related to the device itself and to the V_{BUS} power path during the system operation.

When such conditions happens, the circuit goes into a transient error recovery state named ErrorRecovery in the Type-C FSM. The error recovery state is sufficient to force a detach event.

When entering this state, the device de-asserts the V_{BUS} power path by disabling VBUS_EN_SRC pin and VBUS_EN_SNK pin, and it removes the terminations from the CC pins during few tens of milliseconds. Then it transits to the unattached state related to the configured power mode.

The STUSB1600 goes into error recovery state when at least one condition listed below is met:

- Whatever the power role:
  - If an overtemperature is detected, the "THERMAL_FAULT" bit set to 1b
- In source power role only:
  - If an internal pull-up voltage on CC pins is below UVLO threshold (VPU_VALID bit set to 0b)
  - If an overvoltage is detected on the CC pins (VPU_OVP_FAULT bit set to 1b)
  - If V_{BUS} voltage is out of the valid voltage range during attachment (VBUS_VALID bit set to 0b)
  - If an undervoltage is detected on VDD pin during attachment when UVLO detection is enabled (VDD_UVLO_DISABLE bit set to 0b)
  - If an overvoltage is detected on VDD pin during attachment when OVLO detection is enabled (VDD_OVLO_DISABLE bit set to 0b)

The I^2C register bits above-mentioned give either the state of the hardware fault when it occurs, or the setting conditions to detect the hardware fault (see Section 5.1 Register description).

3.8 Accessory mode detection

The STUSB1600 supports the detection of audio accessory mode and debug accessory mode as defined in USB Type-C standard specification with the following Type-C power modes (see Section 6 Start-up configuration):

- Source power role with accessory support
- Sink power role with accessory support
- Dual power role with accessory support
- Dual power role with accessory and Try.SRC support
- Dual power role with accessory and Try.SNK support

3.8.1 Audio accessory mode detection

The STUSB1600 detects an audio accessory device when both CC1 and CC2 pins are pulled down to ground by Ra resistor from the connected device. The audio accessory detection is advertised through CC_ATTACHED_MODE bits of I^2C register CC_CONNECTION_STATUS (see Section 5.1 Register description).

3.8.2 Debug accessory mode detection

The STUSB1600 detects a connection to a debug and test system (DTS) when it operates either in sink power role or in source power role. The debug accessory detection is advertised by DEBUG1 and DEBUG2 pins as well as through CC_ATTACHED_MODE bits of I^2C register CC_CONNECTION_STATUS (see Section 5.1 Register description).

In sink power role, a debug accessory device is detected when both CC1 and CC2 pins are pulled up by Rp resistor from the connected device. The voltage levels on CC1 and CC2 pins give the orientation and the current capability as described in the table below. DEBUG1 pin is asserted to advertise the DTS detection and A_B_SIDE pin indicates the orientation of the connection. The current capability of the DTS is given through SINK_POWER_STATE bits of I^2C register CC_OPERATION_STATUS (see Section 5.1 Register description).

Table 9. Orientation and current capability detection in sink power role

#	CC1 (CC2)	CC2 (CC1)	Charging current configuration	A_B_SIDE pin CC1/CC2 (CC2/CC1)	Current capability state SINK_POWER_STATE bit values
1	Rp 3A	Rp 1.5 A	Default	HiZ (0)	PowerDefault.SNK (source supplies default USB current)
2	Rp 1.5 A	Rp default	1.5 A	HiZ (0)	Power1.5.SNK (source supplies 1.5 A USB Type-C current)
3	Rp 3 A	Rp default	3.0 A	HiZ (0)	Power3.0.SNK (source supplies 3.0 A USB Type-C current)
4	Rp def/1.5 A/3 A	Rp def/1.5 A/3 A	Default	HiZ (HiZ)	PowerDefault.SNK (source supplies default USB current)

In source power role, a debug accessory device is detected when both CC1 and CC2 pins are pulled down to ground by Rd resistor from the connected device. The orientation detection is performed in two steps as described in the table below. DEBUG2 pin is asserted to advertise the DTS detection and the A_B_SIDE pin indicates the orientation of the connection. The orientation detection is advertised through TYPEC_FSM_STATE bits of I^2C register CC_OPERATION_STATUS (see Section 5.1 Register description).

Table 10. Orientation detection in source power role

#	CC1 (CC2)	CC2 (CC1)	Detection process	A_B_SIDE pin CC1/CC2 (CC2/CC1)	Orientation detection state TYPEC_FSM_STATE bit value
1	Rd	Rd	1st step: debug accessory mode detected	HiZ (HiZ)	UnorientedDebugAccessory.SRC
2	Rd	≤Ra	2nd step: orientation detected (DTS presents a resistance to GND with a value ≤Ra on its CC2 pin)	HiZ (0)	OrientedDebugAccessory.SRC

4 I²C interface

4.1 Read and write operations

The I²C interface is used to configure, control and read the operation status of the device. It is compatible with the Philips I²C Bus® (version 2.1). The I²C is a slave serial interface based on two signals:

- SCL - serial clock line: input clock used to shift data
- SDA - serial data line: input/output bidirectional data transfers

A filter rejects the potential spikes on the bus data line to preserve data integrity.

The bidirectional data line supports transfers up to 400 kbit/s (fast mode). The data are shifted to and from the chip on the SDA line, MSB first.

The first bit must be high (START) followed by the 7-bit device address and the read/write control bit.

Two 7-bit device address are available for the STUSB1600 thanks to the external programming of DevADDR0 through ADDR0 pin setting, i.e. 0x28 or 0x29. It allows two STUSB1600 devices to be connected on the same I²C bus.

Table 11. Device address format

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
DevADDR6	DevADDR5	DevADDR4	DevADDR3	DevADDR2	DevADDR1	DevADDR0	R/W
0	1	0	1	0	0	ADDR0	0/1

Table 12. Register address format

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
RegADDR7	RegADDR6	RegADDR5	RegADDR4	RegADDR3	RegADDR2	RegADDR1	RegADDR0

Table 13. Register data format

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

Figure 4. Read operation

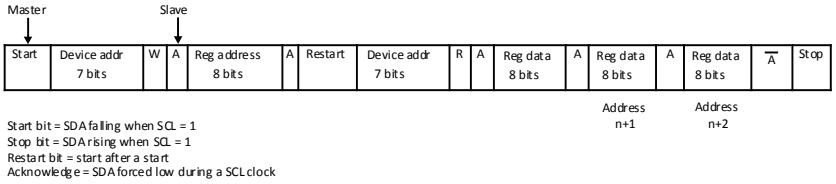
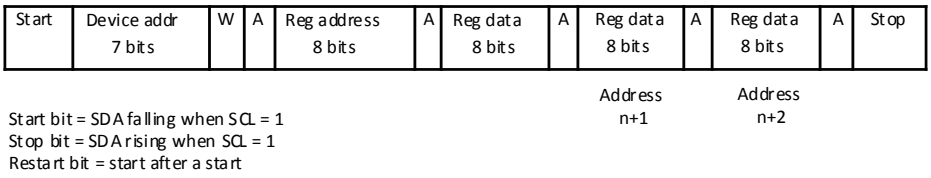


Figure 5. **Write operation**



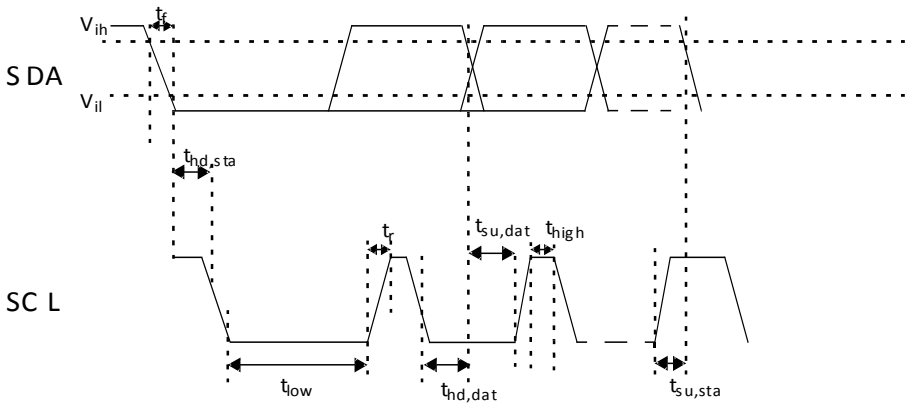
4.2 Timing specifications

The device uses a standard slave I²C channel at speed up to 400 kHz.

Table 14. **I²C timing parameters - V_{DD} = 5 V**

Symbol	Parameter	Min.	Typ.	Max.	Unit
F_{scl}	SCL clock frequency	0	-	400	kHz
$t_{hd,sta}$	Hold time (repeated) START condition	0.6	-	-	µs
t_{low}	LOW period of the SCL clock	1.3	-	-	µs
t_{high}	HIGH period of the SCL clock	0.6	-	-	µs
$t_{su,dat}$	Set-up time for repeated START condition	0.6	-	-	µs
$t_{hd,dat}$	Data hold time	0.04	-	0.9	µs
$t_{su,dat}$	Data set-up time	100	-	-	µs
t_r	Rise time of both SDA and SCL signals	20 + 0.1 C_b	-	300	ns
t_f	Fall time of both SDA and SCL signals	20 + 0.1 C_b	-	300	ns
$t_{su,sto}$	Set-up time for STOP condition	0.6	-	-	µs
t_{buf}	Bus free time between a STOP and START condition	1.3	-	-	µs
C_b	Capacitive load for each bus line	-	-	400	pF

Figure 6. I²C timing diagram



5 I²C register map

Table 15. **Register access legend**

Access code	Expanded name	Description
RO	Read only	Register can be read only
R/W	Read /write	Register can be read or written
RC	Read and clear	Register can be read and is cleared after read

Table 16. **STUSB1600 register map overview**

Address	Register name	Access	Description
00h to 0Ah	Reserved	RO	Do not use
0Bh	ALERT_STATUS	RC	Alert register linked to transition registers
0Ch	ALERT_STATUS_MASK_CTRL	R/W	Allows the interrupt mask on ALERT_STATUS register to be changed
0Dh	CC_CONNECTION_STATUS_TRANS	RC	Alerts about transition in CC_CONNECTION_STATUS register
0Eh	CC_CONNECTION_STATUS	RO	Gives status on CC connection
0Fh	MONITORING_STATUS_TRANS	RC	Alerts about transition in MONITORING_STATUS register
10h	MONITORING_STATUS	RO	Gives status on V_{BUS} and V_{CONN} voltage monitoring
11h	CC_OPERATION_STATUS	RO	Gives status on CC operation modes
12h	HW_FAULT_STATUS_TRANS	RC	Alerts about transition in HW_FAULT_STATUS register
13h	HW_FAULT_STATUS	RO	Gives status on hardware faults
14h to 17h	Reserved	RO	Do not use
18h	CC_CAPABILITY_CTRL	R/W	Allows the CC capabilities to be changed
19h to 1Dh	Reserved	RO	Do not use
1Eh	CC_VCONN_SWITCH_CTRL	R/W	Allows the current limit of V_{CONN} power switches to be changed
1Fh	Reserved	RO	Do not use
20h	VCONN_MONITORING_CTRL	R/W	Allows the monitoring conditions of V_{CONN} voltage to be changed
21h	Reserved	RO	Do not use
22h	VBUS_MONITORING_RANGE_CTRL	R/W	Allows the voltage range for V_{BUS} monitoring to be changed
23h	RESET_CTRL	R/W	Controls the device reset by software
24h	Reserved	RO	Do not use
25h	VBUS_DISCHARGE_TIME_CTRL	R/W	Allows the V_{BUS} discharge time to be changed

Address	Register name	Access	Description
26h	VBUS_DISCHARGE_STATUS	RO	Gives status on V_{BUS} discharge path activation
27h	VBUS_ENABLE_STATUS	RO	Gives status on V_{BUS} power path activation
28h	CC_POWER_MODE_CTRL	R/W	Allows the CC power mode to be changed
29h to 2Dh	Reserved	RO	Do not use
2Eh	VBUS_MONITORING_CTRL	R/W	Allows the monitoring conditions of V_{BUS} voltage to be changed
2Fh	Reserved	RO	Do not use

5.1 Register description

The reset column specified in the register descriptions below defines the default value of the registers at power-up or after a reset. The reset values with (NVM) index correspond to the user-defined parameters that can be customized by NVM re-programming if needed (see Section 6 Start-up configuration).

5.1.1 ALERT_STATUS

Address: 0Bh

Access: RC

Note: This register indicates an alert that has occurred.

Table 17. ALERT_STATUS register

Bit	Field name	Reset	Description
7	Reserved	0b	Do not use
6	CC_CONNECTION_STATUS_AL	0b	0b: cleared 1b: change occurred on CC_CONNECTION_STATUS_TRANS register
5	MONITORING_STATUS_AL	0b	0b: cleared 1b: change occurred on MONITORING_STATUS_TRANS register
4	HW_FAULT_STATUS_AL	0b	0b: cleared 1b: change occurred on HW_FAULT_STATUS_TRANS register
3:0	Reserved	0000b	Do not use

When a bit value change occurs on one of the mentioned transition registers, it automatically sets the corresponding alert bit in ALERT_STATUS register.

5.1.2 ALERT_STATUS_MASK_CTRL

Address: 0Ch

Access: R/W

Note: This register is used to mask event interrupt and prevent the assertion of the alert bit in the ALERT_STATUS register when the corresponding bit defined below is set to 1.

Table 18. **ALERT_STATUS_MASK_CTRL register**

Bit	Field Name	Reset	Description
7	Reserved	1b	Do not use
6	CC_CONNECTION_STATUS_AL_MASK	1b (NVM)	0b: interrupt unmasked 1b: interrupt masked
5	MONITORING_STATUS_AL_MASK	1b (NVM)	0b: interrupt unmasked 1b: interrupt masked
4	HW_FAULT_STATUS_AL_MASK	1b (NVM)	0b: interrupt unmasked 1b: interrupt masked
3:0	Reserved	1111b	Do not use

The condition to generate an active-low ALERT signal is:
[ALERT_STATUS bitwise AND (NOT ALERT_STATUS_MASK)] <> 0

5.1.3 CC_CONNECTION_STATUS_TRANS

Address: 0Dh
Access: RC

Note: This register indicates a bit value change has occurred in CC_CONNECTION_STATUS register.

Table 19. **CC_CONNECTION_STATUS_TRANS register**

Bit	Field name	Reset	Description
7:1	Reserved	0000000b	Do not use
0	CC_ATTACH_TRANS	0b	0b: cleared 1b: transition occurred on CC_ATTACH bit

5.1.4 CC_CONNECTION_STATUS

Address: 0Eh

Access: RO

Note: This register gives the connection state of the CC pins and on associated operating modes of the device.

Table 20. CC_CONNECTION_STATUS register

Bit	Field name	Reset	Description
7:5	CC_ATTACHED_MODE	000b	000b: no device attached 001b: sink attached 010b: source attached 011b: debug accessory attached 100b: audio accessory attached 101b: do not use 110b: do not use 111b: do not use
4	DEVICE_POWER_MODE	0b(NVM)	0b: operating in normal power mode 1b: operating in standby power mode
3	CC_POWER_ROLE	0b	0b: operating as a sink 1b: operating as a source
2	Reserved	0b	Do not use
1	CC_VCONN_SUPPLY	0b	0b: V_{CONN} is not supplied on CC pin 1b: V_{CONN} is supplied on CC pin
0	CC_ATTACH	0b	0b: not attached 1b: attached

The DEVICE_POWER_MODE bit indicates the power consumption mode of the device at start-up and during operation:

- In normal mode, all the internal circuits are turned on
- In standby mode the CC interface and the voltage monitoring blocks remain off until a connection is detected

The standby mode power is disabled by default and can be activated through NVM programming (see Section 6 Start-up configuration).

The CC_POWER_ROLE bit is relevant only when a connection is established and the device is attached.

5.1.5 MONITORING_STATUS_TRANS

Address: 0Fh

Access: RC

Note: This register indicates a bit value change has occurred in MONITORING_STATUS register.

Table 21. MONITORING_STATUS_TRANS register

Bit	Field name	Reset	Description
7:4	Reserved	0000b	Do not use
3	VBUS_VALID_TRANS	0b	0b: cleared 1b: transition occured on VBUS_VALID bit
2	VBUS_VSAFE0V_TRANS	0b	0b: cleared 1b: transition occured on VBUS_VSAFE0V bit
1	VBUS_PRESENCE_TRANS	0b	0b: cleared 1b: transition occured on VBUS_PRESENCE bit
0	VCONN_PRESENCE_TRANS	0b	0b: cleared 1b: transition occured on VCONN_PRESENCE bit

5.1.6 MONITORING_STATUS

Address: 10h

Access: RO

Note: This register gives the current status of V_{BUS} and V_{CONN} voltage monitoring done respectively on VBUS_SENSE pin and VCONN pin.

Table 22. MONITORING_STATUS register

Bit	Field name	Reset	Description
7:4	Reserved	0000b	Do not use
3	VBUS_VALID	0b	0b: V_{BUS} is outside valid V_{BUS} voltage range 1b: V_{BUS} is within valid V_{BUS} voltage range
2	VBUS_VSAFE0V	1b	0b: V_{BUS} is above V_{BUS} VSafe0V threshold 1b: V_{BUS} is below V_{BUS} VSafe0V threshold
1	VBUS_PRESENCE	0b	0b: V_{BUS} is below V_{BUS} UVLO threshold 1b: V_{BUS} is above V_{BUS} UVLO threshold
0	VCONN_PRESENCE	0b or 1b	0b: V_{CONN} is below V_{CONN} UVLO threshold 1b: V_{CONN} is above V_{CONN} UVLO threshold

The default value of valid V_{BUS} voltage range can be changed in VBUS_MONITORING_RANGE_CTRL register during the operation.

V_{BUS} vSafe0V threshold is defined in VBUS_MONITORING_CTRL register. It is used in source power role as a Type-C FSM condition to establish a valid device attachment.

V_{BUS} UVLO threshold is set by hardware.

V_{CONN} UVLO threshold is defined in VCONN_MONITORING_CTRL register.

The reset value of VCONN_PRESENCE bit is:

- 0b when V_{CONN} is not supplied on VCONN pin, or when V_{CONN} is supplied and voltage level is below UVLO threshold, or when V_{CONN} threshold detection circuit is disabled.
- 1b when V_{CONN} is supplied on VCONN pin and the voltage level is above UVLO threshold.

See Section 8.3 Electrical and timing characteristics for the threshold voltage description and value on VBUS_SENSE and VCONN pins.

5.1.7 CC_OPERATION_STATUS

Address: 11h

Access: RO

Note: This register gives the current status of the device operating modes with respect to the Type-C FSM states as defined in the USB Type-C standard specification. This status is informative only and is not used to trigger any alert.

Table 23. CC_OPERATION_STATUS register

Bit	Field name	Reset	Description
7	CC_PIN_ATTACHED	0b	0b: CC1 is attached 1b: CC2 is attached
6:5	SINK_POWER_STATE	00b	00b: PowerDefault.SNK (source supplies default USB current) 01b: Power1.5.SNK (source supplies 1.5 A USB Type-C current) 10b: Power3.0.SNK (source supplies 3.0 A USB Type-C current) 11b: do not use

Bit	Field name	Reset	Description
4:0	TYPEC_FSM_STATE	00h or 08h	00h: Unattached.SNK 01h: AttachWait.SNK 02h: Attached.SNK 03h: DebugAccessory.SNK 04h: reserved 05h: reserved 06h: reserved 07h: TryWait.SNK 08h: Unattached.SRC 09h: AttachWait.SRC 0Ah: Attached.SRC 0Bh: reserved 0Ch: Try.SRC 0Dh: Unattached.Accessory 0Eh: AttachWait.Accessory 0Fh: AudioAccessory 10h: UnorientedDebugAccessory.SRC 11h: reserved 12h: reserved 13h: ErrorRecovery 14h: TryDebounce.SNK (intermediate state towards Try.SNK state) 15h: Try.SNK 16h: reserved 17h: TryWait.SRC 18h: UnattachedWait.SRC (V_{CONN} intermediate discharge state) 19h: OrientedDebugAccessory.SRC 1Ah: reserved 1Bh: reserved 1Ch: reserved 1Dh: reserved 1Eh: reserved 1Fh: reserved

The reset value of TYPEC_FSM_STATE bits is:

- 00h when device operates in sink power role (Unattached.SNK)
- 08h when device operates in source power role (Unattached.SRC)

The CC_PIN_ATTACHED bit indicates which CC pin is connected to the CC line. Its value is consistent with the logic level of the A_B_SIDE output pin providing cable orientation.

The SINK_POWER_STATE bits indicate the current level advertised by the source that the sink can consume when the device works in sink power role.

The TYPEC_FSM_STATE bits indicate the current state of the Type-C FSM corresponding to the power mode defined in CC_POWER_MODE_CTRL register.

5.1.8 HW_FAULT_STATUS_TRANS

Address: 12h

Access: RC

Note: This register indicates a bit value change has occurred in HW_FAULT_STATUS register. It also alerts when the overtemperature condition is met.

Table 24. HW_FAULT_STATUS_TRANS register

Bit	Field name	Reset	Description
7	THERMAL_FAULT	0b	0b: cleared 1b: junction temperature is above temperature threshold of 145° C
6	Reserved	0b	Do not use
5	VPU_OVP_FAULT_TRANS	0b	0b: cleared 1b: transition occured on VPU_OVP_FAULT bit
4	VPU_VALID_TRANS	0b	0b: cleared 1b: transition occured on VPU_VALID bit
3	Reserved	0b	Do not use
2	VCONN_SW_RVP_FAULT_TRANS	0b	0b: cleared 1b: transition occured on VCONN_SW_RVP_FAULT bits
1	VCONN_SW_OCP_FAULT_TRANS	0b	0b: cleared 1b: transition occured on VCONN_SW_OCP_FAULT bits
0	VCONN_SW_OVP_FAULT_TRANS	0b	0b: cleared 1b: transition occured on VCONN_SW_OVP_FAULT bits

5.1.9 HW_FAULT_STATUS

Address: 13h

Access: RO

Note: This register provides information on hardware fault conditions related to the internal pull-up voltage in source power role and to the V_{CONN} power switches.

Table 25. HW_FAULT_STATUS register

Bit	Field name	Reset	Description
7	VPU_OVP_FAULT	0b	0b: voltage on CC pins is below OVP threshold of 6.0 V 1b: voltage on CC pins is above OVP threshold of 6.0 V
6	VPU_VALID	1b	0b: pull-up voltage on CC pins is below UVLO threshold of 2.8 V 1b: pull-up voltage on CC pins is above UVLO threshold of 2.8 V (safe condition)
5	VCONN_SW_RVP_FAULT_CC1	0b	0b: no reverse voltage on V_{CONN} power switch connected to CC1 1b: reverse voltage detected on V_{CONN} power switch connected to CC1
4	VCONN_SW_RVP_FAULT_CC2	0b	0b: no reverse voltage on V_{CONN} power switch connected to CC2 1b: reverse voltage detected on V_{CONN} power switch connected to CC2
3	VCONN_SW_OCP_FAULT_CC1	0b	0b: no short-circuit or overcurrent on V_{CONN} power switch connected to CC1 1b: short-circuit or overcurrent detected on V_{CONN} power switch connected to CC1
2	VCONN_SW_OCP_FAULT_CC2	0b	0b: no short-circuit or overcurrent on V_{CONN} power switch connected to CC2 1b: short-circuit or overcurrent detected on V_{CONN} power switch connected to CC2
1	VCONN_SW_OVP_FAULT_CC1	0b	0b: no overvoltage on V_{CONN} power switch connected to CC1 1b: overvoltage detected on V_{CONN} power switch connected to CC1
0	VCONN_SW_OVP_FAULT_CC2	0b	0b: no overvoltage on V_{CONN} power switch connected to CC2 1b: overvoltage detected on V_{CONN} power switch connected to CC2

The VPU_VALID and VPU_OVP_FAULT bits are related to the internal pull-up voltage applied on the CC pins when the device works in source power role. They inform about an internal supply issue that could prevent the device from detecting a valid connection to a distant device.

5.1.10 CC_CAPABILITY_CTRL

Address: 18h

Access: R/W

Note: When operating in source power role, this register allows the advertising of the current capability to be changed as defined in the USB Type-C standard specification and the V_{CONN} supply capability.

Table 26. **CC_CAPABILITY_CTRL register**

Bit	Field name	Reset	Description
7:6	CC_CURRENT_ADVERTISED	01b(NVM)	00b: default USB current (500 mA or 900 mA) 01b: 1.5 A USB Type-C current 10b: 3.0 A USB Type-C current 11b: do not use
5	Reserved	1b	Do not use
4	CC_VCONN_DISCHARGE_EN	0b (NVM)	0b: V_{CONN} discharge disabled on CC pin 1b: V_{CONN} discharge enabled for 250 ms on CC pin
3:1	Reserved	000b	Do not use
0	CC_VCONN_SUPPLY_EN	1b(NVM)	0b: V_{CONN} supply capability disabled on CC pin 1b: V_{CONN} supply capability enabled on CC pin

5.1.11 CC_VCONN_SWITCH_CTRL

Address: 1Eh

Access: R/W

Note: This register allows the default current limit of the power switches supplying V_{CONN} on the CC pins to be changed.

Table 27. **CC_VCONN_SWITCH_CTRL register**

Bit	Field name	Reset	Description
7:4	Reserved	0000b	Do not use
3:0	CC_VCONN_SWITCH_ILIM	0000b (NVM)	0000b: 350 mA (default) 0001b: 300 mA 0010b: 250 mA 0011b: 200 mA 0100b: 150 mA 0101b: 100 mA 0110b: 400 mA 0111b: 450 mA 1000b: 500 mA 1001b: 550 mA 1010b: 600 mA

5.1.12 VCONN_MONITORING_CTRL

Address: 20h

Access: R/W

Note: This register allows the default voltage monitoring conditions for V_{CONN} to be modified.

Table 28. **VCONN_MONITORING_CTRL register**

Bit	Field name	Reset	Description
7	VCONN_MONITORING_EN	1b	0b: disables UVLO threshold detection on VCONN pin 1b: enables UVLO threshold detection on VCONN pin

Bit	Field name	Reset	Description
6	VCONN_UVLO_THRESHOLD	0b	0b: selects high UVLO threshold (default) 1b: selects low UVLO threshold (case where V_{CONN}-powered accessories operate down to 2.7 V)
5	Reserved	1b	Do not use
4	Reserved	0b	Do not use
3:0	Reserved	0000b	Do not use

Disabling the UVLO threshold detection on VCONN pin deactivates the V_{CONN} power path and sets VCONN_PRESENCE bit to 0b in the MONITORING_STATUS register.

See Section 8.3 Electrical and timing characteristics for the threshold voltage description and value on VCONN pin.

5.1.13 VBUS_MONITORING_RANGE_CTRL

Address: 22h

Access: R/W

Note: This register allows the low and high limits of the V_{BUS} monitoring voltage range to be changed during attachment.

Table 29. VBUS_MONITORING_RANGE_CTRL register

Bit	Field name	Reset	Description
7:4	SHIFT_HIGH_VBUS_LIMIT	0000b (NVM)	Binary coded V_{SHUSBH} coefficient to shift up the nominal high voltage limit from 1% (0001b) to 15% (1111b) of V_{BUS} voltage by step of 1%
3:0	SHIFT_LOW_VBUS_LIMIT	0000b (NVM)	Binary coded V_{SHUSBL} coefficient to shift down the nominal low voltage limit from 1% (0001b) to 15% (1111b) of V_{BUS} voltage by step of 1%

V_{BUS} voltage is fixed at 5.0 V. The nominal values of the high and low limits of V_{BUS} monitoring voltage range are respectively V_{BUS}+5% and V_{BUS}-5%. Each coefficient V_{SHUSBH} and V_{SHUSBL} represents the fraction of V_{BUS} voltage that is either added or subtracted to the nominal value of the corresponding limit to determine the V_{BUS} monitoring voltage limits (see Section 8.3 Electrical and timing characteristics).

When STUSB1600 is in unattached state, the register takes the reset values. When a device is attached, the register takes the values set in the NVM (see Section 6 Start-up configuration) or those set by software during attachment.

The register is valid for both power role. Depending on whether the device operates in source power role or sink power role, the register takes the values set in the NVM related to the running power role.

5.1.14 RESET_CTRL

Address: 23h

Access: R/W

Note: This register allows the device to be reset by software.

Table 30. RESET_CTRL register

Bit #	Field Name	Reset	Description
7:1	Reserved	0000000b	Do not use
0	SW_RESET_EN	0b	0b: device reset is performed by hardware RESET pin 1b: forces the device reset as long as this bit value is set

The SW_RESET_EN bit acts as the hardware RESET pin except that I^2C control registers are not reset to their default value. They keep the last changed value. The SW_RESET_EN bit does not command the RESET pin.

5.1.15 VBUS_DISCHARGE_TIME_CTRL

Address: 25h

Access: R/W

Note: This register contains the parameter used to define the V_{BUS} discharge time when the internal V_{BUS} discharge path is activated on VBUS_SENSE pin.

Table 31. **VBUS_DISCHARGE_TIME_CTRL register**

Bit	Field name	Reset	Description
7:4	VBUS_DISCHARGE_TIME_TO_0V	0110b (NVM)	Binary coded $T_{DISPARAM}$ coefficient used to compute the V_{BUS} discharge time to 0 V: T_{DISUSB} =84 ms (typical) * $T_{DISPARAM}$
3:0	Reserved	1111b	Do not use

5.1.16 VBUS_DISCHARGE_STATUS

Address: 26h

Access: RO

Note: This register gives information during the operation on the activation state of the internal V_{BUS} discharge path on VBUS_SENSE pin.

Table 32. **VBUS_DISCHARGE_STATUS register**

Bit	Field name	Reset	Description
7	VBUS_DISCHARGE_EN	0b	0b: V_{BUS} discharge path is deactivated 1b: V_{BUS} discharge path is activated
6:1	Reserved	0000000b	Do not use

5.1.17 VBUS_ENABLE_STATUS

Address: 27h

Access: R0

Note: This register gives some information during operations on the activation state of the V_{BUS} power path through VBUS_EN_SRC pin in source power role and VBUS_EN_SNK pin in sink power role.

Table 33. **VBUS_ENABLE_STATUS register**

Bit	Field name	Reset	Description
7:2	Reserved	0b	Do not use
1	VBUS_SINK_EN	0b	0b: V_{BUS} sink power path is disabled 1b: V_{BUS} sink power path is enabled
0	VBUS_SOURCE_EN	0b	0b: V_{BUS} source power path is disabled 1b: V_{BUS} source power path is enabled

5.1.18 CC_POWER_MODE_CTRL

Address: 28h

Access: R/W

Note: this register allows the default Type-C power mode to be changed if needed during an operation. It requires that the hardware implementation of the targeted application is consistent with the functioning of the new Type-C power mode selected.

Table 34. CC_POWER_MODE_CTRL register

Bit	Field name	Reset	Description
7:3	Reserved	00000b	Do not use
2:0	CC_POWER_MODE	011 (NVM)	000b: source power role with accessory support 001b: sink power role with accessory support 010b: sink power role without accessory support 011b: dual power role with accessory support 100b: dual power role with accessory and Try.SRC support 101b: dual power role with accessory and Try.SNK support 110b: do not use 111b: do not use

5.1.19 VBUS_MONITORING_CTRL

Address: 2Eh

Access: R/W

Note: this register allows the default monitoring conditions of the V_{BUS} voltage over the power path from the VDD and VBUS_SENSE pins to be modified.

Table 35. VBUS_MONITORING_CTRL register

Bit	Field name	Reset	Description
7	Reserved	0b	Do not use
6	VDD_OVLO_DISABLE	0b(NVM)	0b: enables OVLO threshold detection on VDD pin 1b: disables OVLO threshold detection on VDD pin
5	Reserved	0b	Do not use
4	VBUS_VALID_RANGE_DISABLE	0b(NVM)	0b: enables valid V_{BUS} voltage range detection 1b: disables valid V_{BUS} voltage range detection (V_{BUS} UVLO threshold detection used instead)
3	Reserved	0b	Do not use
2:1	VBUS_VSAFE0V_THRESHOLD	00b (NVM)	00b : V_{BUS} vSafe0V threshold = 0.6 V 01b : V_{BUS} vSafe0V threshold = 0.9 V 10b : V_{BUS} vSafe0V threshold = 1.2 V 11b : V_{BUS} vSafe0V threshold = 1.8 V
0	VDD_UVLO_DISABLE	1b(NVM)	0b: enables UVLO threshold detection on VDD pin 1b: disables UVLO threshold detection on VDD pin

The VBUS_VALID_RANGE_DISABLE and VBUS_VSAFE0V_THRESHOLD bits define monitoring conditions applicable to VBUS_SENSE pin connected to USB Type-C receptacle side.

The VBUS_VALID_RANGE_DISABLE bit allows the valid V_{BUS} voltage range conditions to be substituted by the V_{BUS} UVLO threshold condition to establish a valid device attachment and to assert the V_{BUS} power path.

The VBUS_VSAFE0V_THRESHOLD bit indicates the voltage value of the V_{BUS} vSafe0V threshold used in source power role as a Type-C FSM condition to establish a valid device attachment.

The VDD_UVLO_DISABLE and VDD_OVLO_DISABLE bit define monitoring conditions applicable to VDD supply pin when it is connected to the main power supply in source power role only:

- When UVLO detection is enabled, VBUS_EN_SRC pin is asserted only if voltage on VDD pin is above V_{DDUVLO} threshold
- When OVLO detection is enabled, VBUS_EN_SRC pin is asserted only if voltage on VDD pin is below V_{DDOVLO} threshold

See Section 8.3 Electrical and timing characteristics for the threshold voltage description and value on VDD and VBUS_SENSE pins.

6 Start-up configuration

6.1 User-defined parameters

The STUSB1600 has a set of user-defined parameters that can be customized by NVM re-programming and/or by software through I²C interface. It allows the customer to change the preset configuration of USB Type-C interface and to define a new configuration to meet specific customer requirements addressing various applications, use cases or specific implementations.

The NVM re-programming overrides the initial default setting to define a new default setting that is used at power-up or after a reset. The default value is copied at power-up, or after a reset, from the embedded NVM into dedicated I²C register bits (see Section 5.1 Register description).

When a default value is changed during functioning by software, the new setting remains in effect as long as the STUSB1600 operates or when it is changed again. But after power-off and power-up, or after a reset, the STUSB1600 takes back default values defined in the NVM.

6.2 Default start-up configuration

The table below lists the user-defined parameters and indicates the default start-up configuration of the STUSB1600.

Three types of user-defined parameters are specified in the table with respect to the “Customization type” column:

- SW: indicates parameters that can be customized only by software through I²C interface during system operations
- NVM: indicates parameters that can be customized by NVM re-programming only
- NVM/SW: indicates parameters that can be customized by NVM re-programming and/or by software
- through I²C interface during system operations

Table 36. STUSB1600 user-defined parameters and default settings

Customization type	Parameter	Default value and description	I²C register address
NVM / SW	CC_CONNECTION_STATUS_AL_MASK	1b: interrupt masked	0Ch
NVM / SW	MONITORING_STATUS_AL_MASK	1b: interrupt masked	0Ch
NVM / SW	HW_FAULT_STATUS_AL_MASK	1b: interrupt masked	0Ch
NVM	STANDBY_POWER_MODE_DISABLE	1b: disables standby power mode	n. a.
NVM / SW	CC_CURRENT_ADVERTISED	01b: 1.5 A	18h
NVM / SW	CC_VCONN_DISCHARGE_EN	0b: V_{CONN} discharge disabled on CC pin	18h
NVM / SW	CC_VCONN_SUPPLY_EN	1b: V_{CONN} supply capability enabled on CC pin	18h
NVM / SW	CC_VCONN_SWITCH_ILIM	0000b: 350 mA	1Eh
SW	VCONN_MONITORING_EN	1b: enables UVLO threshold detection on VCONN pin	20h
SW	VCONN_UVLO_THRESHOLD	0b: high UVLO threshold of 4.65 V	20h
NVM / SW	SHIFT_HIGH_VBUS_LIMIT_SOURCE	0101b: V_{SHUSBH} = 5% of V_{BUS}, high voltage limit $V_{MONUSBH\ Source}$ = V_{BUS}+10%	22h
NVM / SW	SHIFT_LOW_VBUS_LIMIT_SOURCE	0101b: V_{SHUSBL} = 5% of V_{BUS}, low voltage limit $V_{MONUSBL\ Source}$ = V_{BUS}-10%	22h

Customization type	Parameter	Default value and description	I²C register address
NVM/SW	SHIFT_HIGH_VBUS_LIMIT_SINK	0101b: V_{SHUSBH} = 5% of V_{BUS}, high voltage limit $V_{MONUSBH\ Sink}$ = V_{BUS}+10%	22h
NVM / SW	SHIFT_LOW_VBUS_LIMIT_SINK	1111b: V_{SHUSBL} = 15% of V_{BUS}, low voltage limit $V_{MONUSBL\ Sink}$ = V_{BUS}-20%	22h
SW	SW_RESET_EN	0b: device reset is performed from hardware RESET pin	23h
NVM / SW	VBUS_DISCHARGE_TIME_TO_0V	0110b:$_{TDISPARAM}$ = 6, discharge time T_{DISUSB} = 504 ms	25h
NVM	VBUS_DISCHARGE_DISABLE	0b: enables V_{BUS} discharge path	n.a.
NVM / SW	CC_POWER_MODE	011b: dual power role with accessory support	28h
NVM / SW	VDD_OVLO_DISABLE	0b: enables OVLO threshold detection on VDD pin	2Eh
NVM / SW	VDD_VALID_RANGE_DISABLE	0b: enables valid V_{BUS} voltage range detection	2Eh
NVM / SW	VBUS_VSAFE0V_THRESHOLD	00b: V_{BUS} vSafe0V threshold = 0.6 V	2Eh
NVM / SW	VDD_UVLO_DISABLE	1b: disables UVLO threshold detection on VDD pin	2Eh

7 Application

The sections below are not part of ST product specifications. They are intended to give a generic application overview to be used by the customer as a starting point for further implementations and customizations. ST does not warrant compliance with customer specifications. Full system implementation and validation are under customer's responsibility.

7.1 General information

7.1.1 Power supplies

The STUSB1600 can be supplied in three different ways depending on the targeted application:

- Through VDD pin only for applications powered by V_{BUS} only that operate either in source power role or in sink power role with dead-battery mode support
- Through VSYS pin only for AC-powered applications with a system power supply delivering 3.3 V or 5 V
- Through VDD and VSYS pins either for applications powered by a battery with a dead-battery mode support or for applications powered by V_{BUS} with a system power supply delivering 3.3 V or 5 V. When both VDD and VSYS power supplies are present, the low power supply VSYS is selected when VSYS voltage is above 3.1 V. Otherwise VDD is selected

7.1.2 Connection to MCU or application processor

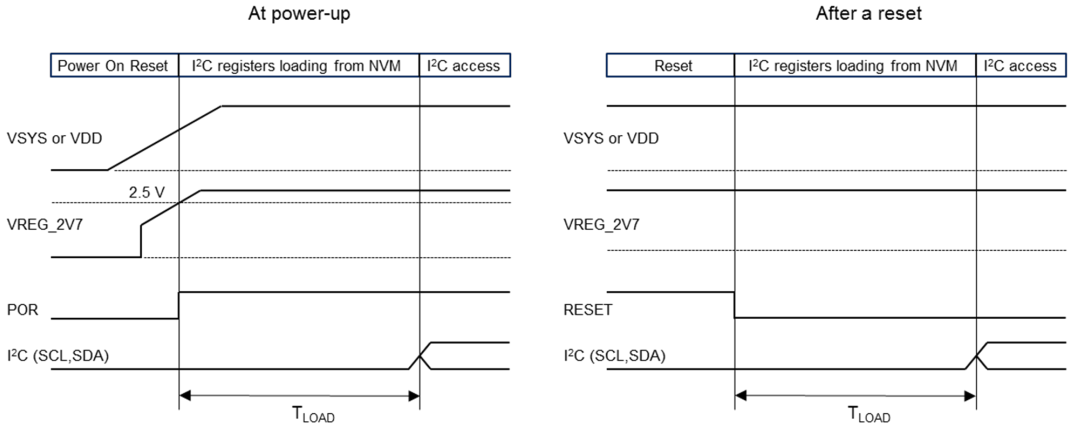
The connection to an MCU or an application processor is optional.

When a connection through I²C interface is implemented, it provides extensive functionality during system operations. For instance, it may be used to:

1. Define the port configuration during system boot (in case the NVM parameters are not customized during manufacturing)
2. Change the default configuration at any time during operations
3. Re-configure the port power mode (i.e. source, sink or dual role),
4. Adjust the port power capability in source power role according to contextual power availability and/or the power partitioning with other ports
5. Save system power by shutting down the DC-DC converter according to the attachment detection state
6. Provide a diagnostic of the Type-C connection and the V_{BUS} power path in real time

At power-up or after a reset, the first software access to the I²C registers of the STUSB1600 can happen only after T_{LOAD} as shown in the figure below. T_{LOAD} corresponds to the time required to initialize the I²C registers with the default values from the embedded NVM. At power-up, the loading phase starts when the voltage level on the VREG_2V7 output pin of the 2.7 V internal regulator reaches 2.5 V to release the internal POR signal. After a reset, the loading phase starts when the signal on the RESET pin is released.

Figure 7. I²C register initialization sequence at power-up or after a reset

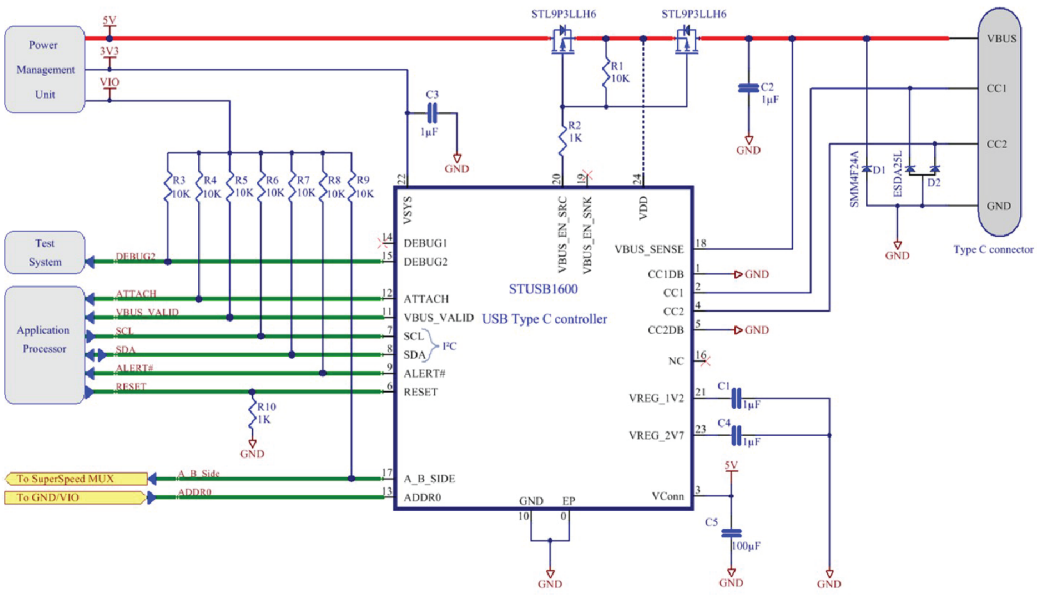


7.2 USB Type-C typical applications

7.2.1 Source type applications

7.2.1.1 *Application schematic*

Figure 8. Implementation example in source type application



7.2.1.2 *Default start-up configuration*

Table 37. Default setting for a source type application

Customization type	Parameter	Default value and description	I²C register address
NVM /SW	CC_CONNECTION_STATUS_AL_MASK	1b: interrupt masked	0Ch
NVM /SW	MONITORING_STATUS_AL_MASK	1b: interrupt masked	0Ch
NVM /SW	HW_FAULT_STATUS_AL_MASK	1b: interrupt masked	0Ch
NVM	STANDBY_POWER_MODE_DISABLE	1b: disables standby power mode	n. a.
NVM /SW	CC_CURRENT_ADVERTISED	01b: 1.5 A	18h
NVM /SW	CC_VCONN_DISCHARGE_EN	0b: VCONN discharge disabled on CC pin	18h
NVM /SW	CC_VCONN_SUPPLY_EN	1b: VCONN supply capability enabled on CC pin	18h
NVM /SW	CC_VCONN_SWITCH_ILIM	0000b: 350 mA	1Eh
SW	VCONN_MONITORING_EN	1b: enables UVLO threshold detection on VCONN pin	20h
SW	VCONN_UVLO_THRESHOLD	0b: high UVLO threshold of 4.65 V	20h
NVM /SW	SHIFT_HIGH_VBUS_LIMIT_SOURCE	0101b: V_{SHUSBH} = 5% of V_{BUS}, high voltage limit $V_{MONUSBH\ Source}$ = V_{BUS}+10%	22h

Customization type	Parameter	Default value and description	I²C register address
NVM /SW	SHIFT_LOW_VBUS_LIMIT_SOURCE	0101b: V_{SHUSBL} = 5% of V_{BUS}, low voltage limit $V_{MONUSBL\ Source}$ = V_{BUS}-10%	22h
SW	SW_RESET_EN	0b: device reset is performed from hardware RESET pin	23h
NVM /SW	VBUS_DISCHARGE_TIME_TO_0V	0110b: $T_{DISPARAM}$ = 6, discharge time T_{DISUSB} = 504 ms	25h
NVM	VBUS_DISCHARGE_DISABLE	0b: enables V_{BUS} discharge path	n. a.
NVM /SW	CC_POWER_MODE	000b: source power role with accessory support (1)	28h
NVM /SW	VDD_OVLO_DISABLE	0b: enables OVLO threshold detection on VDD pin	2Eh
NVM /SW	VBUS_VALID_RANGE_DISABLE	0b: enables valid V_{BUS} voltage range detection	2Eh
NVM /SW	VBUS_VSAFE0V_THRESHOLD	00b : V_{BUS} vSafe0V threshold = 0.6 V	2Eh
NVM /SW	VDD_UVLO_DISABLE	1b: disables UVLO threshold detection on VDD pin	2Eh

1. *Indicates parameter customized by NVM re-programming.*

7.2.1.3 *V_{BUS} power path assertion*

Table 38. Conditions for V_{BUS} power path assertion in source power role

Pin	Electrical value	Operation conditions			Comment
		Type-C attached state	VDD pin monitoring	VBUS_SENSE pin monitoring	
VBUS_EN_SRC	0	Attached.SRC or UnorientedDebug Accessory.SRC or OrientedDebug Accessory.SRC	V_{DD} < V_{DDOVLO} if VDD pin is supplied	V_{BUS} is within valid voltage range	The signal is asserted only if all the valid operation conditions are met
	HiZ	Any other state	V_{DD} > V_{DDOVLO} if VDD pin is supplied	V_{BUS} is out of valid voltage range	The signal is de-asserted when at least one non-valid operation condition is met.

7.2.1.4 *Device state according to connection state*

Table 39. Source power role with accessory support

Connection state	CC1 pin	CC2 pin	Type-C device state CC_OPERATION_STATUS register@11h	A_B_SIDE pin	VCONN supply	VBUS_EN_SRC pin	CC_CONNECTION_STATUS register @0Eh
Nothing attached	Open	Open	Unattached.SRC	HiZ	OFF	HiZ	00h

Connection state	CC1 pin	CC2 pin	Type-C device state CC_OPERATION_ STATUS register@11h	A_B_SIDE pin	VCONN supply	VBUS_EN_SRC pin	CC_CONNECTION_ STATUS register @0Eh
Sink attached	Rd	Open	Attached.SRC	HiZ	OFF	0	2Dh
	Open	Rd		0	OFF	0	2Dh
Powered cable without sink attached	Open	Ra	Unattached.SRC	HiZ	OFF	HiZ	00h
	Ra	Open		HiZ	OFF	HiZ	00h
Powered cable with sink attached or Vconn-powered Accessory attached	Rd	Ra	Attached.SRC	HiZ	CC2	0	2Fh
	Ra	Rd		0	CC1	0	2Fh
Debug accessory mode attached source role	Rp	Rp	Unattached.SRC	HiZ	OFF	HiZ	00h
Debug accessory mode attached sink role	Rd	Rd	UnorientedDebug Accessory.SRC	HiZ	OFF	0	6Dh
Debug accessory mode attached sink role	Rd	≤Ra	OrientedDebug Accessory.SRC	HiZ	OFF	0	6Dh
	≤Ra	Rd		0	OFF	0	6Dh
Audio adapter accessory mode attached	Ra	Ra	AudioAccessory	HiZ	OFF	HiZ	81h

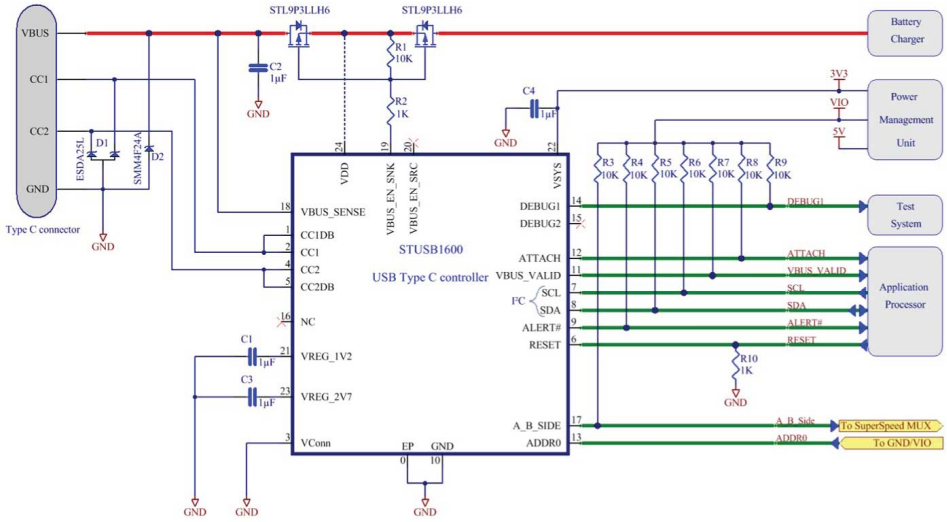
The value of CC1 and CC2 pins is defined from a termination perspective and corresponds to the termination presented by the connected device.

The CC_CONNECTION_STATUS register can report other values than the one presented in this table. This reflects the state transitions in Type-C FSM that can be ignored from the application stand point.

7.2.2 Sink type application

7.2.2.1 *Application schematic in sink type*

Figure 9. Implementation example in sink type application



Note: The schematic configuration is in dead-battery mode.

7.2.2.2 *Default start-up configuration in sink type*

Table 40. Default setting for a sink type application

Customization type	Parameter	Default value and description	I²C register address
NVM / SW	CC_CONNECTION_STATUS_AL_MASK	1b: interrupt masked	0Ch
NVM / SW	MONITORING_STATUS_AL_MASK	1b: interrupt masked	0Ch
NVM / SW	HW_FAULT_STATUS_AL_MASK	1b: interrupt masked	0Ch
NVM	STANDBY_POWER_MODE_DISABLE	1b: disables standby power mode	n. a.
NVM / SW	CC_CURRENT_ADVERTISED	01b: 1.5 A	18h
NVM / SW	CC_VCONN_DISCHARGE_EN	0b: VCONN discharge disabled on CC pin	18h
NVM / SW	CC_VCONN_SUPPLY_EN	1b: VCONN supply capability enabled on CC pin	18h
NVM / SW	CC_VCONN_SWITCH_ILIM	0000b: 350 mA	1Eh
SW	VCONN_MONITORING_EN	1b: enables UVLO threshold detection on VCONN pin	20h
SW	VCONN_UVLO_THRESHOLD	0b: high UVLO threshold of 4.65 V	20h
NVM / SW	SHIFT_HIGH_VBUS_LIMIT_SINK	0101b: V_{SHUSBH} = 5% of V_{BUS}, high voltage limit $V_{MONUSBH\ Sink}$ = V_{BUS}+10%	22h

Customization type	Parameter	Default value and description	I²C register address
NVM / SW	SHIFT_LOW_VBUS_LIMIT_SINK	1111b: V_{SHUSBL} = 15% of V_{BUS}, low voltage limit $V_{MONUSBL\ Sink}$ = V_{BUS}-20%	22h
SW	SW_RESET_EN	0b: device reset is performed from hardware RESET pin	23h
NVM / SW	VBUS_DISCHARGE_TIME_TO_0V	0110b: $T_{DISPARAM}$ = 6, discharge time T_{DISUSB} = 504 ms	25h
NVM	VBUS_DISCHARGE_DISABLE	0b: enables V_{BUS} discharge path	n. a.
NVM / SW	CC_POWER_MODE	001b: sink power role with accessory support(1)	28h
NVM / SW	VDD_OVLO_DISABLE	0b: enables OVLO threshold detection on VDD pin	2Eh
NVM / SW	VBUS_VALID_RANGE_DISABLE	0b: enables valid V_{BUS} voltage range detection	2Eh
NVM / SW	VBUS_VSAFE0V_THRESHOLD	00b: V_{BUS} vSafe0V threshold = 0.6 V	2Eh
NVM / SW	VDD_UVLO_DISABLE	1b: disables UVLO threshold detection on VDD pin	2Eh

1. *Indicates parameter customized by NVM re-programming.*

7.2.2.3 *V_{BUS} power path assertion in sink power role*

Table 41. Conditions for V_{BUS} power path assertion in sink power role

Pin	Electrical value	Operation conditions			Comment
		Type-C attached state	VDD pin monitoring	VBUS_SENSE pin monitoring	
VBUS_EN_SNK	0	Attached.SNK or DebugAccessory.SNK	Not applicable	V_{BUS} is within valid voltage range	The signal is asserted only if all the valid operation conditions are met.
	HiZ	Any other state	Not applicable	V_{BUS} is out of valid voltage range	The signal is de-asserted when at least one non-valid operation condition is met.

7.2.2.4 *Device state according to connection state (sink power role)*

Table 42. Sink power role with accessory support

Connection state	CC1 pin	CC2 pin	Type-C device state CC_OPERATION_ STATUS register @11h	A_B_SIDE pin	VCONN supply	VBUS_EN_SNK pin	CC_CONNECTION_ STATUS register @0Eh
Nothing attached	Open	Open	(Toggling) Unattached. SNK Unattached. ACC	HiZ	OFF	HiZ	00h

Connection state	CC1 pin	CC2 pin	Type-C device state CC_OPERATION_ STATUS register @11h	A_B_SIDE pin	VCONN supply	VBUS_EN_SNK pin	CC_CONNECTION_ STATUS register @0Eh
Source attached	Rp	Open or Ra	Attached. SNK	HiZ	OFF	0	41h
	Open or Ra	Rp		0	OFF	0	41h
Powered cable without source attached	Open	Ra	(Toggling) Unattached. SNK Unattached. ACC	HiZ	OFF	HiZ	00h
	Ra	Open		HiZ	OFF	HiZ	00h
Debug accessory mode attached sink role	Rd	Rd	(Toggling) Unattached. SNK Unattached. ACC	HiZ	OFF	HiZ	00h
Debug accessory mode attached source role	Rp def/ 1.5 A/ 3 A	Rp def/ 1.5A/3A	Debug Accessory.SNK (default USB)	HiZ	OFF	0	61h
Debug accessory mode attached source role	Rp 3 A	Rp 1.5 A	Debug Accessory.SNK (Default USB)	HiZ	OFF	0	61h
	Rp 1.5 A	Rp 3 A		0			61h
Debug accessory mode attached source role	Rp 1.5 A	Rp def.	Debug Accessory.SNK (1.5 A)	HiZ	OFF	0	61h
	Rp def.	Rp 1.5 A		0			61h
Debug accessory mode attached source role	Rp 3 A	Rp def.	Debug Accessory.SNK (3.0 A)	HiZ	OFF	0	61h
	Rp def.	Rp 3 A		0			61h
Audio adapter accessory mode attached	Ra	Ra	Audio accessory	HiZ	OFF	HiZ	81h
VCONN-powered accessory attached	Rd	Ra	(Toggling) Unattached. SNK Unattached. ACC	HiZ	OFF	HiZ	00h
	Ra	Rd		HiZ	OFF	HiZ	00h

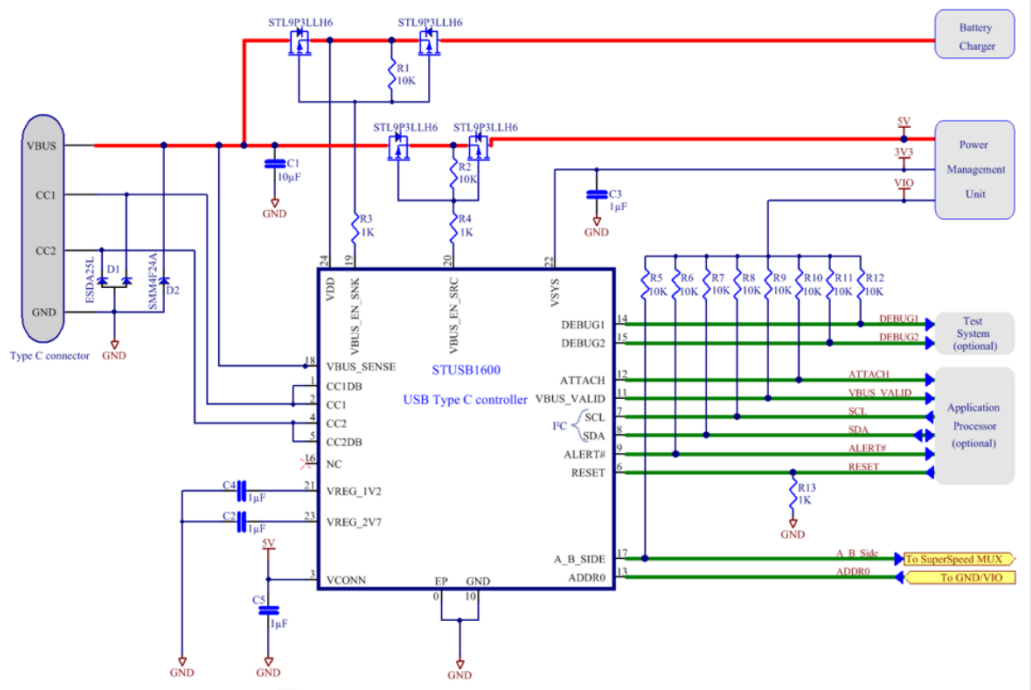
The value of CC1 and CC2 pins is defined from a termination perspective and corresponds to the termination presented by the connected device.

The CC_CONNECTION_STATUS register can report other values than the one presented inside this table. This reflects the state transitions in Type-C FSM that can be ignored from the application stand point.

7.2.3 Dual role type application

7.2.3.1 Application schematic in dual role type

Figure 10. Implementation example in dual role type application



Note: The schematic configuration in dead-battery mode.

7.2.3.2 *Default start-up configuration in dual role type application*

Table 43. Default setting for a dual role type application

Customization type	Parameter	Default value and description	I²C register address
NVM / SW	CC_CONNECTION_STATUS_AL_MASK	1b: interrupt masked	0Ch
NVM / SW	MONITORING_STATUS_AL_MASK	1b: interrupt masked	0Ch
NVM / SW	HW_FAULT_STATUS_AL_MASK	1b: interrupt masked	0Ch
NVM	STANDBY_POWER_MODE_DISABLE	1b: disables standby power mode	n. a.
NVM / SW	CC_CURRENT_ADVERTISED	01b: 1.5 A	18h
NVM / SW	CC_VCONN_DISCHARGE_EN	0b: VCONN discharge disabled on CC pin	18h
NVM / SW	CC_VCONN_SUPPLY_EN	1b: VCONN supply capability enabled on CC pin	18h
NVM / SW	CC_VCONN_SWITCH_ILIM	0000b: 350 mA	1Eh
SW	VCONN_MONITORING_EN	1b: enables UVLO threshold detection on VCONN pin	20h
SW	VCONN_UVLO_THRESHOLD	0b: high UVLO threshold of 4.65 V	20h
NVM / SW	SHIFT_HIGH_VBUS_LIMIT_SOURCE	0101b: V_{SHUSBH} = 5% of V_{BUS}, high voltage limit $V_{MONUSBH\ Source}$ = V_{BUS} +10%	22h
NVM / SW	SHIFT_LOW_VBUS_LIMIT_SOURCE	0101b: V_{SHUSBL} = 5% of V_{BUS}, low voltage limit $V_{MONUSBL\ Source}$ = V_{BUS}-10%	22h
NVM / SW	SHIFT_HIGH_VBUS_LIMIT_SINK	0101b: V_{SHUSBH} = 5% of V_{BUS}, high voltage limit $V_{MONUSBH\ Sink}$ = V_{BUS}+10%	22h
NVM / SW	SHIFT_LOW_VBUS_LIMIT_SINK	1111b: V_{SHUSBL} = 15% of V_{BUS}, low voltage limit $V_{MONUSBL\ Sink}$ = V_{BUS}-20%	22h
SW	SW_RESET_EN	0b: device reset is performed from hardware RESET pin	23h
NVM / SW	VBUS_DISCHARGE_TIME_TO_0V	0110b:$T_{DISPARAM}$ = 6, discharge time T_{DISUSB} = 504 ms	25h
NVM	VBUS_DISCHARGE_DISABLE	0b: enables V_{BUS} discharge path	n. a.
NVM / SW	CC_POWER_MODE	011b: dual power role with accessory support	28h
NVM / SW	VDD_OVLO_DISABLE	0b: enables OVLO threshold detection on VDD pin	2Eh
NVM / SW	VBUS_VALID_RANGE_DISABLE	0b: enables valid V_{BUS} voltage range detection	2Eh
NVM / SW	VBUS_VSAFE0V_THRESHOLD	00b : V_{BUS} vSafe0V threshold = 0.6 V	2Eh
NVM / SW	VDD_UVLO_DISABLE	1b: disables UVLO threshold detection on VDD pin	2Eh

7.2.3.3 V_{BUS} power path assertion in dual role

Table 44. Conditions for V_{BUS} power path assertion in source power role

Pin	Electrical value	Operation conditions			Comment
		Type-C attached state	VDD pin monitoring	VBUS_SENSE pin monitoring	
VBUS_EN_SRC	0	Attached.SRC or UnorientedDebug Accessory.SRC or OrientedDebug Accessory.SRC	$V_{DD} < V_{DDOVLO}$ if VDD pin is supplied	V_{BUS} within valid voltage range	The signal is asserted only if all the valid operation conditions are met
	HiZ	Any other state	$VDD > V_{DDOVLO}$ if VDD pin is supplied	V_{BUS} is out of valid voltage range	The signal is de-asserted when at least one non-valid operation condition is met

Table 45. Conditions for V_{BUS} power path assertion in sink power role

Pin	Electrical value	Operation conditions			Comment
		Type-C attached state	VDD pin monitoring	VBUS_SENSE pin monitoring	
VBUS_EN_SNK	0	Attached.SNK or Debug Accessory.SNK	Not applicable	V_{BUS} is within valid voltage range	The signal is asserted only if all the valid operation conditions are met
	HiZ	Any other state	Not applicable	V_{BUS} is out of valid voltage range	The signal is de-asserted when at least one non-valid operation condition is met

7.2.3.4 *Device state according to connection state (dual role)*

Table 46. Dual power role with accessory support

Connect. state	CC1 pin	CC2 pin	Type-C device state CC_ OPERAT_ STATUS register @11h	A_B_SIDE pin	VCONN supply	VBUS_EN_SRC pin	VBUS_EN_SNK pin	CC_CONNECTION_ STATUS register @0Eh
Nothing attached	Open	Open	(Toggling) Unattached.SRC Unattached.SNK	HiZ	OFF	Hiz	HiZ	00h
Sink attached	Rd	Open	Attached. SRC	HiZ	OFF	0	HiZ	2Dh
	Open	Rd		0	OFF	0	HiZ	2Dh
Powered cable without sink or source attached	Open	Ra	(Toggling) Unattached.SRC Unattached.SNK	HiZ	OFF	HiZ	HiZ	00h
	Ra	Open		HiZ	OFF	HiZ	HiZ	00h
Powered cable with sink attached or V_{CONN} powered accessory attached	Rd	Ra	Attached. SRC	HiZ	CC2	0	HiZ	2Fh
	Ra	Rd		0	CC1	0	HiZ	2Fh
Debug accessory mode attached sink role	Rd	Rd	UnorientedDebug Accessory.SRC	HiZ	OFF	0	Hiz	6Dh
Debug accessory mode attached sink role	Rd	≤Ra	Oriented Debug Accessory.SRC	HiZ	OFF	0	HiZ	6Dh
	≤Ra	Rd		0	OFF	0	HiZ	6Dh
Audio adapter accessory mode attached	Ra	Ra	Audio Accessory	HiZ	OFF	HiZ	HiZ	81h
Source attached	Rp	Open or Ra	Attached. SNK	HiZ	OFF	HiZ	0	41h
	Open or Ra	Rp		0	OFF	HiZ	0	41h
Debug accessory mode attached source role	Rp def/ 1.5 A/3 A	Rp def/ 1.5 A/3 A	Debug Accessory.SNK (default USB)	HiZ	OFF	HiZ	0	61h
	Rp 3 A	Rp 1.5 A		HiZ	OFF	HiZ	0	61h
	Rp 1.5 A	Rp 3 A		0	OFF	HiZ	0	61h

Connect. state	CC1 pin	CC2 pin	Type-C device state CC_ OPERAT_ STATUS register @11h	A_B_SIDE pin	VCONN supply	VBUS_EN_SRC pin	VBUS_EN_SNK pin	CC_CONNECTION_ STATUS register @0Eh
Debug accessory mode attached source role	Rp 1.5 A	Rp def.	Debug Accessory.SNK (1.5 A)	HiZ	OFF	HiZ	0	61h
	Rp def	Rp 1.5 A		0	OFF	HiZ	0	61h
Debug accessory mode attached source role	Rp 3 A	Rp def.	Debug Accessory.SNK (3.0 A)	HiZ	OFF	HiZ	0	61h
	Rp def.	Rp 3 A		0	OFF	HiZ	0	61h

The value of CC1 and CC2 pins is defined from a termination perspective and corresponds to the termination presented by the connected device.

The CC_CONNECTION_STATUS register can report other values than the one presented inside this table. This reflects the state transitions in Type-C FSM that can be ignored from the application stand point.

8 Electrical characteristics

8.1 Absolute maximum ratings

All voltages are referenced to GND.

Table 47. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DD}	Supply voltage on VDD pin	28	V
V_{SYS}	Supply voltage on VSYS pin	6	
V_{CC1}, V_{CC2} V_{CC1DB}, V_{CC2DB}	High voltage on CC pins	22	
$V_{VBUS_EN_SRC}$ $V_{VBUS_EN_SNK}$ V_{VBUS_SENSE}	High voltage on V_{BUS} pins	28	
V_{SCL}, V_{SDA} $V_{ALERT\#}$ V_{RESET} V_{ATTACH} $V_{A_B_SIDE}$ V_{BUS_VALID} V_{DEBUG1} V_{DEBUG2}	Operating voltage on I/O pins	-0.3 to 6	
V_{CONN}	V_{CONN} voltage	6	
T_{STG}	Storage temperature	-55 to 150	°C
T_J	Maximum junction temperature	145	
ESD	HBM	4	kV
	CDM	1.5	

8.2 Operating conditions

Table 48. Operating conditions

Symbol	Parameter	Value	Unit
V_{DD}	Supply voltage on VDD pin	4.1 to 22	V
V_{SYS}	Supply voltage on VSYS pin	3.0 to 5.5	
V_{CC1}, V_{CC2} V_{CC1DB}, V_{CC2DB}	CC pins	0 to 5.5	
$V_{VBUS_EN_SRC}$ $V_{VBUS_EN_SNK}$ V_{VBUS_SENSE}	High voltage pins	0 to 22	
V_{SCL}, V_{SDA} $V_{ALERT\#}$ V_{RESET} V_{ATTACH} $V_{A_B_SIDE}$ V_{VBUS_VALID} V_{DEBUG1} V_{DEBUG2}	Operating voltage on I/O pins	0 to 4.5	
V_{CONN}	V_{CONN} voltage	2.7 to 5.5	
I_{CONN}	V_{CONN} rated current (default = 0.35 A)	0.1 to 0.6	A
T_A	Operating temperature	-40 to 105	°C

8.3 Electrical and timing characteristics

Unless otherwise specified: V_{DD} = 5 V, T_A = 25 °C, all voltages are referred to GND.

Table 49. Electrical characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$I_{DD(SRC)}$	Current consumption	Device idle as a SOURCE (not connected, no communication) V_{SYS} @ 3.3 V		158		µA
		Device idle as a SOURCE (not connected, no communication) V_{DD} @ 5.0 V		188		
$I_{DD (SNK)}$	Current consumption	Device idle as a SINK (not connected, no communication) V_{SYS} @ 3.3 V		113		
		Device idle as a SINK (not connected, no communication) V_{DD} @ 5.0 V		140		
I_{STDBY}	Standby current consumption	Device standby (not connected, low power) V_{SYS} @ 3.3 V		33		
		Device standby (not connected, low power) V_{DD} @ 5.0 V		53		
T_{LOAD}	I^2C registers loading time from NVM	at power-up after a reset			30	ms
CC1 and CC2 pins						
I_{P-USB}	CC current sources	CC pin voltage V_{CC} = 0 to 2.6 V, 40 °C < T_A < +105 °C	-20%	80	+20%	µA
$I_{P-1.5}$			-8%	180	+8%	
$I_{P-3.0}$			-8%	330	+8%	
V_{CCO}	CC open pin voltage	CC unconnected, V_{DD} = 3.0 to 5.5 V	2.75			V
R_d	CC pull-down resistors	-40 °C < T_A < +105 °C	-10%	5.1	+10%	kΩ
$V_{CCDB-1.5}$	CC pin voltage in dead battery condition	External I_P = 180 µA applied into CC			1.2	V
$V_{CCDB-3.0}$		External I_P = 330 µA applied into CC V_{DD} = 0 V, dead-battery function enabled			2.0	
R_{INCC}	CC input impedance	Pull-up and pull-down resistors off	200			kΩ

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$V_{TH0.2}$	Detection threshold 1	Max. R_a detection by source at $I_P = I_{P\text{-}USB}$, min. I_{P_USB} detection by sink on R_d, min. CC voltage for connected sink	0.15	0.20	0.25	V
$V_{TH0.4}$	Detection threshold 2	Max. R_a detection by source at $I_P = I_{P\text{-}1.5}$	0.35	0.40	0.45	V
$V_{TH0.66}$	Detection threshold 3	Min. $I_{P_1.5}$ detection by sink on R_d	0.61	0.66	0.70	V
$V_{TH0.8}$	Detection threshold 4	Max. R_a detection by source at $I_P = I_{P\text{-}3.0}$	0.75	0.80	0.85	V
$V_{TH1.23}$	Detection threshold 5	Min. $I_{P_3.0}$ detection by sink on R_d	1.16	1.23	1.31	V
$V_{TH1.6}$	Detection threshold 6	Max. R_d detection by source at $I_P = I_{P\text{-}USB}$ and $I_P = I_{P\text{-}1.5}$	1.50	1.60	1.65	V
$V_{TH2.6}$	Detection threshold 7	Max. R_d detection by source at $I_{P\text{-}3.0}$, max. CC voltage for connected sink	2.45	2.60	2.75	V
VCONN pin and power switches						
R_{VCONN}	V_{CONN} path resistance	I_{VCONN}= 0.2 A, -40 °C < T_A < +105 °C	0.25	0.5	0.975	Ω
I_{OCP}	Overcurrent protection	Programmable current limit threshold (from 100 mA to 600 mA by step of 50 mA)	85	100	125	mA
			300	350	400	
			550	600	650	
V_{OVP}	Overvoltage protection on CC output pins		5.9	6	6.1	V
V_{UVP}	Undervoltage protection on VCONN input pin	Low UVLO threshold	2.6	2.65	2.7	V
		High UVLO threshold (default)	4.6	4.65	4.8	
VDD pin monitoring (source power role)						
V_{DDOVLO}	Overvoltage lockout	OVLO threshold detection enabled, VDD pin supplied	5.8	6.0	6.2	V
V_{DDUVLO}	Undervoltage lockout	UVLO threshold detection enabled, VDD pin supplied	3.8	3.9	4.0	
VBUS_SENSE pin monitoring and driving						
V_{THUSB}	V_{BUS} presence threshold	V_{SYS} = 3.0 to 5.5 V	3.8	3.9	4.0	V
V_{TH0V}	V_{BUS} safe 0 V threshold (vSafe0V)	V_{SYS} = 3.0 to 5.5 V, The threshold is programmable from 0.6 V to 1.8 V. Default V_{THOV} = 0.6 V	0.5	0.6	0.7	
			0.8	0.9	1.0	
			1.1	1.2	1.3	
			1.7	1.8	1.9	

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
R_{DISUSB}	V_{BUS} discharge resistor		600	700	800	Ω
T_{DISUSB}	V_{BUS} discharge time to 0 V	The coefficient $T_{DISPARAM}$ is programmable by NVM default $T_{DISPARAM}$ = 6, T_{DISUSB} = 504 ms	70* $T_{DISPARAM}$	84* $T_{DISPARAM}$	100* $T_{DISPARAM}$	ms
$V_{MONUSBH}$	V_{BUS} monitoring high threshold voltage	Coefficient V_{SHUSBH} programmable by NVM from 1% to 15% of V_{BUS} by step of 1%, default $V_{MONUSBH}$ source/sink = V_{BUS}+10%		V_{BUS} +5% +V_{SHUSBH}		V
$V_{MONUSBL}$	V_{BUS} monitoring low threshold voltage	Coefficient V_{SHUSBL} programmable by NVM from 1% to 15% of V_{BUS} by step of 1%, default $V_{MONUSBL\ Source}$ = V_{BUS}-10% $V_{MONUSBL\ Sink}$ = V_{BUS}-20%		V_{BUS} -5%-V_{SHUSBL}		V
Digital input/output (SCL, SDA, ALERT#, RESET, ATTACH, A_B_SIDE, VBUS_VALID, DEBUG1, DEBUG2)						
V_{IH}	High level input voltage		1.2			V
V_{IL}	Low level input voltage				0.35	V
V_{OL}	Low level output voltage	Ioh = 3 mA			0.4	V
20 V open-drain outputs (VBUS_EN_SRC, VBUS_EN_SNK)						
V_{OL}	Low level output voltage	Ioh = 3 mA			0.4	V

9 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

9.1 QFN-24 EP - pitch 0.50 mm - (4 x 4 mm) package information

Figure 11. QFN-24 EP 4x4 mm package outline

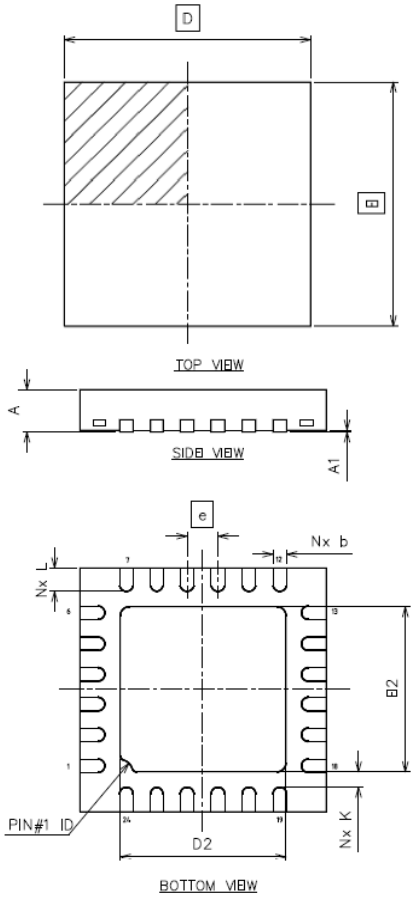
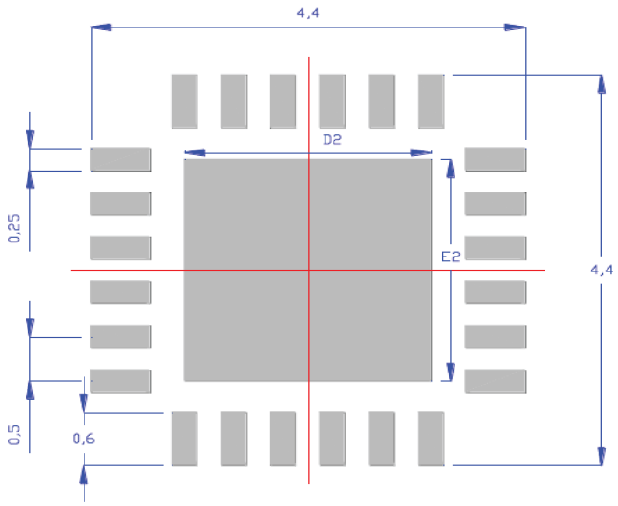


Table 50. **QFN24-EP 4x4 mm package mechanical data**

Symbol	mm			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.80	0.90	1.00	0.031	0.035	0.039
A1	0.00	0.02	0.05	0.000	0.001	0.002
b	0.18	0.25	0.30	0.007	0.010	0.012
D	3.95	4.00	4.05	0.156	0.157	0.159
D2	2.55	2.70	2.80	0.100	0.106	0.110
E	3.95	4.00	4.05	0.156	0.157	0.159
E2	2.55	2.70	2.80	0.100	0.106	0.110
e	0.45	0.50	0.55	0.018	0.020	0.022
K	0.15	-	-	0.006	-	-
L	0.30	0.40	0.50	0.0012	0.0016	0.020

Figure 12. **QFN24 EP 4x4 mm recommended footprint**



9.2 Thermal information

Table 51. **Thermal information**

Symbol	Parameter	Value	Unit
$R_{\theta JA}$	Junction-to-ambient thermal resistance	37	°C/W
$R_{\theta JC}$	Junction-to-case thermal resistance	5	°C/W

10 Terms and abbreviations

Table 52. List of terms and abbreviations

Term	Description
Accessory modes	Audio adapter accessory mode. It is defined by the presence of Ra/Ra on CC1/CC2 pins. Debug accessory mode. It is defined by the presence of Rd/Rd on CC1/CC2 pins in source power role or Rp/Rp on CC1/CC2 pins in sink power role
DFP	Downstream facing port, specifically associated with the flow of data in a USB connection. Typically the ports on a host or the ports on a hub to which devices are connected. In its initial state, the DFP sources V_{BUS} and V_{CONN}, and supports data
DRP	Dual-role port. A port that can operate as either a source or a sink. The port role may be changed dynamically
Sink	Port asserting Rd on CC pins and consuming power from V_{BUS}; most commonly a device
Source	Port asserting Rp on CC pins and providing power over V_{BUS}; most commonly a host or hub DFP
UFP	Upstream facing port, specifically associated with the flow of data in a USB connection. The port on a device or a hub that connects to a host or the DFP of a hub. In its initial state, the UFP sinks V_{BUS} and supports data

11 Ordering information

Table 53. **Ordering information**

Order code	USB Type-C	R_p default	Package	Marking
STUSB1600AQTR	Rev1.2+ECN	1.5 A	QFN24 EP 4x4 mm	1600A

Revision history

Table 54. **Document revision history**

Date	Revision	Changes
30-Nov-2016	1	Initial release.
05-Sep-2017	2	Updated: title, features, description and Table 1 in cover page. Updated Table 17, Table 20, Table 27, Table 31, Table 32, Table 35, Table 37, Table 38, Table 41, Table 44, Table 48 and Table 49. Updated Section 3.2.3, Section 5.1.4, Section 5.1.6, Section 5.1.12, Section 5.1.13, Section 5.1.19.
22-Jun-2018	3	Updated: title, features, description and Table 1 in cover page. Updated Table 26. CC_CAPABILITY_CTRL register, Table 31. VBUS_DISCHARGE_TIME_CTRL register, Table 36. STUSB1600 user-defined parameters and default settings, Table 37. Default setting for a source type application, Table 40. Default setting for a sink type application, Table 43. Default setting for a dual role type application and Table 49. Electrical characteristics. Minor text changes.
10-Oct-2019	4	Updated Section 7.1.2 Connection to MCU or application processor and Table 49. Electrical characteristics.

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