

Product data sheet

1. Product profile

1.1 General description

Passivated sensitive gate thyristor in a SOT54 plastic package.

1.2 Features

 Designed to be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits

1.3 Applications

General purpose switching and phase control

1.4 Quick reference data

- V_{DRM} ≤ 400 V
- $V_{RRM} \le 400 \text{ V}$
- $I_{TSM} \le 8 A$

- $I_{T(RMS)} \le 0.8 A$
- $I_{T(AV)} \le 0.5 A$
- I_{GT} \leq 50 μ A

2. Pinning information

Table 1. Pinning

	•		
Pin	Description	Simplified outline	Symbol
1	anode (A)		
2	gate (G)		A → K
3	cathode (K)		G <i>sym037</i>
		SOT54 (TO-92)	



3. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
BT169D-L	TO-92	plastic single-ended leaded (through hole) package; 3 leads	SOT54

4. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DRM}	repetitive peak off-state voltage		<u>[1]</u> _	400	V
V_{RRM}	repetitive peak reverse voltage		<u>[1]</u> _	400	V
$I_{T(AV)}$	average on-state current	half sine wave; $T_{lead} \le 83 ^{\circ}C$; see Figure 1	-	0.5	A
$I_{T(RMS)}$	RMS on-state current	all conduction angles; see Figure 4 and $\underline{5}$	-	0.8	Α
I _{TSM}	non-repetitive peak on-state current	half sine wave; $T_j = 25$ °C prior to surge; see Figure 2 and 3			
		t = 10 ms	-	8	Α
		t = 8.3 ms	-	9	Α
I ² t	I ² t for fusing	t = 10 ms	-	0.32	A ² s
dl _T /dt	rate of rise of on-state current	I_{TM} = 2 A; I_G = 10 mA; dI_G/dt = 100 mA/ μ s	-	50	A/μs
I _{GM}	peak gate current		-	1	Α
V_{GM}	peak gate voltage		-	5	V
V_{RGM}	peak reverse gate voltage		-	5	V
P_{GM}	peak gate power		-	2	W
$P_{G(AV)}$	average gate power	over any 20 ms period	-	0.1	W
T _{stg}	storage temperature		-40	+150	°C
Tj	junction temperature		-	125	°C

^[1] Although not recommended, off-state voltages up to 800 V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 15 A/µs.

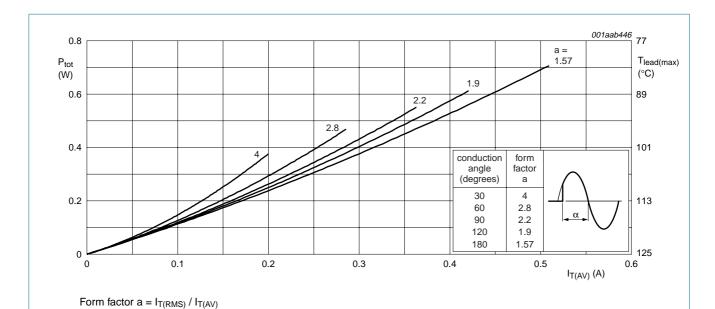
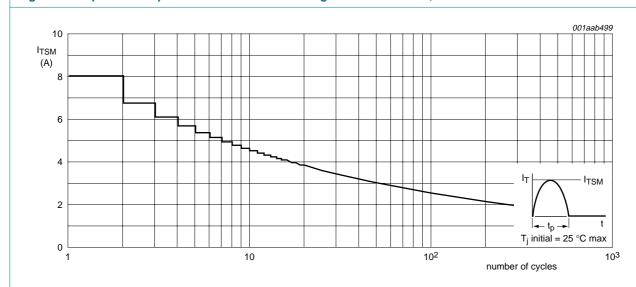


Fig 1. Total power dissipation as a function of average on-state current; maximum values



f = 50 Hz

Fig 2. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values

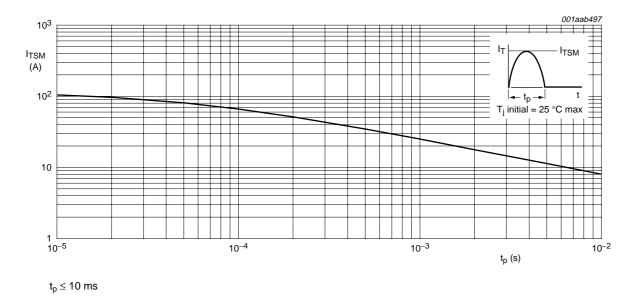


Fig 3. Non-repetitive peak on-state current as a function of pulse width for sinusoidal currents; maximum values

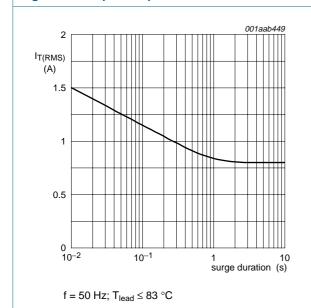
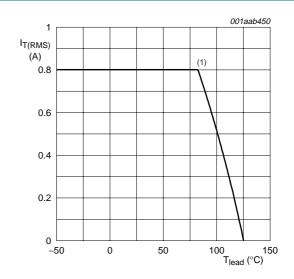


Fig 4. RMS on-state current as a function of surge duration for sinusoidal currents



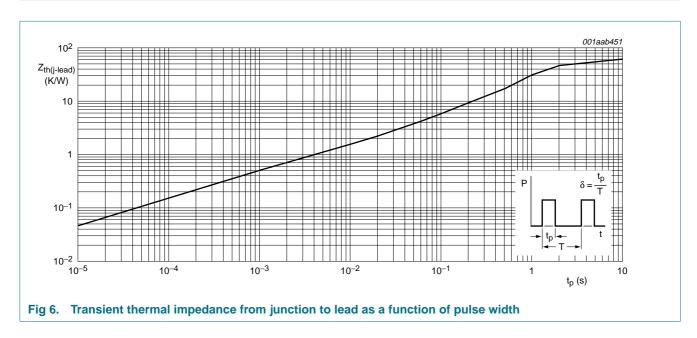
(1) $T_{lead} = 83 \, ^{\circ}C$

Fig 5. RMS on-state current as a function of lead temperature; maximum values

5. Thermal characteristics

Table 4. Thermal characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$R_{th(j\text{-lead})}$	thermal resistance from junction to lead	see Figure 6	-	-	60	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	Printed-circuit board mounted; lead length = 4 mm	-	150	-	K/W



6. Characteristics

Table 5. Characteristics

 $T_j = 25$ °C unless otherwise stated.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static char	racteristics					
I _{GT}	gate trigger current	$V_D = 12 \text{ V}; I_T = 10 \text{ mA};$ gate open circuit; see Figure 8	-	-	50	μΑ
IL	latching current	V_D = 12 V; I_{GT} = 0.5 mA; R_{GK} = 1 k Ω ; see Figure 10	-	2	6	mA
l _H	holding current	V_D = 12 V; I_{GT} = 0.5 mA; R_{GK} = 1 k Ω ; see Figure 11	-	2	5	mA
V_{T}	on-state voltage	I _T = 1.2 A	-	1.25	1.7	V
V_{GT}	gate trigger voltage	I _T = 10 mA; gate open circuit; see Figure 7				
		V _D = 12 V	-	0.5	8.0	V
		$V_D = V_{DRM(max)}$; $T_j = 125 ^{\circ}C$	0.2	0.3	-	V
I _D	off-state current	$V_D = V_{DRM(max)}$; $T_j = 125$ °C; $R_{GK} = 1 \text{ k}\Omega$	-	0.05	0.1	mA
Dynamic c	haracteristics					
dV _D /dt	rate of rise of off-state voltage	$V_{DM} = 0.67 \times V_{DRM(max)}$; $T_j = 125$ °C; exponential waveform; see Figure 12				
		$R_{GK} = 1 k\Omega$	500	800	-	V/μs
		gate open circuit	-	25	-	V/μs
t _{gt}	gate-controlled turn-on time	$I_{TM} = 2 \text{ A}; \ V_D = V_{DRM(max)}; \ I_G = 10 \text{ mA}; \\ dI_G/dt = 0.1 \text{ A}/\mu s$	-	2	-	μs
t _q	commutated turn-off time	$\begin{split} &V_{DM}=0.67\times V_{DRM(max)};T_{j}=125~^{\circ}C;\\ &I_{TM}=1.6~A;V_{R}=35~V;\\ &(dI_{T}/dt)_{M}=30~A/\mu s;dV_{D}/dt=2~V/\mu s;\\ &R_{GK}=1~k\Omega \end{split}$	-	100	-	μs

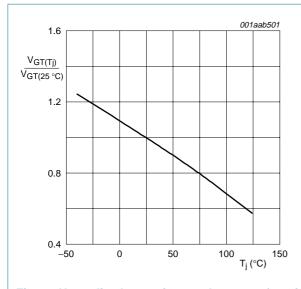


Fig 7. Normalized gate trigger voltage as a function of junction temperature

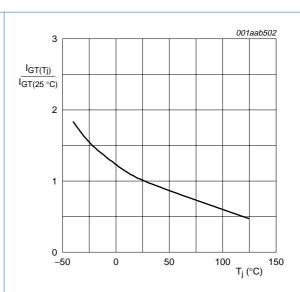
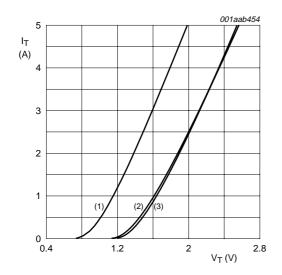


Fig 8. Normalized gate trigger current as a function of junction temperature

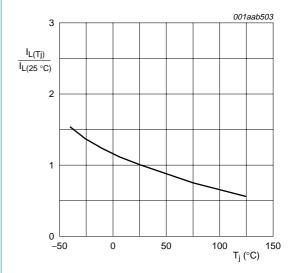


 $V_0 = 1.067 \text{ V}$

 $R_s = 0.187 \Omega$

- (1) $T_j = 125 \,^{\circ}C$; typical values
- (2) $T_j = 125$ °C; maximum values
- (3) $T_j = 25$ °C; maximum values

Fig 9. On-state current as a function of on-state voltage

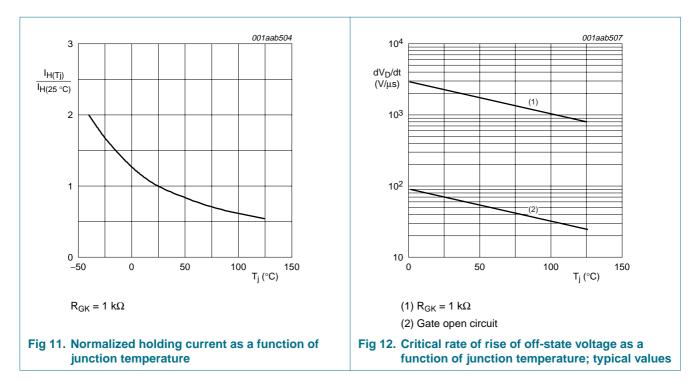


 $R_{GK} = 1 k\Omega$

Fig 10. Normalized latching current as a function of junction temperature

 NXP Semiconductors BT169D-L

Thyristor, logic level



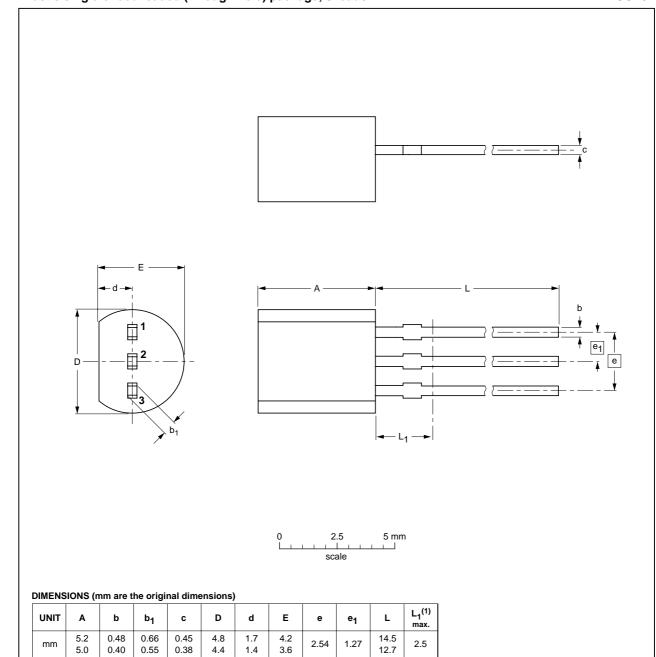
7. Package information

Epoxy meets requirements of UL 94 V-0 at 3.175 mm

8. Package outline

Plastic single-ended leaded (through hole) package; 3 leads

SOT54



Note

1. Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

OUTLINE		REFER	ENCES	EUROPEAN	ISSUE DATE
VERSION	IEC	JEDEC	JEITA	PROJECTION	ISSUE DATE
SOT54		TO-92	SC-43A		-04-06-28- 04-11-16

Fig 13. Package outline SOT54 (TO-92)



9. Revision history

Table 6. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BT169D-L_1	20071112	Product data sheet	-	-

10. Legal information

10.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions"
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