

Wireless Audio Link IC

BH1414K

The BH1414K is a FM stereo transmitter IC that uses a simple configuration. This IC consists of a stereo modulator for generating stereo composite signals and a FM transmitter for broadcasting a FM signal on the air. A high S/N ratio and good timbre transmitter circuit can be composed with a few components. It is available for many applications due to the varieties of setting such as transmission output by serial data input.

●Applications

CD changer, Car TV, Car navigation, Wireless speakers, Personal computer (sound board), Game machine

●Features

- 1) It is possible to improve the timbre because it has the pre-emphasis circuit, limiter circuit, and the 19kHz/38kHz low-pass trap filter circuit.
- 2) Built-in pilot-tone system FM stereo modulator circuit.
- 3) The transmission frequency is stable because it has a PLL system for the FM transmitter circuit.
- 4) PLL data input (CE, CK, DA) by serial input.
- 5) It is possible for input level setting, monaural operation and output ON/OFF control by serial input.
- 6) It is possible for the transmission output control.

●Absolute maximum ratings (Ta = 25°C)

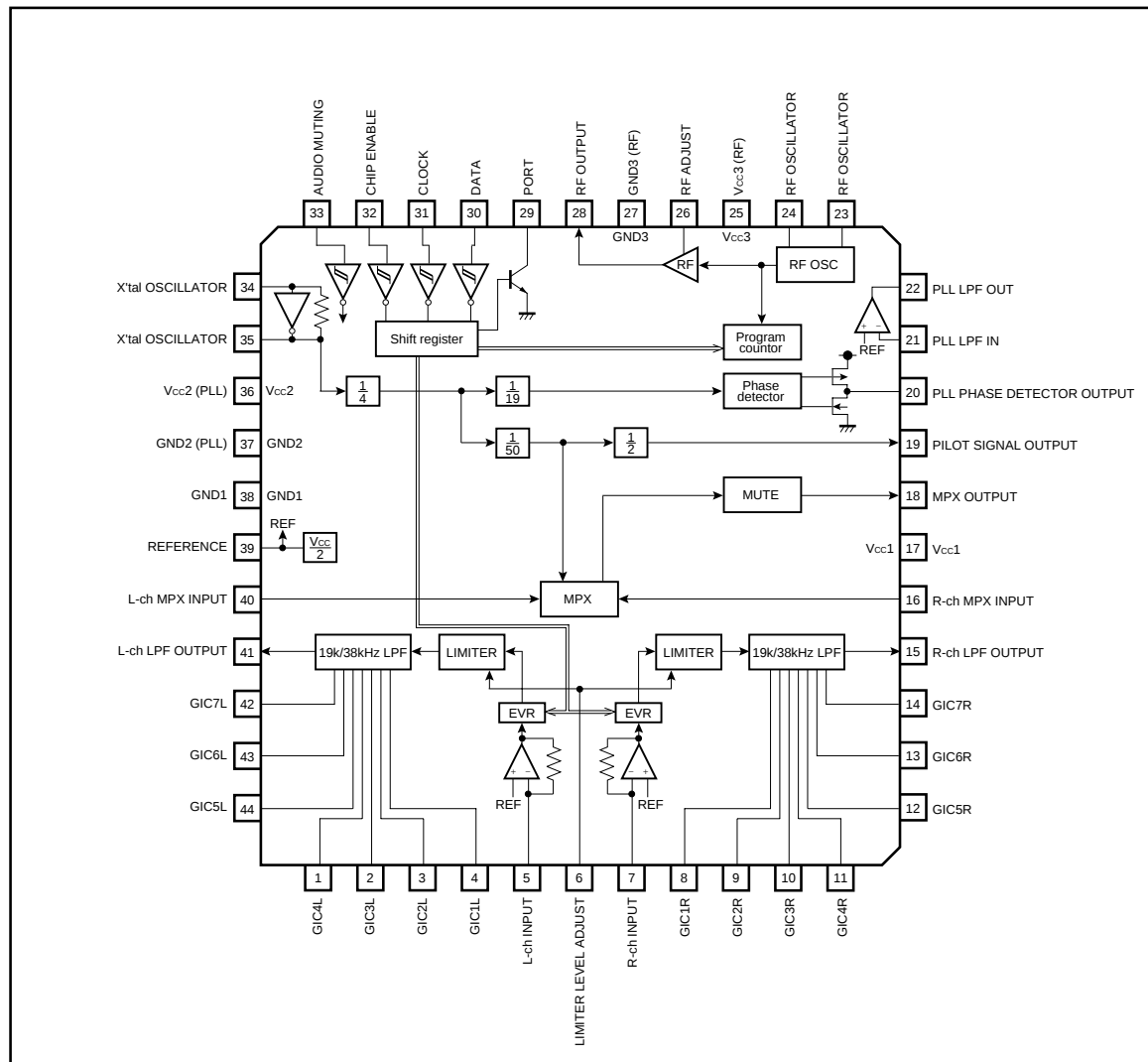
Parameter	Symbol	Limits	Unit
Supply voltage	V _{CC1}	+9.0	V
	V _{CC2}	+10.0	
Power dissipation	P _d	500	mW
Storage temperature range	T _{stg}	-55~+125	°C

* Reduced by 5mW for each increase in Ta of 1°C over 25°C.

●Recommended operating conditions (Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Operating supply voltage	V _{CC}	4.5	—	5.5	V
Operating temperature range	T _{opr}	-40	—	+85	°C
Audio input level	V _{IN-A}	—	—	500	mVrms
Audio input frequency	f _{IN-A}	20	—	15k	Hz
Transmission frequency	f _{TX}	75	—	110	MHz

●Block diagram



Multimedia ICs

●Pin descriptions

Pin No.	Pin name	Equivalent circuit	Description	DC voltage (V)
1 2 3 4 42 43 44	L-ch LPF time constant terminal		It connects resistor and capacitor.	$\frac{1}{2} V_{CC}$
8 9 10 11 12 13 14	R-ch LPF time constant terminal		It connects resistor and capacitor.	
15	R-ch LPF output and LPF time constant terminal			
41	L-ch LPF output and LPF time constant terminal			
5	L-ch audio source input terminal		It cuts DC with the capacitor and it inputs L-ch audio signal.	$\frac{1}{2} V_{CC}$
7	R-ch audio source input terminal		It cuts DC with the capacitor and it inputs R-ch audio signal.	
6	Limiter level adjust terminal		It adjusts a limiter level by the resistance.	$\frac{1}{2} V_{CC}$

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Pin No.	Pin name	Equivalent circuit	Description	DC voltage (V)
16	R-ch MPX input terminal			$\frac{1}{2} V_{CC}$
40	L-ch MPX input terminal			
17	Power supply 1 terminal	—		V_{CC}
18	MPX signal output terminal		It connects to the FM modulator.	$\frac{1}{2} V_{CC} - 0.7$
19	Pilot signal output terminal		It connects to the FM modulator.	$\frac{1}{2} V_{CC} - 0.7$
20	PLL phase detector output terminal		It connects to the PLL LPF circuit.	—
21	PLL LPF input terminal			—
22	PLL LPF output terminal			

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Pin No.	Pin name	Equivalent circuit	Description	DC voltage (V)
23	RF oscillator terminal		This is the colpitts oscillator. It connects time constant of the oscillation.	$\frac{5}{9} V_{CC}$
24				$\frac{5}{9} V_{CC} - 0.7$
25	Power supply 3 terminal (RF)	—		V_{CC}
26	RF adjust terminal		It connects resistor and capacitor.	$\frac{3}{4} V_{CC} - 0.9$
28	RF transmission output terminal		It connects LC.	V_{CC}
27	GND3 (RF)	—		GND
29	Port output terminal			—
30	Data input terminal		The input terminal of the serial data which is forwarded from the controller.	—
31	Clock input terminal		The clock which takes data and synchronization in serial data input.	
32	Chip enable terminal		The terminal to make high level in serial data input.	
33	Audio mute terminal		$0.8V_{CC2} \leq \text{Pin33}$: Mute OFF $0.2V_{CC2} \geq \text{Pin33}$: Mute ON	

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Pin No.	Pin name	Equivalent circuit	Description	DC voltage (V)
34 35	X'tal oscillator terminal		It connects a 7.6MHz crystal oscillator.	—
36	Power supply 2 terminal (PLL)	—		V _{CC}
37	GND2 (PLL)	—		GND
38	GND1	—		GND
39	Reference voltage terminal		It is a ripple filter for the reference voltage.	$\frac{1}{2} V_{CC}$

Multimedia ICs

●Electrical characteristics (Unless otherwise noted, Ta = 25°C, V_{CC}=5.0V, Signal source : f_{IN}=400Hz)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	Measurement circuit
Quiescent current	I _Q	15	21	29	mA		Fig.1
Channel separation	Sep	30	45	—	dB	V _{IN} =125mVrms, L→R, R→L	Fig.2
Total harmonic distortion	THD	—	0.1	0.3	%	V _{IN} =125mVrms, L+R	Fig.3
Channel balance	C.B	-1.5	0	+1.5	dB	V _{IN} =125mVrms, L+R	Fig.2
Input output gain 1	G _{V1}	-4	-2	0	dB	V _{IN} =125mVrms, EVR=0dB, L+R	Fig.3
Input output gain 2	G _{V2}	+2	+4	+6	dB	V _{IN} =125mVrms, EVR=+6dB, L+R	Fig.3
Input output gain 3	G _{V3}	-10	-8	-6	dB	V _{IN} =125mVrms, EVR=-6dB, L+R	Fig.3
Limiter input level	V _{IN(LIM)}	205	260	325	mVrms	Output distortion at 3% for input level	Fig.4
LPF attenuation volume 1	V _{O(LPF)1}	-2	0.5	+1.5	dB	V _{IN} =125mVrms, f=10kHz	Fig.5
LPF attenuation volume 2	V _{O(LPF)2}	—	-37	-30	dB	V _{IN} =125mVrms, f=19kHz	Fig.5
LPF attenuation volume 3	V _{O(LPF)3}	—	-49	-35	dB	V _{IN} =125mVrms, f=38kHz	Fig.5
Signal to noise ratio	S/N	55	68	—	dB	V _{IN} =125mVrms, L+R	Fig.3
Sub carrier rejection ratio	SCR	—	-30	-20	dB	V _{IN} =125mVrms, L+R	Fig.3
Pilot output level	V _{OP}	180	200	220	mV _{P-P}	Pin19	Fig.3
Mute attenuation volume	V _{O(MUTE)}	—	-68	-60	dB	V _{IN} =125mVrms, L+R	Fig.6
Transmission output level	V _{TX}	84	87	90	dBμV	f _{TX} =100MHz	Fig.7
Transmission frequency precision	Δf _{TX}	-3	0	+3	kHz	f _{TX} =100MHz	Fig.7
"H" level input current	I _{IH}	—	—	1.0	μA	Pin30, 31, 32, 33 V _{IN} =5V	Fig.8
"L" level input current	I _{IL}	-1.0	—	—	μA	Pin30, 31, 32, 33 V _{IN} =0V	Fig.8
"H" level output voltage	V _{OH}	V _{CC} -1.0	V _{CC} -0.3	—	V	Pin20 I _{OUT} =-1.0mA	Fig.8
"L" level output voltage	V _{OL}	—	0.3	1.0	V	Pin20 I _{OUT} =1.0mA	Fig.8
"OFF" level leak current 1	I _{OFF1}	—	—	100	nA	Pin20 V _{OUT} =5V	Fig.9
"OFF" level leak current 2	I _{OFF2}	-100	—	—	nA	Pin20 V _{OUT} =GND	Fig.9
"L" level output voltage	V _{OL}	—	0.2	1.0	V	Pin29 I _{OUT} =3.0mA	Fig.8
"OFF" level leak current	I _{OFF}	—	—	1.0	μA	Pin29 V _{OUT} =5V	Fig.9

© This product is not designed for protection against radioactive rays.

© The specification of transmission output level be based on the Radio Law in every country and the area.

Quiescent current

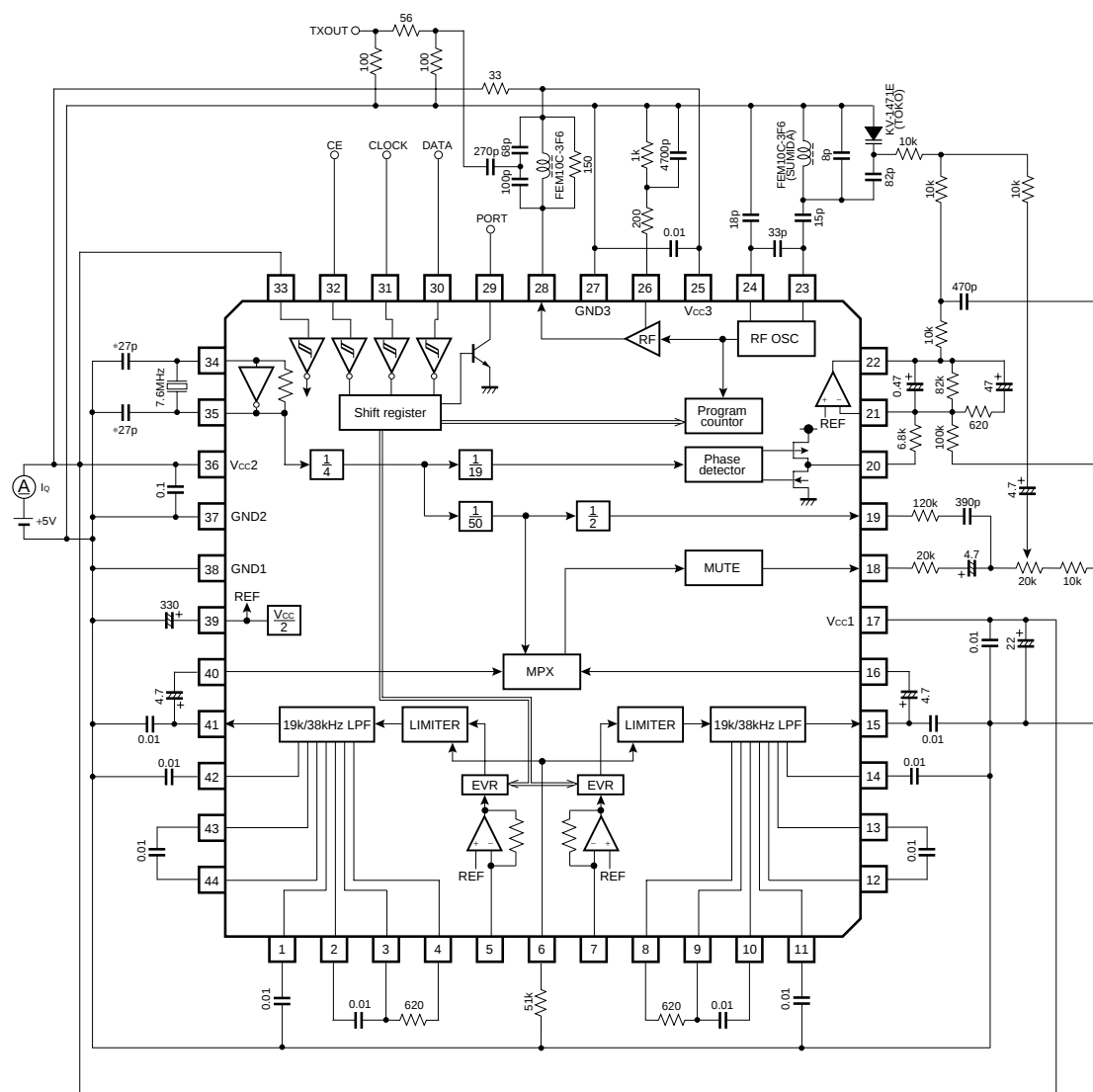


Fig.1

*The constant of the capacitor must be determined by the agreement with a crystal maker.

The diagram illustrates a PLL-based FM receiver IC with the following components and connections:

- Power Supply:** A +5V supply is connected to pins 36 (Vcc2), 38 (GND2), 39 (REF), and 40 (Vcc1). Pin 37 is GND1.
- Control Signals:** GE (pin 32), CLOCK (pin 31), DATA (pin 30), and PORT (pin 29) are shown as inputs.
- Internal Blocks:** The IC contains a Shift register, Program counter, Phase detector, MUTE, MPX, two 19k/38kHz LPF filters, two LIMITER stages, two EVR (Envelope Voltage Regulator) blocks, and an RF OSC (Radio Frequency Oscillator).
- External Components:**
 - Capacitors:** Various values are used throughout, including 27pF, 7.6MHz, 0.1, 330, 4.7, 0.01, 0.001, 1000pF, and 390pF.
 - Resistors:** Values include 33, 27, 26, 25, 24, 23, 22, 21, 20, 19, 18, 17, 16, 15, 14, 13, 12, 11, 10, 9, 8, 7, 6, 5, 4, 3, 2, 1, 0.01, 0.001, 0.1, 1, 10k, 51k, 620, 120k, 20k, and 10k.
- Output Stage:** The stereo signal demodulator outputs L-ch and R-ch signals, which are filtered by 10k resistors and 0.01 capacitors before being sent to the output terminals.
- Frequency and Amplitude:** The input frequency is specified as $f_{IN}=400\text{Hz}$ and the input voltage as $V_{IN}=125\text{mVrms}$.

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Total harmonic distortion
 Input output gain
 Signal to noise ratio
 Sub carrier rejection ratio
 Pilot output level

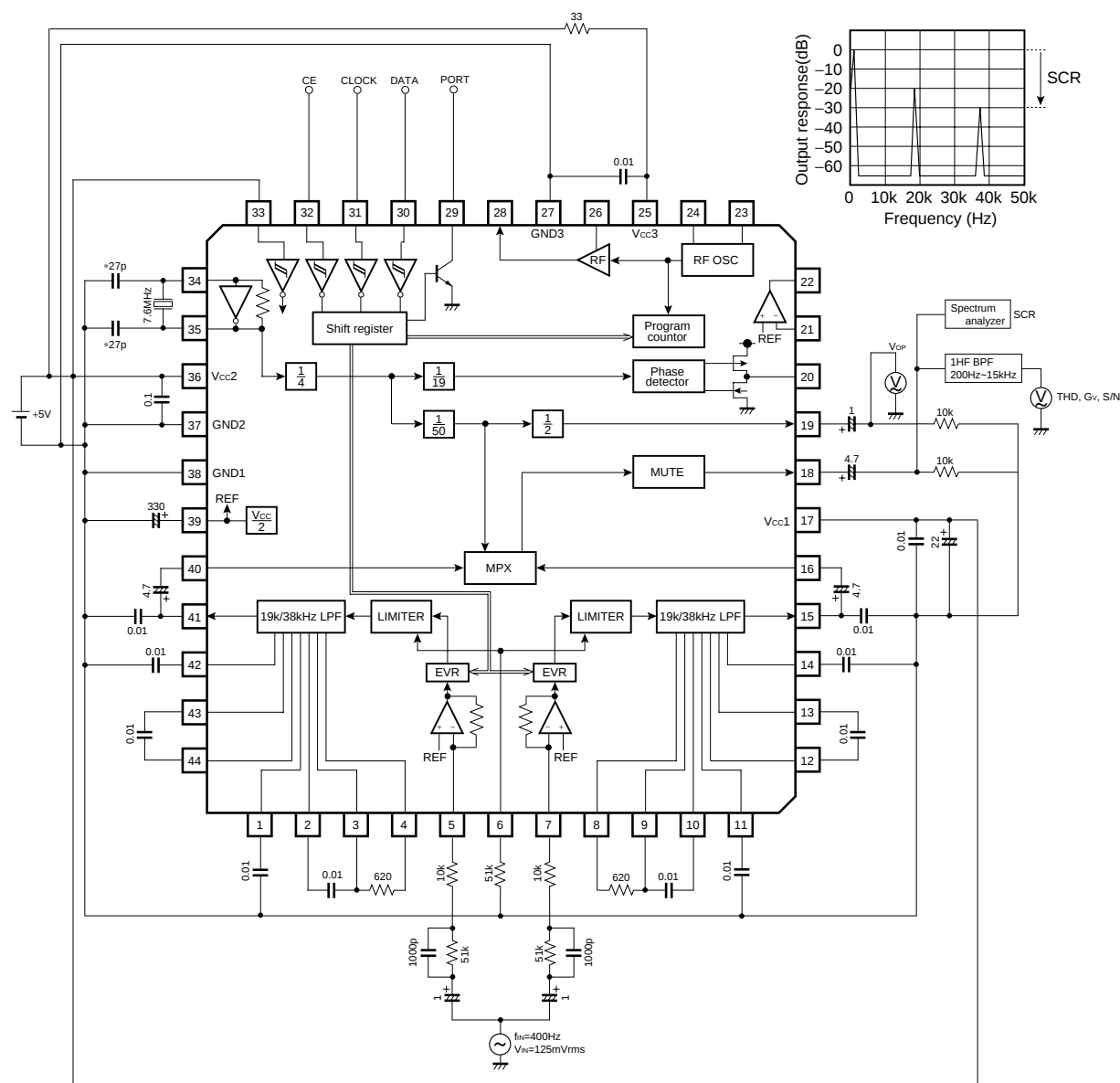


Fig.3

* The constant of the capacitor must be determined by the agreement with a crystal maker.

Fig.4

*The constant of the capacitor must be determined by the agreement with a crystal maker.

LPF attenuation volume

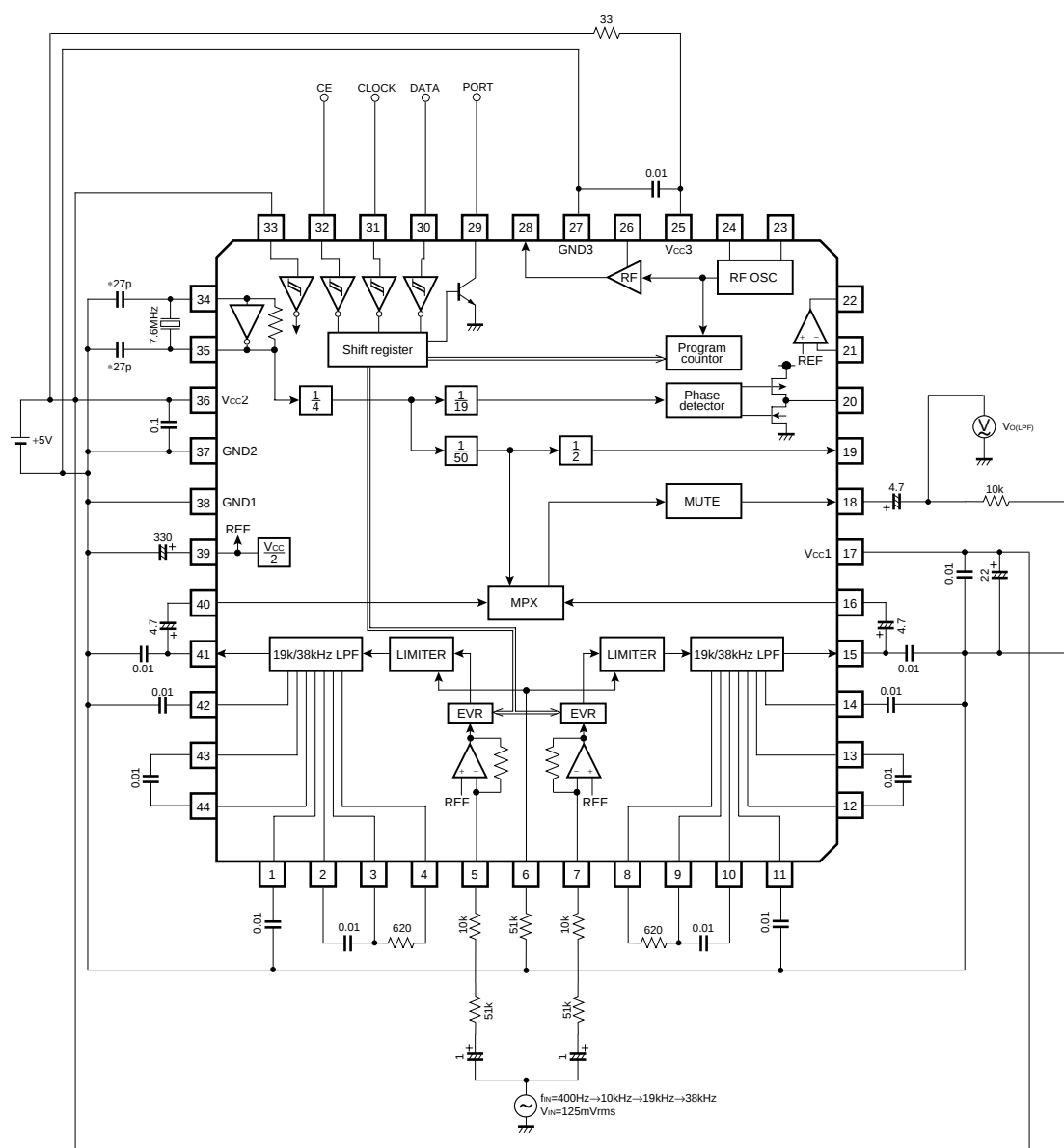


Fig.5

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Transmission frequency precision

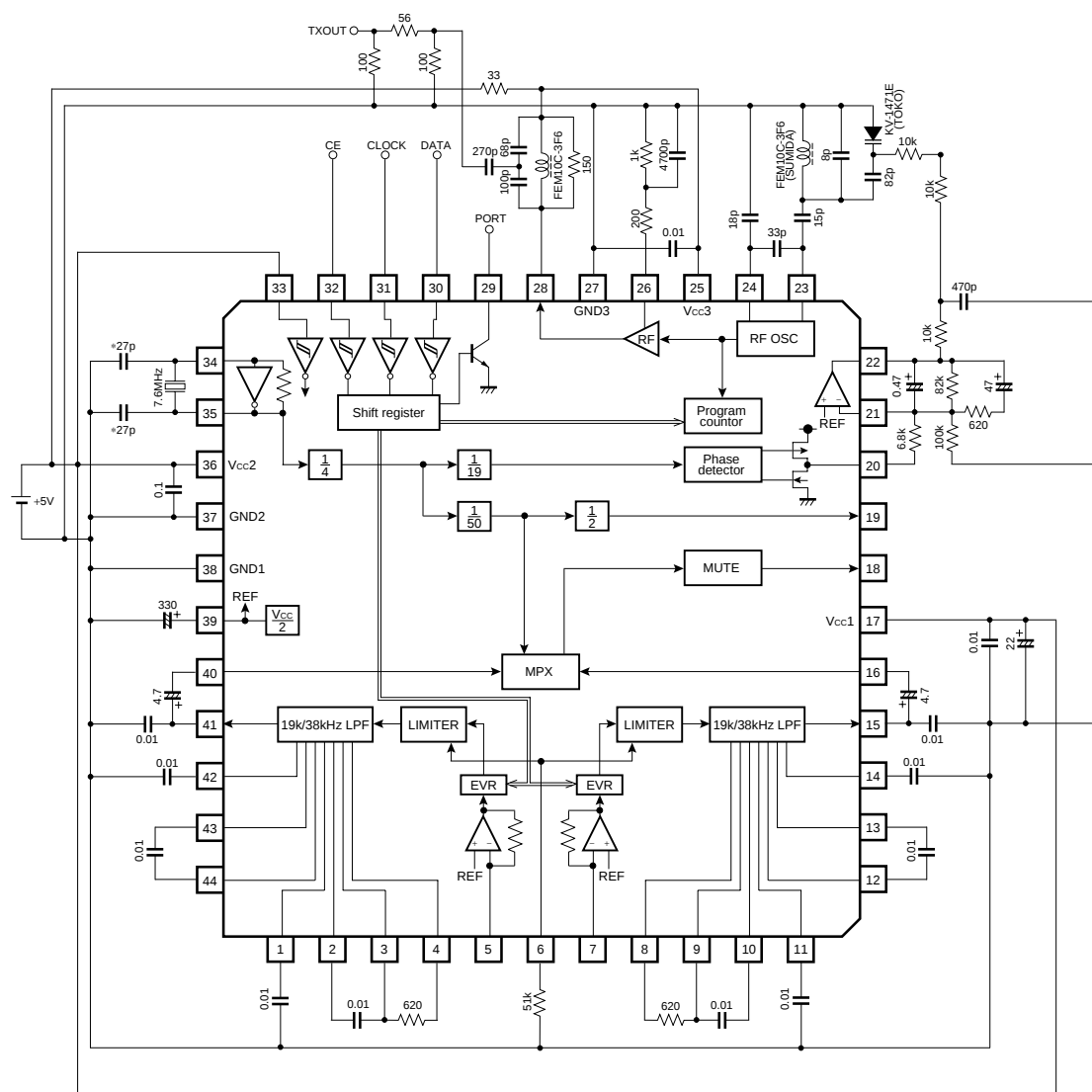


Fig.7

*The constant of the capacitor must be determined by the agreement with a crystal maker.

“L” level output voltage



*The constant of the capacitor must be determined by the agreement with a crystal maker.

“OFF” level leak current

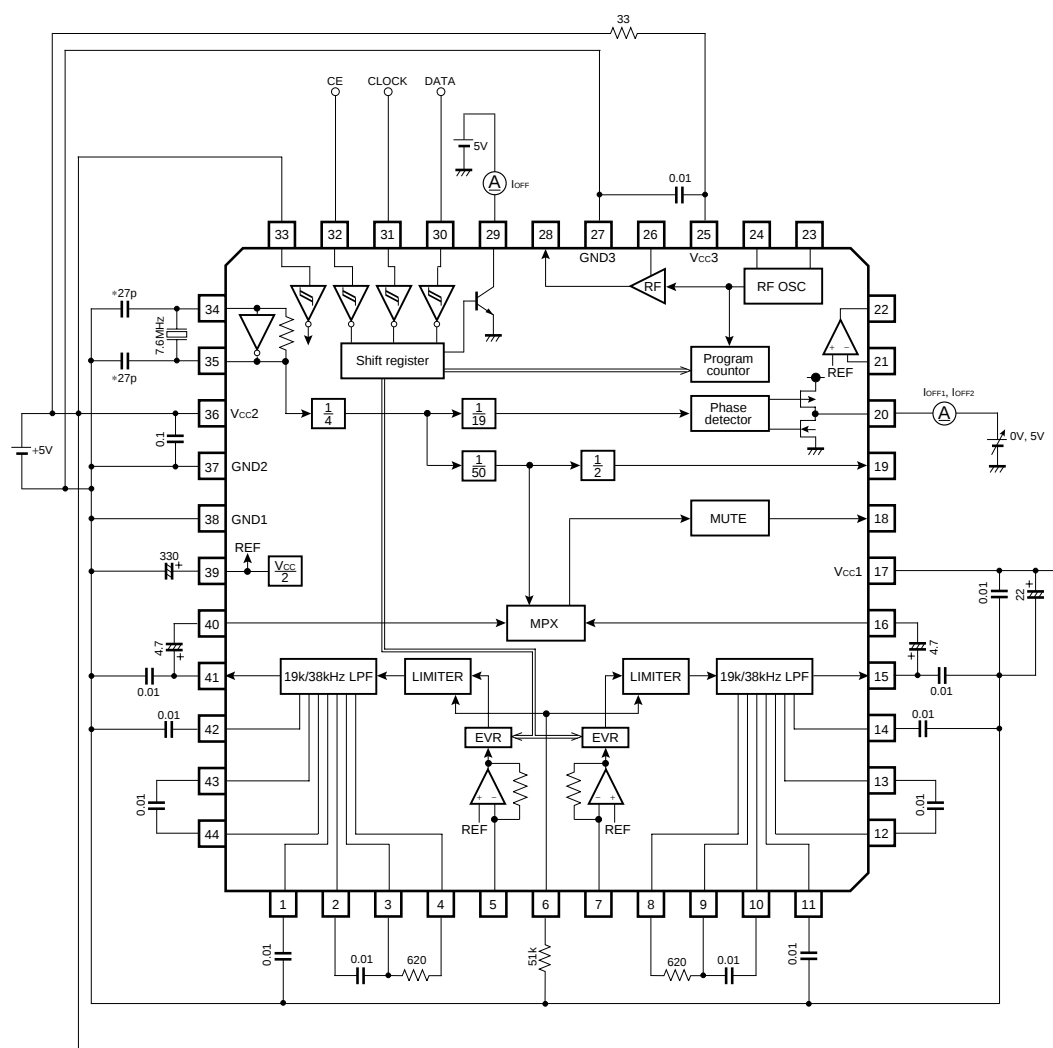


Fig.9

* The constant of the capacitor must be determined by the agreement with a crystal maker.

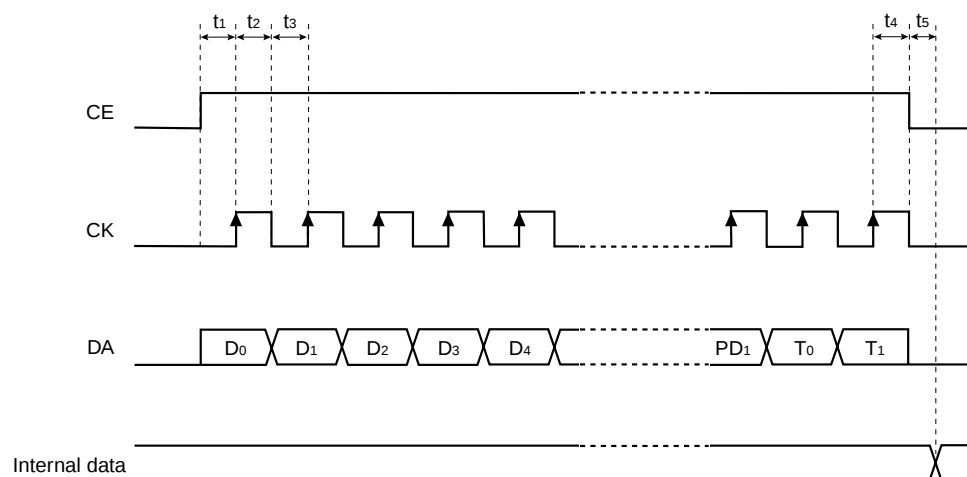
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●Circuit operations

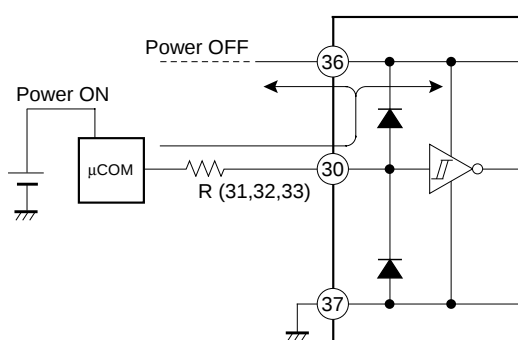
(1) Input of the serial data

$$t_1, t_2, t_3, t_4 \geq 1.5\mu\text{sec}$$

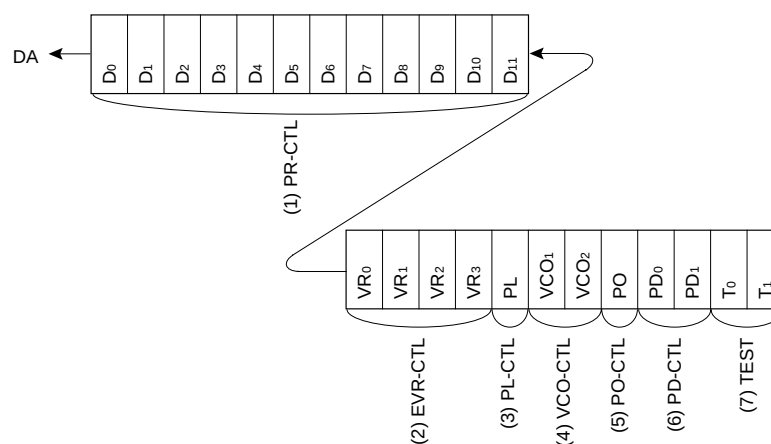
$$t_5 < 1.5\mu\text{sec} (X'tal : 7.6\text{MHz})$$



When the serial data input terminal (Pin 30, Pin 31, Pin 32) and the mute control terminal (Pin 33) connect with the μ -com, in off the power of BH1414K and on the power of μ -com, because the current flows backward from the μ -com to BH1414K, insert limitation resistance between the serial data input terminal and the data output terminal of μ -com. But, when the data output by μ -com doesn't always maintain at the "H" voltage, that matter may be left out of consideration.



(2) Composition of the serial data



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(3) Explanation of the serial data

No.	Control unit	Contents																																																																																					
(1)	PROGRAM COUNTER D ₀ ~D ₁₁	· It is the data which sets the program counter number of the dividing. This data can set a transmission frequency. · It is a binary value. It sets D₁₁ With MSB and it sets D₀ with LSB. Example In case of 99.7MHz oscillation 99.7MHz÷100kHz(fref)=997→3E5(HEX) <table><tr><td colspan="4">5</td><td colspan="4">E</td><td colspan="4">3</td></tr><tr><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td></tr><tr><td>D₀</td><td>D₁</td><td>D₂</td><td>D₃</td><td>D₄</td><td>D₅</td><td>D₆</td><td>D₇</td><td>D₈</td><td>D₉</td><td>D₁₀</td><td>D₁₁</td></tr></table> LSBMSB	5				E				3				1	0	1	0	0	1	1	1	1	1	0	0	D ₀	D ₁	D ₂	D ₃	D ₄	D ₅	D ₆	D ₇	D ₈	D ₉	D ₁₀	D ₁₁																																																	
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D ₀	D ₁	D ₂	D ₃	D ₄	D ₅	D ₆	D ₇	D ₈	D ₉	D ₁₀	D ₁₁																																																																												
(2)	EVR VR ₀ ~VR ₃	· It controls EVR. L-ch and R-ch are set at the same time. <table><tr><th>VR₀</th><th>VR₁</th><th>VR₂</th><th>VR₃</th><th>EVR GAIN</th></tr><tr><td>0</td><td>1</td><td>1</td><td>1</td><td>-6</td></tr><tr><td>0</td><td>1</td><td>1</td><td>0</td><td>-6</td></tr><tr><td>0</td><td>1</td><td>0</td><td>1</td><td>-5</td></tr><tr><td>0</td><td>1</td><td>0</td><td>0</td><td>-4</td></tr><tr><td>0</td><td>0</td><td>1</td><td>1</td><td>-3</td></tr><tr><td>0</td><td>0</td><td>1</td><td>0</td><td>-2</td></tr><tr><td>0</td><td>0</td><td>0</td><td>1</td><td>-1</td></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr><tr><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td></tr><tr><td>1</td><td>0</td><td>0</td><td>1</td><td>+1</td></tr><tr><td>1</td><td>0</td><td>1</td><td>0</td><td>+2</td></tr><tr><td>1</td><td>0</td><td>1</td><td>1</td><td>+3</td></tr><tr><td>1</td><td>1</td><td>0</td><td>0</td><td>+4</td></tr><tr><td>1</td><td>1</td><td>0</td><td>1</td><td>+5</td></tr><tr><td>1</td><td>1</td><td>1</td><td>0</td><td>+6</td></tr><tr><td>1</td><td>1</td><td>1</td><td>1</td><td>+6</td></tr></table>	VR ₀	VR ₁	VR ₂	VR ₃	EVR GAIN	0	1	1	1	-6	0	1	1	0	-6	0	1	0	1	-5	0	1	0	0	-4	0	0	1	1	-3	0	0	1	0	-2	0	0	0	1	-1	0	0	0	0	0	1	0	0	0	0	1	0	0	1	+1	1	0	1	0	+2	1	0	1	1	+3	1	1	0	0	+4	1	1	0	1	+5	1	1	1	0	+6	1	1	1	1	+6
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(3)	MULTIPLEXER PL	· It changes a stereo and monaural operation. <table><tr><th>PL</th><th colspan="2">Condition of the composite signal</th></tr><tr><td>0</td><td>Stereo operation</td><td>L+R+ (L-R) sin ω_{st}+P sin $\frac{\omega_s}{2}$ t</td></tr><tr><td>1</td><td>Monaural operation</td><td>L+R, Pilot OFF</td></tr></table>	PL	Condition of the composite signal		0	Stereo operation	L+R+ (L-R) sin ω _{st} +P sin $\frac{\omega_s}{2}$ t	1	Monaural operation	L+R, Pilot OFF																																																																												
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(4)	VCO VCO ₁ , VCO ₂	· It controls the VCO operation. <table><tr><th>VCO₁</th><th>VCO₂</th><th>VCO</th></tr><tr><td>0</td><td>0 or 1</td><td>Enable</td></tr><tr><td>1</td><td>0 or 1</td><td>Disable</td></tr></table>	VCO ₁	VCO ₂	VCO	0	0 or 1	Enable	1	0 or 1	Disable																																																																												
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(5)	PORT(Pin29) PO	· It controls open collector output. <table><tr><th>PO</th><th>Open collector output</th></tr><tr><td>0</td><td>High impedance</td></tr><tr><td>1</td><td>Low (ON)</td></tr></table>	PO	Open collector output	0	High impedance	1	Low (ON)																																																																															
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(6)	PHASE DETECTOR PD ₀ , PD ₁	· It controls change pump output by the phase comparator compulsorily. <table><tr><th>PD₀</th><th>PD₁</th><th>Charge pump output</th></tr><tr><td>0</td><td>0</td><td>Usual operation</td></tr><tr><td>0</td><td>1</td><td>Compulsion by Low</td></tr><tr><td>1</td><td>0</td><td>Compulsion by High</td></tr><tr><td>1</td><td>1</td><td>High impedance</td></tr></table>	PD ₀	PD ₁	Charge pump output	0	0	Usual operation	0	1	Compulsion by Low	1	0	Compulsion by High	1	1	High impedance																																																																						
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(7)	TEST MODE T ₀ , T ₁	· It is data for the LSI test. · Always Input "00".																																																																																					

Fig.10

*The constant of the capacitor must be determined by the agreement with a crystal maker.

Multimedia ICs

●External dimensions (Units : mm)

