

SN54F109, SN74F109  
DUAL J- $\bar{K}$  POSITIVE-EDGE-TRIGGERED FLIP-FLOPS  
WITH CLEAR AND PRESET

SDF047A – MARCH 1987 – REVISED OCTOBER 1993

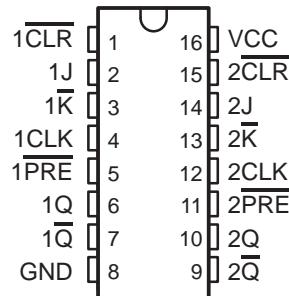
- Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

### description

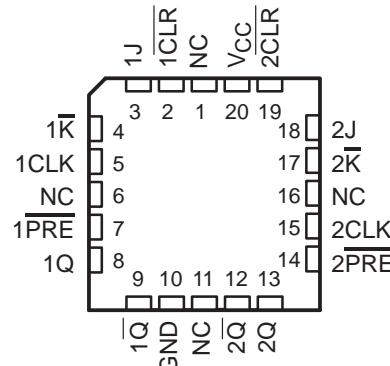
These devices contain two independent J- $\bar{K}$  positive-edge-triggered flip-flops. A low level at the preset (PRE) or clear (CLR) inputs sets or resets the outputs regardless of the levels of the other inputs. When  $\overline{\text{PRE}}$  and  $\overline{\text{CLR}}$  are inactive (high), data at the J and  $\bar{K}$  input meeting the setup-time requirements are transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the J and  $\bar{K}$  inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by grounding  $\bar{K}$  and trying J high. They also can perform as D-type flip-flops if J and  $\bar{K}$  are tied together.

The SN54F109 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74F109 is characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

SN54F109 . . . J PACKAGE  
SN74F109 . . . D OR N PACKAGE  
(TOP VIEW)



SN54F109 . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection

FUNCTION TABLE

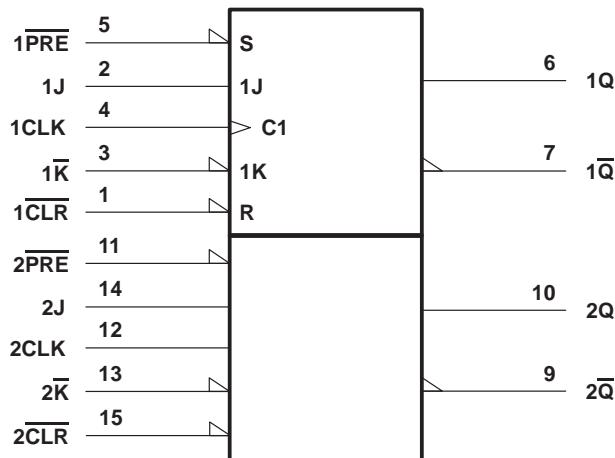
INPUTS					OUTPUTS	
$\overline{\text{PRE}}$	$\overline{\text{CLR}}$	CLK	J	$\bar{K}$	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H <sup>†</sup>	H <sup>†</sup>
H	H	↑	L	L	L	H
H	H	↑	H	L	Toggle	
H	H	↑	L	H	Q <sub>0</sub>	$\bar{Q}_0$
H	H	↑	H	H	H	L
H	H	L	X	X	Q <sub>0</sub>	$\bar{Q}_0$

<sup>†</sup> The output levels are not guaranteed to meet the minimum levels for  $V_{OH}$ . Furthermore, this configuration is nonstable; that is, it will not persist when PRE or CLR returns to its inactive (high) level.

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SDFS047A – MARCH 1987 – REVISED OCTOBER 1993

## logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the D, J, and N packages.

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡**

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input voltage ratings may be exceeded provided the input current ratings are observed.

### **recommended operating conditions**

		SN54F109			SN74F109			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V <sub>IH</sub>	High-level input voltage		2			2		V
V <sub>IL</sub>	Low-level input voltage			0.8			0.8	V
I <sub>IK</sub>	Input clamp current			-18			-18	mA
I <sub>OH</sub>	High-level output current			-1			-1	mA
I <sub>OL</sub>	Low-level output current			20			20	mA
T <sub>A</sub>	Operating free-air temperature	-55		125	0		70	°C

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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	SN54F109			SN74F109			UNIT	
		MIN	TYP†	MAX	MIN	TYP†	MAX		
$V_{IK}$	$V_{CC} = 4.5 \text{ V}$ , $I_I = -18 \text{ mA}$			-1.2			-1.2	V	
$V_{OH}$	$V_{CC} = 4.5 \text{ V}$ , $I_{OH} = -1 \text{ mA}$	2.5	3.4		2.5	3.4		V	
	$V_{CC} = 4.75 \text{ V}$ , $I_{OH} = -1 \text{ mA}$			2.7					
$V_{OL}$	$V_{CC} = 4.5 \text{ V}$ , $I_{OL} = 20 \text{ mA}$		0.3	0.5		0.3	0.5	V	
$I_I$	$V_{CC} = 5.5 \text{ V}$ , $V_I = 7 \text{ V}$			0.1			0.1	mA	
$I_{IH}$	$V_{CC} = 5.5 \text{ V}$ , $V_I = 2.7 \text{ V}$			20			20	$\mu\text{A}$	
$I_{IL}$	$J, \bar{K}, \text{CLK}$ $\text{PRE or CLR}$	$V_{CC} = 5.5 \text{ V}$ , $V_I = 0.5 \text{ V}$		-0.6			-0.6	mA	
				-1.8			-1.8		
$I_{OS}^{\ddagger}$	$V_{CC} = 5.5 \text{ V}$ , $V_O = 0$		-60	-150	-60	-150		mA	
$I_{CC}$	$V_{CC} = 5.5 \text{ V}$ , See Note 2			11.7	17		11.7	17	mA

† All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

NOTE 2:  $I_{CC}$  is measured with  $J, \bar{K}, \text{CLK}$ , and  $\text{PRE}$  grounded then with  $J, \bar{K}, \text{CLK}$ , and  $\text{CLR}$  grounded.

**timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)**

		$V_{CC} = 5 \text{ V}$ , $T_A = 25^\circ\text{C}$	SN54F109		SN74F109		UNIT		
			'F74		MIN MAX				
			MIN	MAX	MIN	MAX			
$f_{clock}$ Clock frequency			0	100	0	70	0	90	MHz
$t_w$	Pulse duration	CLK high, $\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ low	4		4		4	ns	
		CLK low	5		5		5		
$t_{su}$	Setup time, data before $\text{CLK}^\uparrow$	High	3		3		3	ns	
		Low	3		3		3		
	Setup time, inactive-state before $\text{CLK}^\uparrow\$$	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ to CLK	2		2		2		
$t_h$	Hold time, data after $\text{CLK}^\uparrow$	High	1		1		1	ns	
		Low	1		1		1		

§ Inactive-state setup time is also referred to as recovery time.

**switching characteristics (see Note 3)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5 \text{ V}$ , $C_L = 50 \text{ pF}$ , $R_L = 500 \Omega$ , $T_A = 25^\circ\text{C}$	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$ , $C_L = 50 \text{ pF}$ , $R_L = 500 \Omega$ , $T_A = \text{MIN to MAX}^\ddagger$			UNIT		
				'F109					
				MIN	TYP	MAX	MIN	MAX	
$f_{max}$			100	150			70	90	MHz
$t_{PLH}$	CLK	Q or $\overline{Q}$	3	4.9	7		3	9	ns
			3.6	5.8	8	3.6	10.5	3.6	
$t_{PHL}$	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$	Q or $\overline{Q}$	2.4	4.8	7	2.4	9	2.4	ns
			2.7	6.6	9	2.7	11.5	2.7	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

NOTE 3: Load circuits and waveforms are shown in Section 1.



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