National Semiconductor

PRELIMINARY

NM28C64/C64L/C64A
64k (8k x 8) Parallel Extended Voltage Range CMOS EEPROM

General Description

The NM28C64/C64L/C64A are fast, single-power supply CMOS EEPROM organized as 8k by 8 bits. Both READ and WRITE modes function over the full V_{CC} range of 2.7V–5.5V.

In-system programming of the part requires only a simple interface. On-chip address and data latches, self-timed write cycle with auto-clear and V_{CC} power-up/down protection eliminate the need for external timing and protection hardware.

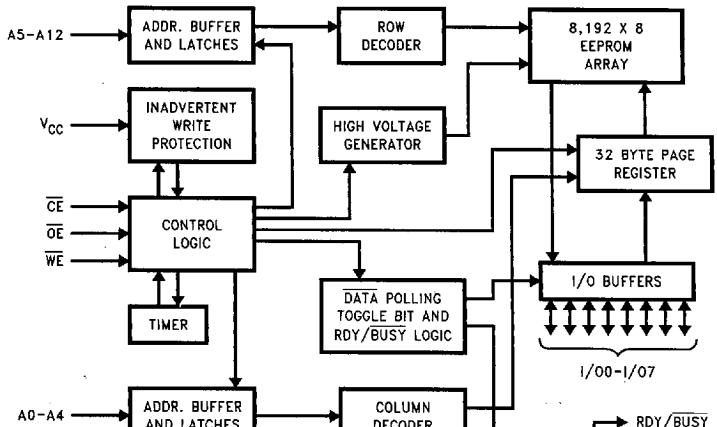
$\overline{DATA}$ and Toggle-Bit Polling and a RDY/$\overline{BUSY}$ pin provide a convenient means for determining the beginning and end of the internal self-timed WRITE cycle.

Both internal hardware and software WRITE protection are provided. Page organization permits the loading of from one to 32 bytes into a data register, the entire page is programmed at one time in 10 ms.

Features

- Voltage Supply
  - — Full Read and Write operation
  - — C64: 4.5V to 5.5V
  - — C64L: 2.7V to 3.6V
  - — C64A: 2.7V to 5.5V
- Low Power Dissipation
  - — 8 mA Active Current
  - — 50 µA CMOS Standby Current
- Read Access Time
  - — 200 ns at 2.7V
  - — 120 ns at 4.5V
- 32 Byte Page Write
- End of Write Detection
  - — $\overline{DATA}$ Polling on I/O_7
  - — Toggle Bit Polling on I/O_6
  - — READY/$\overline{BUSY}$ Open Drain Output
- Hardware Data Protection
- High Reliability CMOS Technology
  - — Endurance 100,000 Cycles
  - — Data Retention: 10 years
- Low Voltage CMOS and TTL Compatible Inputs and Outputs
- JEDEC Standard Byte-Wide Pinout
- Commercial and Industrial Temperature Ranges

Block Diagram



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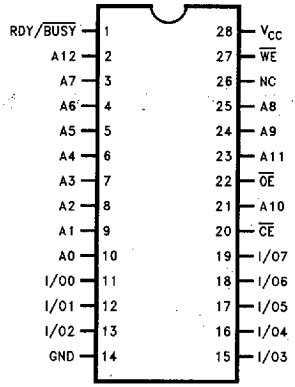
Pin Configurations

DIP (N)



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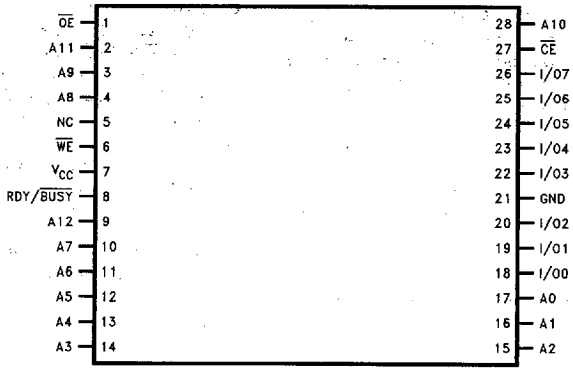
A0–A12	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
I/O_0–I/O_7	Data Inputs/Outputs
RDY/$\overline{BUSY}$	Ready/Busy Output
NC	No Connect

TSOP (T) Package Type I



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Top View

Ordering Information

Commercial Temperature Range (0°C to +70°C)

Order Number	4.5V–5.5V
NM28C64N28 NM28C64T28	

Order Number	2.7V–3.6V
NM28C64LN28 NM28C64LT28	

Order Number	2.7V–5.5V
NM28C64AN28 NM28C64AT28	

Extended Temperature Range (−40°C to +85°C)

Order Number	4.5V–5.5V
NM28C64EN28 NM28C64ET28	

Order Number	2.7V–3.6V
NM28C64LEN28 NM28C64LET28	

Order Number	2.7V–5.5V
NM28C64AEN28 NM28C64AET28	

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Functional Description

DEVICE OPERATION

Read Mode

Data are transferred from the addressed memory location to the external data bus when $\overline{WE}$ is held HIGH, $\overline{OE}$ is held LOW, and $\overline{CE}$ is held LOW. The 2-line control architecture of the $\overline{OE}$ and $\overline{CE}$ pins eliminates bus contention in a system environment. When either the $\overline{OE}$ or $\overline{CE}$ lines are set HIGH, the NM28C64A releases the data bus.

Write Mode

A write cycle is initiated when both the $\overline{WE}$ and $\overline{CE}$ lines are LOW and $\overline{OE}$ is HIGH. The address is latched on the falling edge of either $\overline{WE}$ or $\overline{CE}$, whichever occurs last. The data are latched on the rising edge of either the $\overline{WE}$ or $\overline{CE}$, whichever occurs first. It takes approximately 10 ms for the write cycle to erase the addressed memory locations and store the new data.

Page Write

From one to thirty-two bytes can be written to the selected page address (A5–A12) during any write operation. The page address is latched once the data-load cycle is started. The data latch loading may be interrupted in order to fetch data from another system location. However, data loading must continue again within the byte load cycle time (t_{BLC}), otherwise the internal programming cycle will begin. When returning to loading data into the latches, the page address is ignored because of the latched-page register.

There are no page write window limitations; the page write window can continue indefinitely as long as the $t_{BLC\ MAX}$ time is not exceeded.

The program cycle first erases data located in the addressed cells, then writes the new data into these addressed cells. A page write does not rewrite the entire page, only those locations selected during data-latch loading.

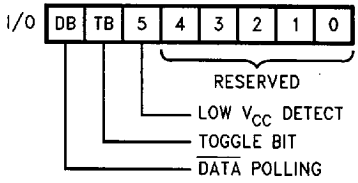
Write Abort

During a data load cycle in preparation for programming, $\overline{OE}$ must be held at V_{IH}. If $\overline{OE}$ is held LOW during the rising edge of $\overline{CE}$ ($\overline{CE}$ controlled WRITE), or $\overline{WE}$ ($\overline{WE}$-controlled WRITE), the WRITE operation is aborted and the data latches are reset.

RDY/$\overline{BUSY}$

The RDY/$\overline{BUSY}$ pin is an open drain output that monitor the status of a write cycle. The open drain connection allows for OR-tying several devices to the same RDY/$\overline{BUSY}$ pin. This output is actively pulled LOW during the write cycle and released at the end of the cycle.

Additional methods for monitoring status and internal programming cycles are provided.



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Toggle Bit (I/O_6)

The toggle bit (I/O_6) toggles between ZERO and ONE on alternate READS while the NM28C64A performs an internal write cycle. After the write cycle is completed, I/O_6 stops toggling.

$\overline{DATA}$ Polling (I/O_7)

A third method for determining the end an internal programming cycle is $\overline{DATA}$ polling. This method allows the host to perform a simple bit test to determine whether the device is in an internal write cycle without the need for system interrupts or external hardware.

After the initiation of the internal programming cycle, bit 7 of the last byte written is complemented and sent to I/O_7. The host can read I/O_7 to determine whether or not the device is in an internal write cycle. Upon completion of the write cycle, I/O_7 provides the true value.

Low V_{CC} Detect (I/O_5)

Once an internal write cycle is initiated, it continues to completion even if the supply voltage falls below 2.0V (typical) during the cycle. In the event that V_{CC} does fall below 2.0V during the programming cycle, an internal latch is set. Its status can be polled by reading the state of I/O_5.

A high level on I/O_5 indicates that a sub-2.0V level was detected and programmed-data integrity may be suspect.

Hardware Data Protection

The device is protected from inadvertent memory writes by the following three hardware methods:

1. V_{CC} Sense: The write function is inhibited if V_{CC} falls below 2.0V (typical), prior to the beginning of an internal write cycle.
2. Noise Protection: A write cycle will not be initiated if the $\overline{WE}$ or $\overline{CE}$ LOW pulse is $<$ 20 ns wide (typical).
3. Write Inhibit: Write cycles can be inhibited during power-on and power-off by holding any one or more of the following pins to the indicated levels.
   (a) $\overline{OE}$ LOW
   (b) $\overline{CE}$ HIGH
   (c) $\overline{WE}$ HIGH

Chip Erase

The entire memory can be erased (set to logic ONE) by a single operation. To activate Chip Erase, $\overline{OE}$ must be raised to 12V ±0.5V and all I/O pins set HIGH while $\overline{CE}$ and $\overline{WE}$ are simultaneously brought LOW. The erase operation occurs within 10 ms.

Device Identification

The user has an extra 32 bytes (one page) of memory available for device identification. This extra memory can be read or written to just like the regular memory array but only by setting address pin A9 to 12V ±0.5V and selecting addresses 1FE0h–1FFFh.

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Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Temperature Under Bias	−55°C to +125°C
Storage Temperature	−65°C to +150°C
All Input Voltage (including NC pins) with Respect to Ground	−0.6V to V_{CC} + 0.6V
Lead Temperature (Soldering, 10 seconds)	+300°C
All Output Voltages with Respect to Ground	−0.6V to V_{CC} + 0.6V
Voltage on $\overline{OE}$ and A9 with Respect to Ground	−0.6V to +13.5V
ESD Rating	2000V

Note: *Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

DC and AC Operating Range

		NM28C64	NM28C64L	NM28C64A
Operating Temperature (Case)	Comm.	0°C–70°C	0°C–70°C	0°C–70°C
	Indust.	−40°C–85°C	−40°C–85°C	−40°C–85°C
V_{CC} Power Supply		4.5V–5.5V	2.7V–3.6V	2.7V–5.5V

Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O	Power	A9
Standby	V_{IH}	X	X	High Z	Standby	
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}	Active	
Write ($\overline{WE}$ Controlled)	V_{IL}	V_{IH}	⊓	D_{IN}	Active	
Write ($\overline{CE}$ Controlled)	⊓	V_{IH}	V_{IL}	D_{IN}	Active	
Read and Write Inhibit	V_{IL}	V_{IH}	V_{IH}	High Z	Active	
Output Disable	X	V_{IH}	X	High Z		
Chip Erase*	V_{IL}	12V ±0.5V	⊓	$D_{IN} = V_{IH}$	Active	
Chip ID Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}	Active	12V ±0.5V
Chip ID Write	V_{IL}	V_{IH}	V_{IL}	D_{IN}	Active	12V ±0.5V

*$\overline{OE}$ must be raised to 12V prior to establishing the condition $\overline{CE} = \overline{WE} = V_{IL}$ to initiate a chip-erase cycle.

DC Characteristics

Symbol	Parameter	Test Conditions	Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC}		5	μA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0V to V_{CC}		5	μA
I_{SB}	V_{CC} Standby Current CMOS	$\overline{CE} = V_{CC}$		50	μA
I_{CC}	V_{CC} Active Current AC	f = 5 MHz; I_{OUT} = 0 mA; $\overline{CE} = V_{IL}$		8.0	mA
V_{IL}	Input Low Voltage			0.6	V
V_{IH}	Input High Voltage		2.0		V
V_{OL}	Output Low Voltage	I_{OL} = 1 mA		0.3	V
		I_{OL} = 2 mA for RDY/$\overline{BUSY}$		0.3	V
V_{OH}	Output High Voltage	I_{OH} = −100 μA	2.0		V

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Capacitance ($f = 1.0$ MHz, $T_A = 25°C$)

Symbol	Conditions	Typ	Max	Units
C_{IN}	$V_{IN} = 0V$	4	6	pF
C_{VO}	$V_{I/O} = 0V$	8	12	pF

AC Read Characteristics—NM28C64

Symbol	Parameter	V_{CC}	Min	Typ	Max	Units
t_{ACC}	Address to Output Delay	4.5V–5.5V			120	ns
t_{CE}	$\overline{CE}$ to Output Delay	4.5V–5.5V			120	ns
t_{OE}	$\overline{OE}$ to Output Delay	4.5V–5.5V	0		50	ns
t_{OH}	Output Hold from Address Change	4.5V–5.5V	0			ns
t_{LZ} (Note 1)	$\overline{CE}$ Low to Output Active	4.5V–5.5V	0			ns
t_{OLZ} (Note 1)	$\overline{OE}$ Low to Output Active	4.5V–5.5V	0			ns
t_{HZ} (Notes 1, 2)	$\overline{CE}$ High to Output Float	4.5V–5.5V			50	ns
t_{OHZ} (Notes 1, 2)	$\overline{OE}$ High to Output Float	4.5V–5.5V			50	ns

AC Read Characteristics—NM28C64L

Symbol	Parameter	V_{CC}	Min	Typ	Max	Units
t_{ACC}	Address to Output Delay	2.7V–3.6V			200	ns
t_{CE}	$\overline{CE}$ to Output Delay	2.7V–3.6V			200	ns
t_{OE}	$\overline{OE}$ to Output Delay	2.7V–3.6V	0		80	ns
t_{OH}	Output Hold from Address Change	2.7V–3.6V	0			ns
t_{LZ} (Note 1)	$\overline{CE}$ Low to Output Active	2.7V–3.6V	0			ns
t_{OLZ} (Note 1)	$\overline{OE}$ Low to Output Active	2.7V–3.6V	0			ns
t_{HZ} (Notes 1, 2)	$\overline{CE}$ High to Output Float	2.7V–3.6V			50	ns
t_{OHZ} (Notes 1, 2)	$\overline{OE}$ High to Output Float	2.7V–3.6V			50	ns

AC Read Characteristics—NM28C64A

Symbol	Parameter	V_{CC}	Min	Typ	Max	Units
t_{ACC}	Address to Output Delay	2.7V–4.4V			200	ns
		4.5V–5.5V			120	ns
t_{CE}	$\overline{CE}$ to Output Delay	2.7V–4.4V			200	ns
		4.5V–5.5V			120	ns
t_{OE}	$\overline{OE}$ to Output Delay	2.7V–4.4V			80	ns
		4.5V–5.5V	0		50	ns
t_{OH}	Output Hold from Address Change	2.7V–4.4V				ns
		4.5V–5.5V				ns
t_{LZ} (Note 1)	$\overline{CE}$ Low to Output Active	2.7V–4.4V	0			ns
		4.5V–5.5V	0			ns
t_{OLZ} (Note 1)	$\overline{OE}$ Low to Output Active	2.7V–4.4V	0			ns
		4.5V–5.5V	0			ns
t_{HZ} (Notes 1, 2)	$\overline{CE}$ High to Output Float	2.7V–4.4V			50	ns
		4.5V–5.5V			50	ns
t_{OHZ} (Notes 1, 2)	$\overline{OE}$ High to Output Float	2.7V–4.4V			50	ns
		4.5V–5.5V			50	ns

Note 1: This parameter is characterized and is not 100% tested.

Note 2: Output floating (High Z) is defined as the state when the external data line is no longer driven by the output buffer.

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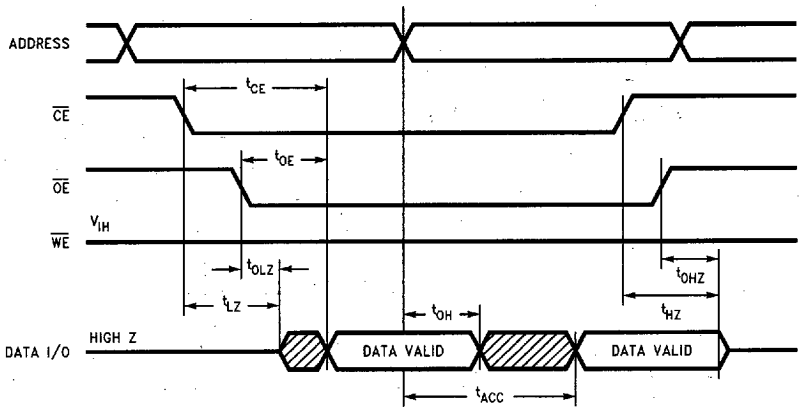
AC Read Waveforms



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AC Write Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
t_{WC}	Write Cycle Time				10	ms
t_{AH}	Address Hold Time		100			ns
t_{AS}	Address Setup		10			ns
t_{CH}	Write Hold Time		0			ns
t_{CS}	Write Setup Time		0			ns
t_{DH}	Data Hold		10			ns
t_{DS}	Data Setup Time		100			ns
t_{OEH}	$\overline{OE}$ High Hold Time		10			ns
t_{OES}	$\overline{OE}$ High Setup Time		10			ns
t_{RB}	$\overline{WE}$ Low to RSY/$\overline{BUSY}$ Low				120	ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)		150			ns
t_{BLC}	Byte Load Cycle Time		1		100	μs
t_{INIT}	Write Inhibit Period after Power Up		5		15	ms

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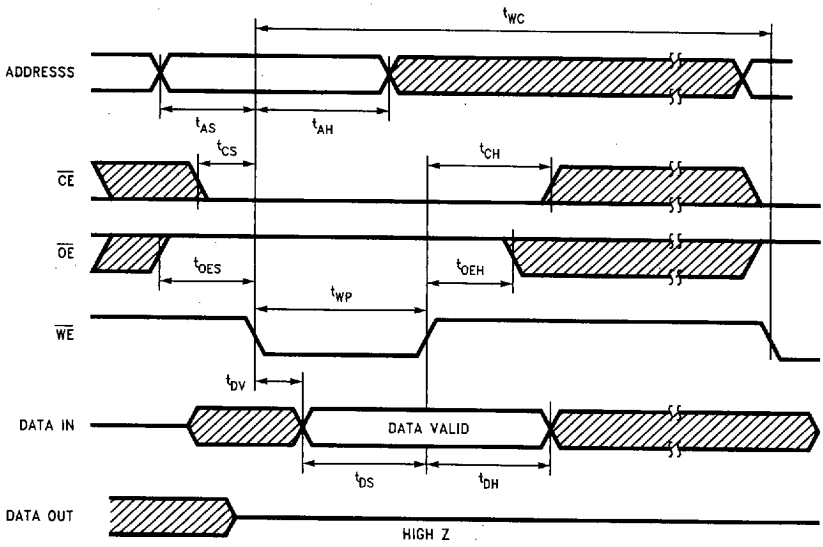
AC Write Waveforms—$\overline{WE}$ Controlled



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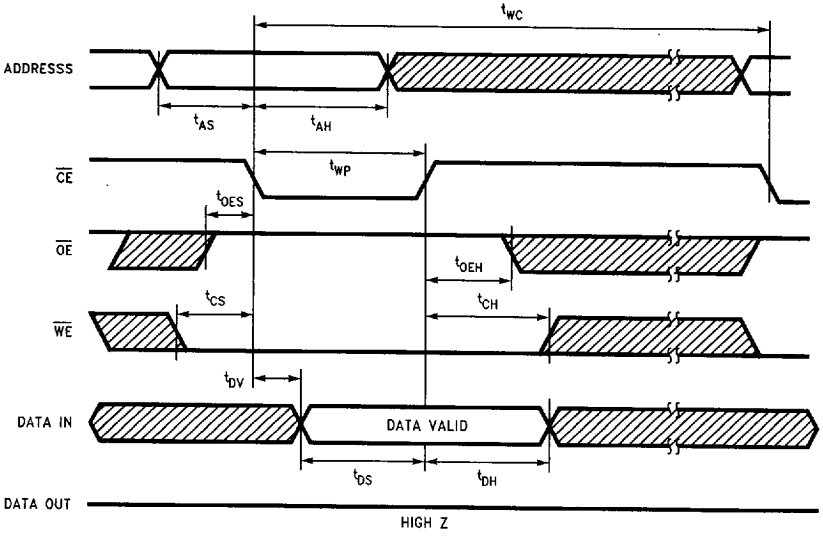
AC Write Waveforms—$\overline{CE}$ Controlled



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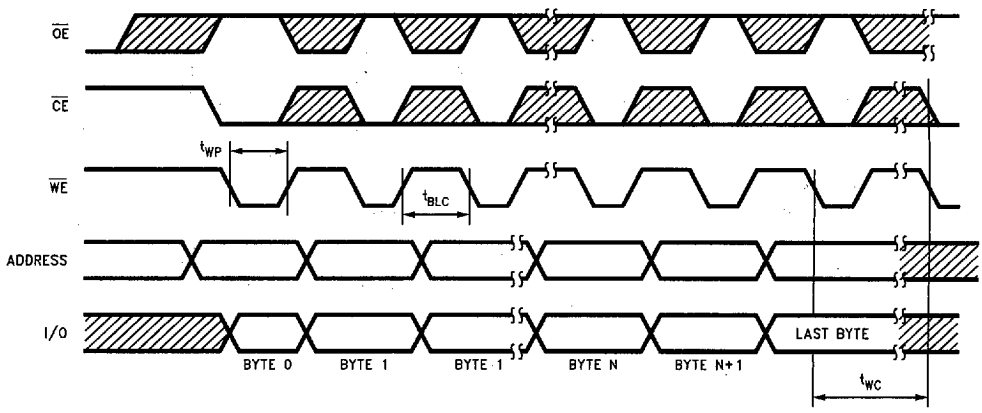
Page Write Cycle



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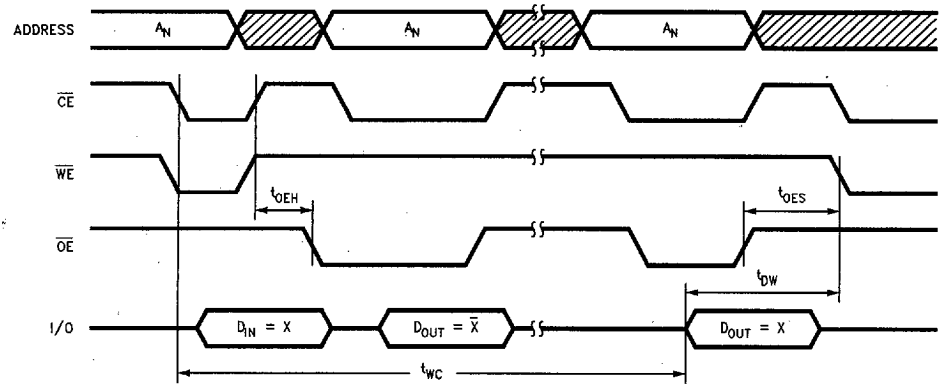
Data Polling Waveforms (Note 1)



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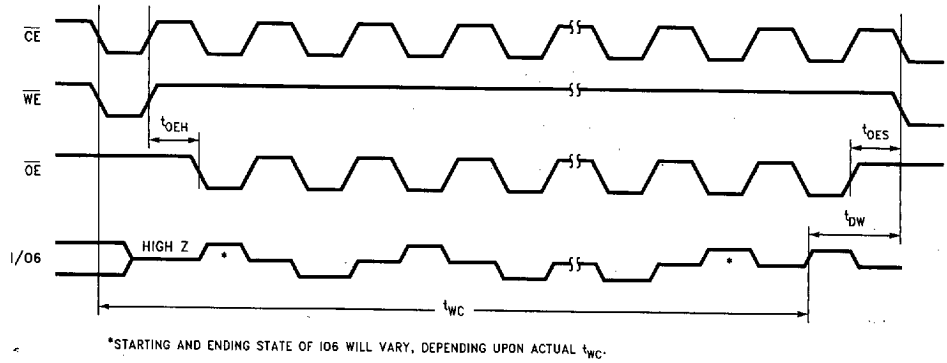
Toggle Bit Timing Diagram (Note 1)



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Note 1: Polling operations are by definition read cycles and are therefore subject to read cycle timings

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