CIRRUS LOGIC®

CS4412A

30 W Quad Half-Bridge Digital Amplifier Power Stage

Features

- Configurable Outputs (10% THD+N)
  - 2 x 15 W into 8 Ω, Full-Bridge
  - 1 x 30 W into 4 Ω, Parallel Full-Bridge
  - 4 x 7.5 W into 4 Ω, Half-Bridge
  - 2 x 7.5 W into 4 Ω, Half-Bridge + 1 x 15 W into 8 Ω, Full-Bridge
- Space-Efficient Thermally-Enhanced QFN
  - No External Heat Sink Required
- > 100 dB Dynamic Range - System Level
- < 0.1% THD+N @ 1 W - System Level
- Built-In Protection with Error Reporting
  - Over-Current
  - Thermal Warning and Overload
  - Under-Voltage
- +8 V to +18 V High Voltage Supply
- PWM Popguard® Technology for Quiet Startup
- No Bootstrap Required
- Low Quiescent Current
- Low Power Standby Mode

Common Applications

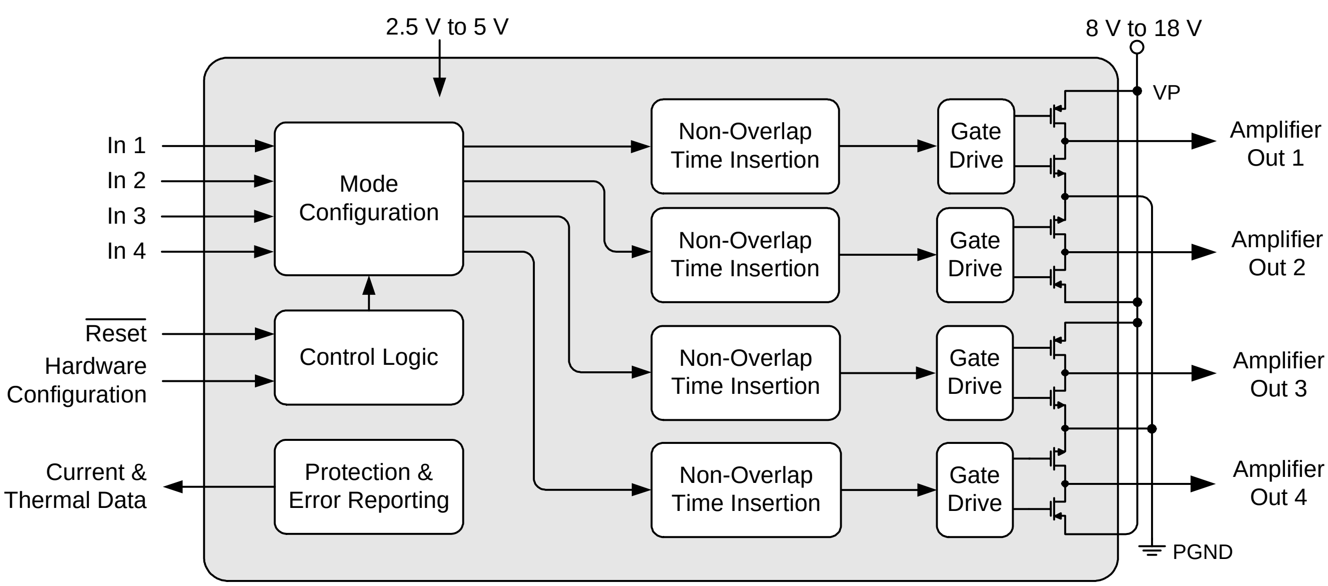
- Integrated Digital Televisions
- Portable Media Player Docking Stations
- Mini/Micro Shelf Systems
- Powered Desktop Speakers

General Description

The CS4412A is a high-efficiency power stage for digital Class-D amplifiers designed to input PWM signals from a modulator such as the CS4525. The power stage outputs can be configured as four half-bridge channels, two half-bridge channels and one full-bridge channel, two full-bridge channels, or one parallel full-bridge channel.

The CS4412A integrates on-chip over-current, under-voltage, over-temperature protection, and error reporting as well as a thermal warning indicator. The low $R_{DS(ON)}$ outputs can source up to 2.5 A peak current, delivering high efficiency which allows small device package and lower power supplies.

The CS4412A is available in a 48-pin QFN package in Commercial grade (-10°C to +70°C). The CRD4412A customer reference design is also available. Please refer to "Ordering Information" on page 23 for complete ordering information.



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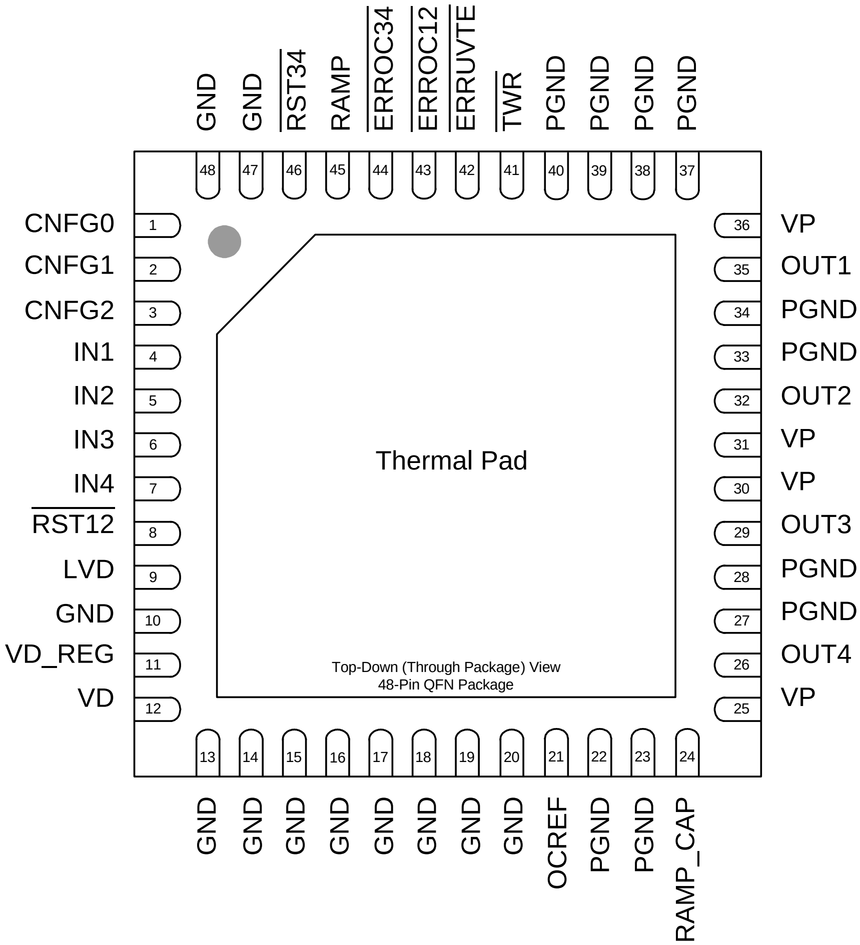
1. PIN DESCRIPTION



Pin Name	Pin #	Pin Description
CNFG0 CNFG1 CNFG2	1 2 3	**Out Configuration Select** (*Input*) - Used to set the PWM output configuration mode. See “Output Mode Configuration” on page 15.
IN1 IN2 IN3 IN4	4 5 6 7	**PWM Input** (*Input*) - Logic-level switching inputs from a PWM modulator.
$\overline{\text{RST12}}$ $\overline{\text{RST34}}$	8 46	**Reset Input** (*Input*) - Reset inputs for channels 1/2 and 3/4, respectively. Active low.
LVD	9	**VD Voltage Level Indicator** (*Input*) - Identifies the voltage level attached to VD. When applying 5.0 V to VD, LVD must be connected to VD. When applying 2.5 V or 3.3 V to VD, LVD must be GND.
VD_REG	11	**Core Digital Power** (*Output*) - Internally generated low voltage power supply for digital logic.
VD	12	**Digital Power** (*Input*) - Positive power supply for the internal regulators and digital I/O.
OCREF	21	**Over-current Reference** (*Input*) - Sets over-current trigger level. Connect pin through a resistor to GND. See “Device Protection and Error Reporting” on page 19. This pin should not be left floating.

Pin Name	Pin #	Pin Description
RAMP_CAP	24	**Output Ramp Capacitor** (*Input*) - Used by the PWM PopGuard Transient Control to suppress the initial pop in half-bridge-configured outputs.
GND	10,13 14,15 16,17 18,19 20,47 48	**Ground** (*Input*) - Ground for the internal logic and I/O. These pins should be connected to the common system ground.
VP	25,30 31,36	**High Voltage Output Power** (*Input*) - High voltage power supply for the individual output power half-bridge devices.
PGND	22,23 27,28 33,34 37,38 39,40	**Power Ground** (*Input*) - Ground for the individual output power half-bridge devices. These pins should be connected to the common system ground.
OUT4 OUT3 OUT2 OUT1	26 29 32 35	**PWM Output** (*Output*) - Amplified PWM power outputs.
$\overline{\text{TWR}}$	41	**Thermal Warning Output** (*Output*) - Thermal warning output. Open drain, active low. See "Device Protection and Error Reporting" on page 19.
$\overline{\text{ERRUVTE}}$	42	**Thermal and Under-voltage Error Output** (*Output*) - Error flag for thermal shutdown and under-voltage. Open drain, active low. See "Device Protection and Error Reporting" on page 19
$\overline{\text{ERROC12}}$ $\overline{\text{ERROC34}}$	43 44	**Over-current Error Output** (*Output*) - Over-current error flag for the associated outputs. Open drain, active low. See "Device Protection and Error Reporting" on page 19.
RAMP	45	**Ramp-up/down Select** (*Input*) - Set high to enable ramping. When set low, ramping is disabled. See "PWM Popguard Transient Control" on page 13.
Thermal Pad	-	**Thermal Pad** - Thermal relief pad for optimized heat dissipation. See "QFN Thermal Pad" on page 20 for more information.

2. CHARACTERISTICS AND SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS

GND = PGND = 0 V, all voltages with respect to ground.

Parameters		Symbol	Min	Nom	Max	Units
DC Power Supply						
Digital Core		VD	2.375	2.5	2.625	V
		VD	3.135	3.3	3.465	V
		VD	4.75	5.0	5.25	V
Power Stage		VP	8.0		18.0	V
Temperature						
Ambient Temperature	Commercial	T_A	-10	-	+70	°C
Junction Temperature		T_J	-10	-	+125	°C

ABSOLUTE MAXIMUM RATINGS

GND = PGND = 0 V; all voltages with respect to ground.

Parameters		Symbol	Min	Max	Units
DC Power Supply					
Power Stage	Outputs Switching and Under Load	VP	-0.3	19.8	V
Power Stage	No Output Switching	VP	-0.3	23.0	V
Digital Core		VD	-0.3	6.0	V
Inputs					
Input Current	(Note 1)	I_{in}	-	±10	mA
Digital Input Voltage	(Note 2)	V_{IND}	-0.3	VD + 0.4	V
Temperature					
Ambient Operating Temperature - Power Applied	Commercial	T_A	-20	+85	°C
Storage Temperature		T_{stg}	-65	+150	°C

WARNING: Operation beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

Notes:
1. Any pin except supplies. Transient currents of up to ±100 mA on the PWM input pins will not cause SCR latch-up.
2. The maximum over/under voltage is limited by the input current.

PWM POWER OUTPUT CHARACTERISTICS

Test Conditions (unless otherwise specified): GND = PGND = 0 V; All voltages with respect to ground; T_A = 25°C; VD = 3.3 V; VP = 18 V; R_L = 8 Ω for full-bridge, R_L = 4 Ω for half-bridge and parallel full-bridge; PWM Switch Rate = 384 kHz; 10 Hz to 20 kHz Measurement Bandwidth; Input source is CS4525 PWM_SIG outputs; Performance measurements taken with a full-scale 997 Hz sine wave, an AES17 measurement filter; Half-Bridge measurements taken through the Half-Bridge Output Filter shown in Figure 5; Stereo Full-Bridge and Parallel Full-Bridge measurements taken through the Full-Bridge Output Filter shown in Figure 6;.

Parameters	Symbol	Conditions	Min	Typ	Max	Units
Power Output per Channel						
Stereo Full-Bridge	P_O	THD+N < 10%	-	15	-	W
		THD+N < 1%	-	12	-	W
Half-Bridge		THD+N < 10%	-	7.5	-	W
		THD+N < 1%	-	5.5	-	W
Parallel Full-Bridge		THD+N < 10%	-	30	-	W
		THD+N < 1%	-	23.5	-	W
Total Harmonic Distortion + Noise						
Stereo Full-Bridge	THD+N	P_O = 1 W	-	0.08	-	%
		P_O = 0 dBFS = 11.3 W	-	0.10	-	%
Half-Bridge		P_O = 1 W	-	0.12	-	%
		P_O = 0 dBFS = 5.0 W	-	0.19	-	%
Parallel Full-Bridge		P_O = 1 W	-	0.1	-	%
		P_O = 0 dBFS = 22.6 W	-	0.3	-	%
Dynamic Range						
Stereo Full-Bridge	DYR	P_O = -60 dBFS, A-Weighted	-	102	-	dB
		P_O = -60 dBFS, Unweighted	-	99	-	dB
Half-Bridge		P_O = -60 dBFS, A-Weighted	-	102	-	dB
		P_O = -60 dBFS, Unweighted	-	97	-	dB
Parallel Full-Bridge		P_O = -60 dBFS, A-Weighted	-	102	-	dB
		P_O = -60 dBFS, Unweighted	-	99	-	dB
MOSFET On Resistance	$R_{DS(ON)}$	I_d = 0.5 A, T_J = 50°C	-	280	-	mΩ
Efficiency	h	P_O = 2 x 15 W, R_L = 8 Ω	-	85	-	%
Minimum Output Pulse Width	PW_{min}	No Load	-	25	-	ns
Rise Time of OUTx	t_r	Resistive Load	-	10	-	ns
Fall Time of OUTx	t_f	Resistive Load	-	5	-	ns
PWM Output Over-Current Error Trigger Point	I_{CE}	T_A = 25°C, OCREF = 16.2 kΩ	-	2.5	-	A
		T_A = 25°C, OCREF = 18 kΩ	-	2.1	-	A
		T_A = 25°C, OCREF = 22 kΩ	-	1.7	-	A
Junction Thermal Warning Trigger Point	T_{TW}		-	105	-	°C
Junction Thermal Error Trigger Point	T_{TE}		-	125	-	°C
VP Under-Voltage Error Falling Trigger Point	V_{UVFALL}	T_A = 25°C	-	4.7	4.9	V
VP Under-Voltage Error Rising Trigger Point	V_{UVRISE}	T_A = 25°C	-	4.95	5.4	V

DC ELECTRICAL CHARACTERISTICS

GND = PGND = 0 V; All voltages with respect to ground; PWM switch rate = 384 kHz; Unless otherwise specified.

Parameters		Min	Typ	Max	Units
Normal Operation	(Notes 3, 5)				
Power Supply Current	VD = 3.3 V	-	20	-	mA
Power Dissipation	VD = 3.3 V	-	66	-	mW
Power-Down Mode	(Note 4)				
Power Supply Current	VD = 3 .3 V	-	2	-	mA
VD_REG Characteristics					
Nominal Voltage DC current source		2.25 -	2.5 -	2.75 3	V mA

Notes: 3. Normal operation is defined as $\overline{RST12}$ and $\overline{RST34}$ = HI.

4. Power-Down Mode is defined as $\overline{RST12}$ and $\overline{RST34}$ = LOW with all input lines held static.

5. Power supply current increases with increasing PWM switching rates.

DIGITAL INTERFACE SPECIFICATIONS

GND = PGND = 0 V; All voltages with respect to ground; Unless otherwise specified.

Parameters		Symbol	Min	Max	Units
High-Level Input Voltage		V_{IH}	0.7*VD_REG	VD	V
Low-Level Input Voltage		V_{IL}	-	0.20*VD_REG	V
High-Level Output Voltage	I_o = 2 mA	V_{OH}	0.90*VD	-	V
Input Leakage Current		I_{in}	-	±10	µA
Input Capacitance			-	8	pF

DIGITAL I/O PIN CHARACTERISTICS

The logic level for each input is set by its corresponding power supply and should not exceed the maximum ratings.

Power Supply	Pin Number	Pin Name	I/O	Driver	Receiver
VD	1	CNFG0	Input	-	2.5 V - 5.0 V
	2	CNFG1	Input	-	2.5 V - 5.0 V
	3	CNFG2	Input	-	2.5 V - 5.0 V
	4	IN1	Input	-	2.5 V - 5.0 V
	5	IN2	Input	-	2.5 V - 5.0 V
	6	IN3	Input	-	2.5 V - 5.0 V
	7	IN4	Input	-	2.5 V - 5.0 V
	8	$\overline{\text{RST12}}$	Input	-	2.5 V - 5.0 V
	9	LVD	Input	-	2.5 V - 5.0 V
	41	$\overline{\text{TWR}}$	Output	2.5 V - 5.0 V, Open Drain	-
	42	$\overline{\text{ERRUVTE}}$	Output	2.5 V - 5.0 V, Open Drain	-
	43	$\overline{\text{ERROC12}}$	Output	2.5 V - 5.0 V, Open Drain	-
	44	$\overline{\text{ERROC34}}$	Output	2.5 V - 5.0 V, Open Drain	-
	45	RAMP	Input	-	2.5 V - 5.0 V
	46	$\overline{\text{RST34}}$	Input	-	2.5 V - 5.0 V
VP	35	OUT1	Output	8 V - 18 V Power MOSFET	-
	32	OUT2	Output	8 V - 18 V Power MOSFET	-
	29	OUT3	Output	8 V - 18 V Power MOSFET	-
	26	OUT4	Output	8 V - 18 V Power MOSFET	-

Table 1. I/O Power Rails

3. TYPICAL CONNECTION DIAGRAMS

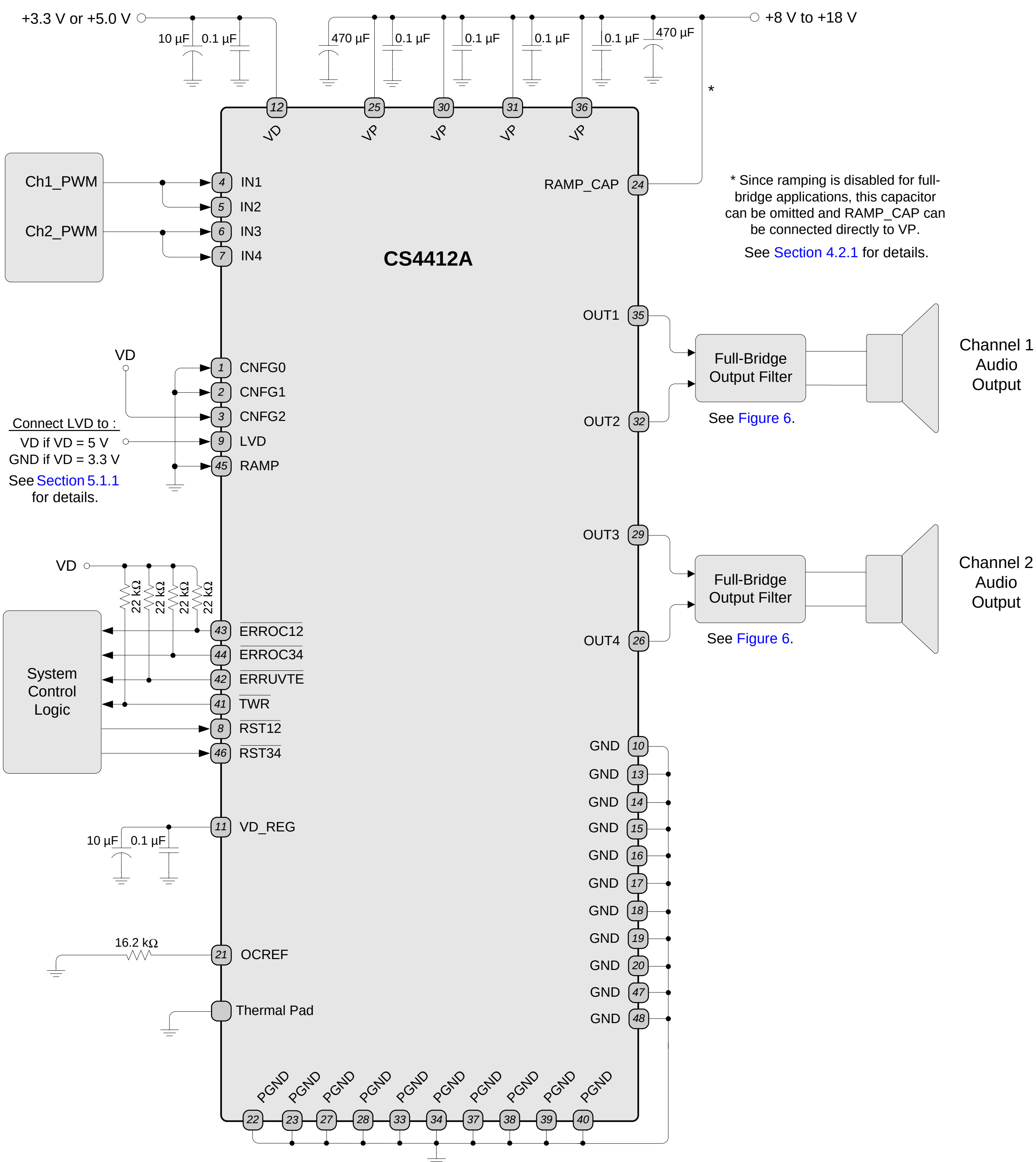


Figure 1. Stereo Full-Bridge Typical Connection Diagram

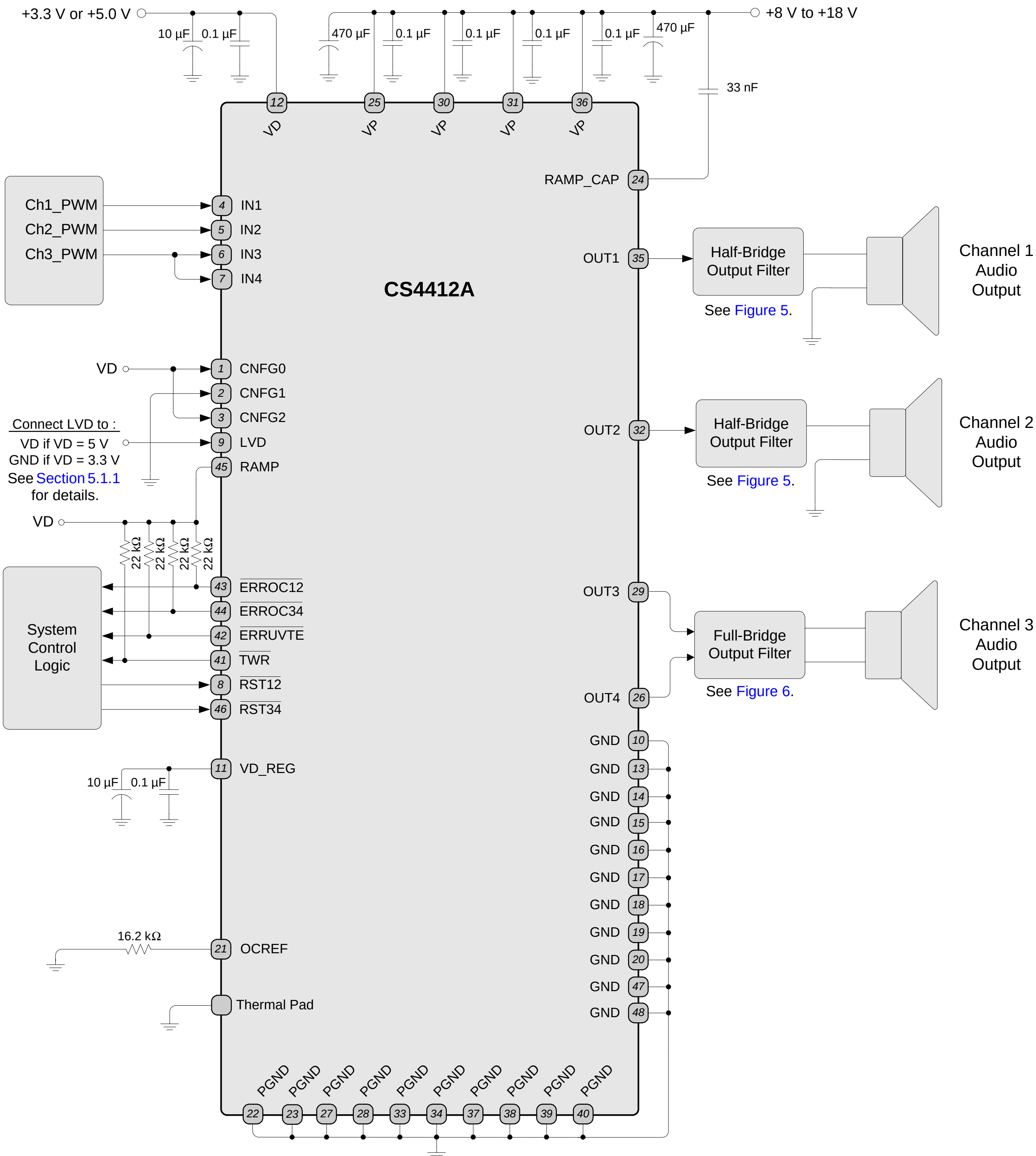


Figure 2. 2.1 Channel Typical Connection Diagram

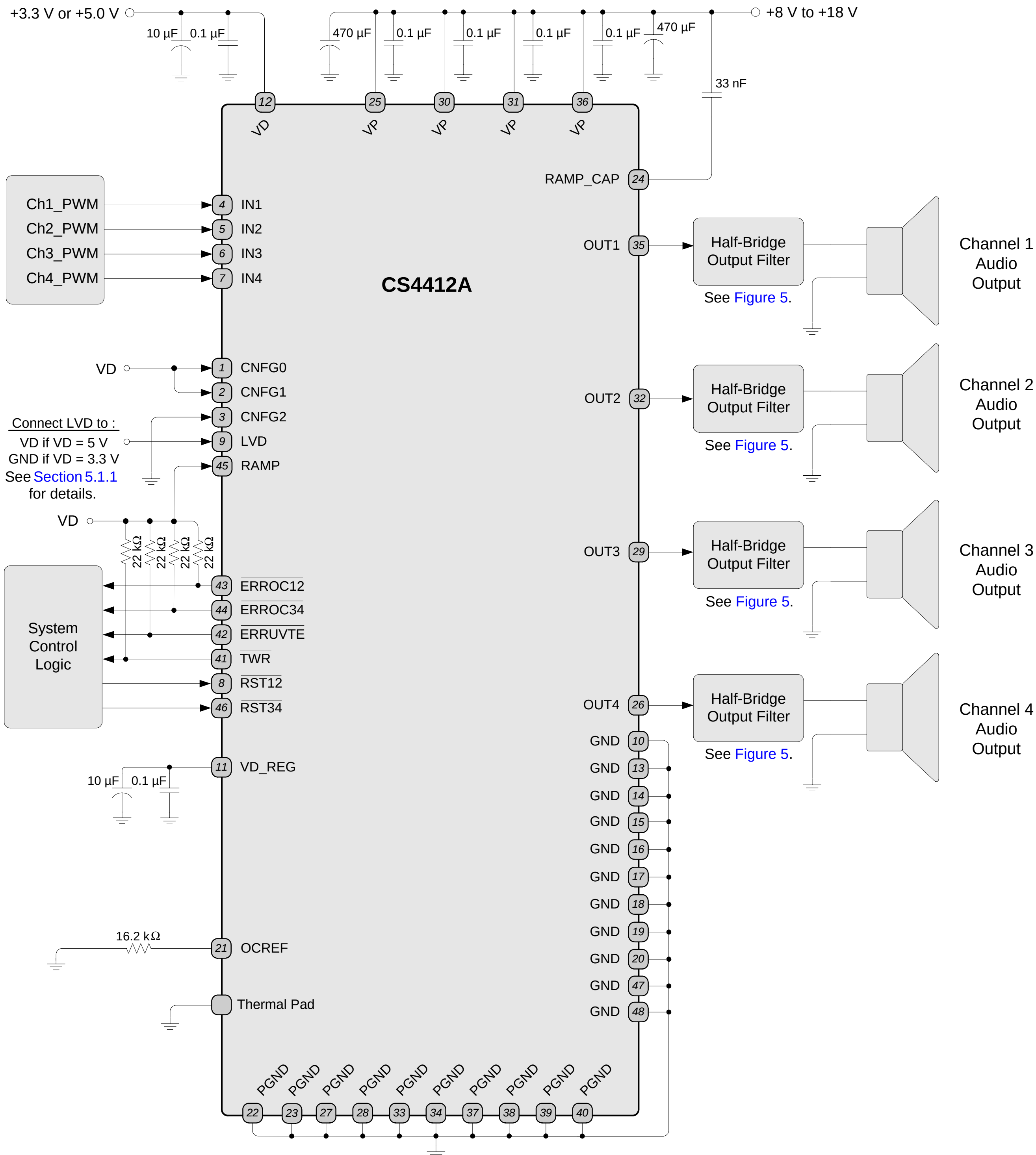


Figure 3. 4 Channel Half-Bridge Typical Connection Diagram

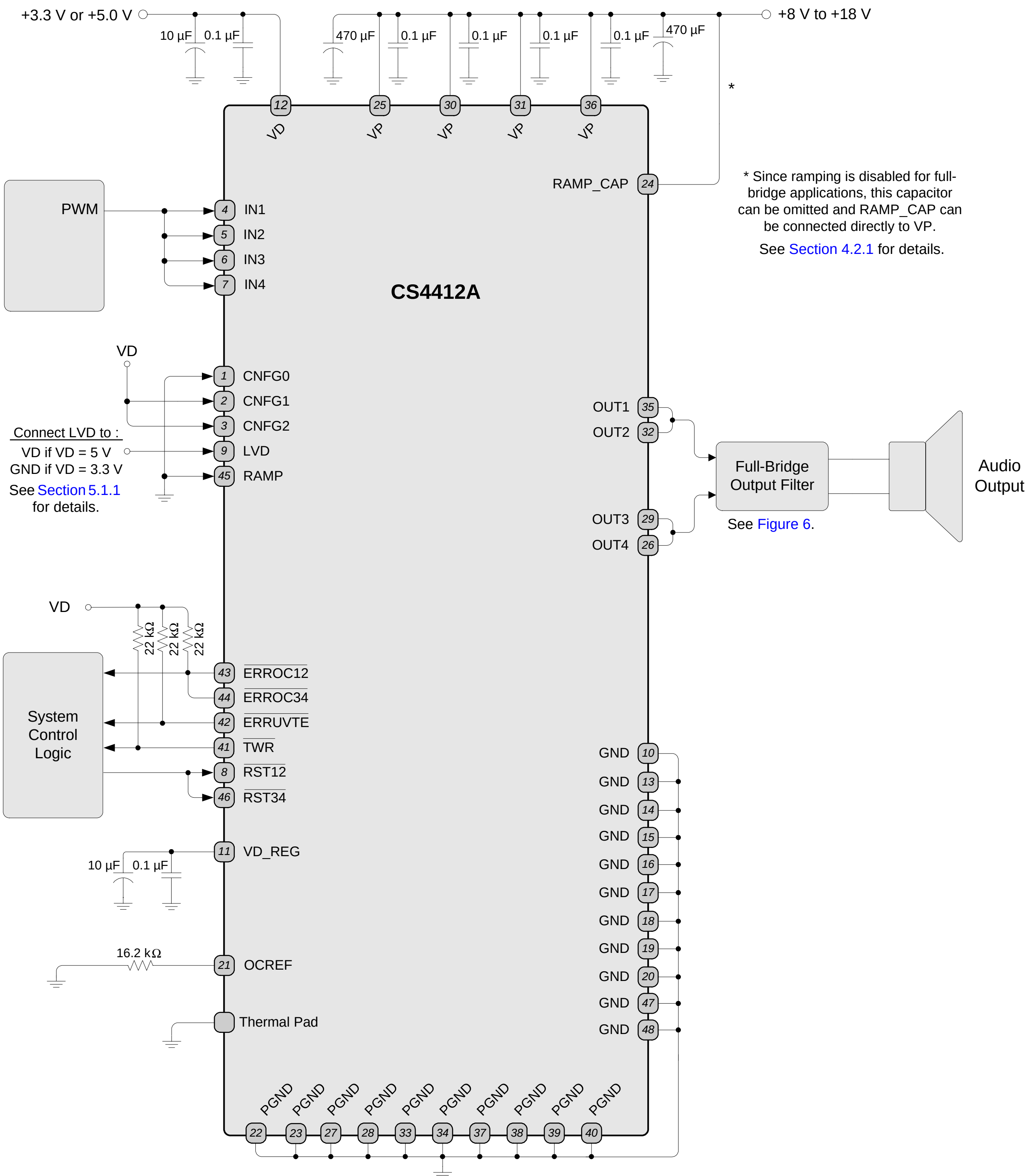


Figure 4. Parallel Full-Bridge Typical Connection Diagram

4. APPLICATIONS

4.1 Overview

The CS4412A is a high-efficiency power stage for digital Class-D amplifiers designed to be configured as four half-bridge channels, two half-bridge channels and one full-bridge channel, two full-bridge channels, or one parallel full-bridge channel.

The CS4412A integrates on-chip over-current, under-voltage, over-temperature protection and error reporting as well as a thermal warning indicator. The low $R_{DS(ON)}$ outputs can source up to 2.5 A peak current, delivering 85% efficiency. This efficiency provides for a smaller device package, smaller power supplies, and no external heat sink.

4.2 Reset and Power-Up

Reliable power-up can be accomplished by keeping the device in reset until the power supplies and configuration pins are stable. It is also recommended that the $\overline{RST12}$ and $\overline{RST34}$ pins be activated if the voltage supplies drop below the recommended operating condition to prevent power-glitch related issues.

When the $\overline{RST12}$ or $\overline{RST34}$ are low, the corresponding channels of the CS4412A enter a low-power mode. All of the channels' internal states are reset, and the corresponding power output pins are held in a high-impedance state. When $\overline{RST12}$ or $\overline{RST34}$ are high, the corresponding outputs begin normal operation according to the RAMP, CNFG[2:0], and IN1 - IN4 pins.

4.2.1 PWM Popguard Transient Control

The CS4412A uses PWM Popguard technology to minimize the effects of output transients during power-up and power-down for half-bridge configurations. This technique reduces the audio transients commonly produced by half-bridge, single-supply amplifiers when implemented with external DC-blocking capacitors connected in series with the audio outputs.

WARNING: The Popguard feature can not be used for the CS4412A in applications where VP exceeds 12 V. Doing so could result in permanent damage to the CS4412A. The RAMP pin must always be tied low in applications where VP exceeds 12 V.

When the device is configured for ramping (RAMP set high) and $\overline{RST12}$ or $\overline{RST34}$ is set high, the corresponding power outputs will ramp-up to the bias point (VP/2). This gradual voltage ramping allows time for the external DC-blocking capacitor to charge to the quiescent voltage, minimizing the power-up transient. The corresponding outputs will not begin normal operation until the ramp has reached the bias point. The time it takes to complete a ramp-up sequence will vary slightly from the applied VP voltage; typical ramp-up speeds achieved with a 1000 µF DC blocking capacitor are listed in Table 2. These times scale with the value of the capacitor.

VP Voltage	Typical Ramp Time*
8 V	2.20 seconds
12 V	1.25 seconds

* With 1000 µF DC Blocking Capacitor.

Table 2. Typical Ramp Times for Typical VP Voltages

When the device is configured for ramping (RAMP set high) and RST12 or RST34 is set low, the corresponding outputs will begin to slowly ramp down from the bias point to PGND, allowing the DC-blocking capacitor to discharge.

The ramp feature is intended for use with half-bridge outputs. For “2.1 channel” applications with stereo half-bridge and mono full-bridge (CNFG[2:0] = 001 or 101), the ramp will only be applied to OUT1 and OUT2 (the half-bridge channels); OUT3 and OUT4 (the full-bridge channel) will not ramp.

The ramp feature requires a 33 nF capacitor on the RAMP_CAP pin to VP. For applications that do not enable the ramping feature, RAMP_CAP can be connected directly to VP.

It is not necessary to complete a ramp-up/down sequence before ramping up/down again.

4.2.2 Initial Pulse Edge Delay

After RST12 or RST34 is released, the CS4412A continues to hold the corresponding power output pins in a high-impedance state until a pulse edge is sensed on a corresponding PWM input pin. This is done to prevent a possible DC output condition on the speakers if the PWM inputs are not yet modulating immediately following the release of the corresponding reset signal. This initial transition delay is independent for each input/output pin pair; each output corresponding to an inactive input will remain in a high-impedance state until its input receives a pulse edge even if other inputs are activated. The pulse edge must be from a digital low state to a digital high state. Once a pulse edge is detected, the corresponding output pin will activate and switch as dictated by the output mode configuration described in Section 4.3 on page 15 until either an error condition is detected or until its reset pin is set low.

If the outputs are configured for ramping, the CS4412A will perform a ramp-up sequence on OUT1/2 immediately following the release of RST12 and a ramp sequence on OUT3/4 immediately following the release of RST34. See Section 4.2.1 on page 13 for more information on output ramping. If a pulse edge is detected on an input before the ramp-up sequence finishes on its corresponding output pin, the CS4412A continues the ramp sequence and begins normal output operation immediately following its completion. If a pulse edge is not detected on an input by the time the ramp-up sequence has finished on its corresponding output pin, the output pin is placed into and remains in a high-impedance state until a pulse edge is detected on the corresponding input.

4.2.3 Recommended Power-Up Sequence

1. Turn on the system power.
2. Hold RST12 and RST34 low until the power supply is stable. In this state, all associated outputs are held in a high-impedance state.
3. Release RST12 and RST34 high.
4. Start the PWM modulator output.

4.2.4 Recommended Power-Down Sequence

1. Mute the logic-level PWM inputs present on IN1 - IN4 by applying 50% duty-cycle input signals.
2. Hold RST12 and RST34 low.
3. Power down the remainder of the system.

4.3 Output Mode Configuration

Each OUTx pin will switch in association with the corresponding INx pin. For most configurations, OUTx will be non-inverted from INx; however, some INx pins can be configured for internal inversion to allow one PWM input to drive both the positive and negative sides of a full-bridge output. Unused OUTx pins must have their corresponding INx pin tied to ground.

Table 3 shows the setting of the CNFG[2:0] inputs and the corresponding mode of operation. These pins should remain static during operation ($\overline{\text{RST12}}$ or $\overline{\text{RST34}}$ set high).

CNFG2	CNFG1	CNFG0	Description	Necessary Input Connections
0	0	0	Stereo Full-Bridge Tied Loads	IN1 must provide the PWM data for the first full-bridge. IN2 must be inverted from IN1 for full-bridge operation. IN3 must provide the PWM data for the second full-bridge. IN4 must be inverted from IN3 for full-bridge operation.
0	0	1	Stereo Half-Bridge & Mono Full-Bridge Tied Loads*	IN1 must provide the PWM data for the first half-bridge. IN2 must provide the PWM data for the second half-bridge. IN3 must provide the PWM data for the mono full-bridge. IN4 must be inverted from IN3 for full-bridge operation.
0	1	0	Mono Parallel Full-Bridge Tied Load	IN1 must provide the PWM data for the mono full-bridge. IN2 must be wired directly to IN1 for parallel full-bridge operation. IN3 must be inverted from IN1 for parallel full-bridge operation. IN4 must be wired to IN3 for parallel full-bridge operation.
0	1	1	Quad Half-Bridge Tied Loads	IN1 must provide the PWM data for the first half-bridge. IN2 must provide the PWM data for the second half-bridge. IN3 must provide the PWM data for the third half-bridge. IN4 must provide the PWM data for the fourth half-bridge.
1	0	0	Stereo Full-Bridge Tied Loads With Inversion	IN1 must provide the PWM data for the first full-bridge. IN2 must be wired to IN1; the CS4412A will internally invert IN2. IN3 must provide the PWM data for the second full-bridge. IN4 must be wired to IN3; the CS4412A will internally invert IN4.
1	0	1	Stereo Half-Bridge & Mono Full-Bridge Tied Loads With Inversion*	IN1 must provide the PWM data for the first half-bridge. IN2 must provide the PWM data for the second half-bridge. IN3 must provide the PWM data for the mono full-bridge. IN4 must be wired to IN3; the CS4412A will internally invert IN4.
1	1	0	Mono Parallel Full-Bridge Tied Load With Inversion	IN1 must be provided for half-bridge operation. IN2 must be wired to IN1 for parallel full-bridge operation. IN3 must be wired to IN1; the CS4412A will internally invert IN3. IN4 must be wired to IN1; the CS4412A will internally invert IN4.
1	1	1	Reserved	The input connections are not applicable.

* PWM Popguard Transient Control only affects OUT1 and OUT2.

Table 3. Output Mode Configuration Options

In Stereo Half-Bridge and Mono Full-Bridge configurations, the PWM Popguard Transient Control only affects the two half-bridge outputs, OUT1 and OUT2. The full-bridge output will not ramp regardless of the state of the RAMP pin. See Section 4.2.1 on page 13 for more details about PWM Popguard Transient Control.

4.4 Output Filters

The filter placed after the PWM outputs can greatly affect the output performance. The filter not only reduces radiated EMI (snubber filter) but also filters high frequency content from the switching output before going to the speaker (low-pass LC filter).

4.4.1 Half-Bridge Output Filter

Figure 5 shows the output filter for a half-bridge configuration. The transient-voltage suppression circuit (snubber circuit) is comprised of a capacitors (680 pF) and a resistor (5.6 Ω, 1/8 W) and should be placed as close as possible to the corresponding PWM output pin to greatly reduce radiated EMI.

Each output pin must be connected to two Schottky diodes—one to ground and one to the VP supply. These diodes should be placed within 12 mm of the corresponding OUTx pin. The requirements of this diode are:

1. Rated I_F (average rectifier forward current) is greater than or equal to 1.0 A.
2. Support up to 80°C of lead temperature with V_F drop (forward voltage) less than or equal to 480 mV at the corresponding I_F.
3. V_R (reverse voltage) is greater than or equal to 20 V.

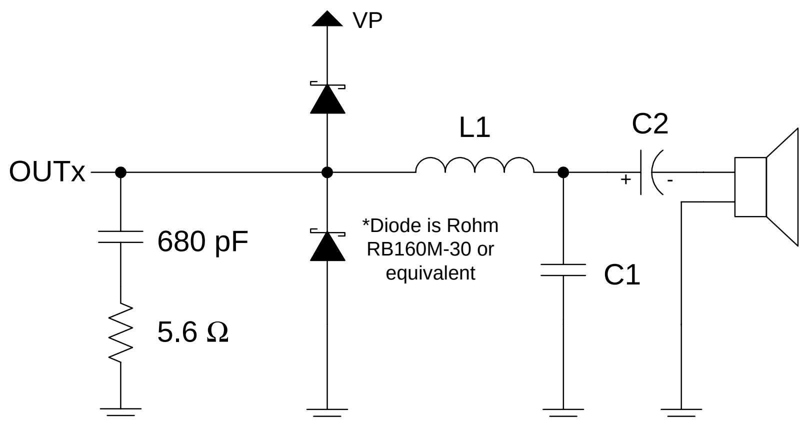


Figure 5. Output Filter - Half-Bridge

The inductor, L1, and capacitor, C1, comprise the low-pass filter. Along with the nominal load impedance of the speaker, these values set the cut-off frequency of the filter. Table 4 shows the component values for L1 and C1 based on nominal speaker (load) impedance for a corner frequency (-3 dB point) of approximately 35 kHz.

Load	L1	C1
4 Ω	22 µH	1.0 µF
6 Ω	33 µH	0.68 µF
8 Ω	47 µH	0.47 µF

Table 4. Low-Pass Filter Components - Half-Bridge

C2 is the DC-blocking capacitor. Table 5 shows the component values for C2 based on corner frequency (-3 dB point) and a nominal speaker (load) impedances of 4 Ω, 6 Ω, and 8 Ω. This capacitor should also be chosen to have a ripple current rating above the amount of current that will passed through it.

Load	Corner Frequency	C2
4 Ω	40 Hz	1000 µF
	58 Hz	680 µF
	120 Hz	330 µF
6 Ω	39 Hz	680 µF
	68 Hz	390 µF
	120 Hz	220 µF
8 Ω	42 Hz	470 µF
	60 Hz	330 µF
	110 Hz	180 µF

Table 5. DC-Blocking Capacitors Values - Half-Bridge

4.4.2 *Full-Bridge Output Filter (Stereo or Parallel)*

Figure 6 shows the output filter for a full-bridge configuration. The transient-voltage suppression circuit (snubber circuit) is comprised of a capacitor (680 pF) and a resistor (5.6 Ω) on each output pin and should be placed as close as possible to the corresponding PWM output pins to greatly reduce radiated EMI. The inductors, L1 and L2, and capacitor, C1, comprise the low-pass filter. Along with the nominal load impedance of the speaker, these values set the cutoff frequency of the filter. Table 6 shows the component values based on nominal speaker (load) impedance for a corner frequency (-3 dB point) of approximately 35 kHz.

Each output pin must be connected to two Schottky diodes—one to ground and one to the VP supply. These diodes should be placed within 12 mm of the corresponding OUTx pin. The requirements of this diode are:

1. Rated I_F (average rectifier forward current) is greater than or equal to 1.0 A.
2. Support up to 80°C of lead temperature with V_F drop (forward voltage) less than or equal to 480 mV at the corresponding I_F.
3. V_R (reverse voltage) is greater than or equal to 20 V.

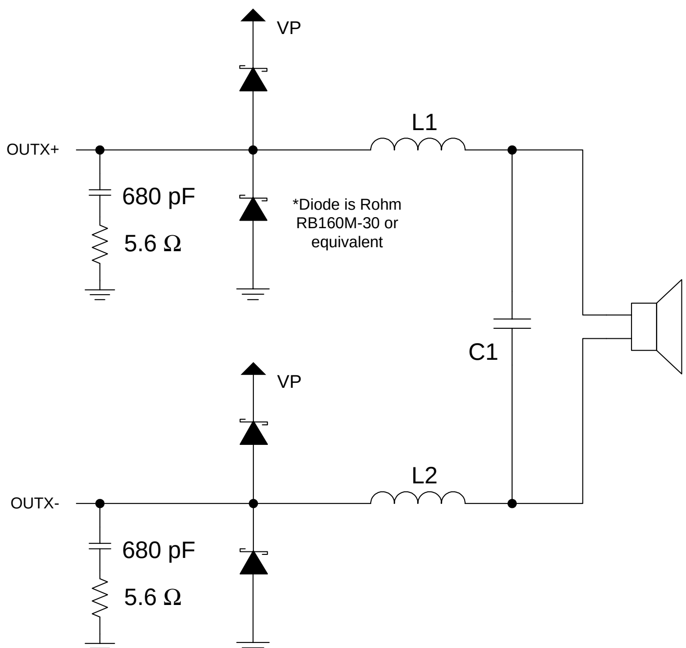


Figure 6. Output Filter - Full-Bridge

Load	L1, L2	C1
4 Ω	10 µH	1.0 µF
6 Ω	15 µH	0.47 µF
8 Ω	22 µH	0.47 µF

Table 6. Low-Pass Filter Components - Full-Bridge

4.5 Device Protection and Error Reporting

The CS4412A has built-in protection circuitry for over-current, under-voltage, and thermal warning/overload conditions. The levels of the over-current error, thermal error, and VP under-voltage trigger points are listed in the PWM Power Output Characteristics table on page 6. Automatic shut-down occurs whenever any of these preset thresholds, other than thermal warning, are crossed.

Each error and warning pin implements an active-low open-drain driver and requires an external 22 kΩ pull-up resistor for proper operation.

4.5.1 Over-Current Protection

An over-current error condition occurs if the peak output current exceeds the Over-Current Error trigger point. Over-current errors for OUT1/2 and OUT3/4 are reported on the ERROC12 and ERROC34 pins, respectively. The power output of the channel that is reporting the over-current condition will be set to high-impedance until the error condition has been removed and the reset signal for that channel has been toggled from low to high.

ERROCxy	Reported Condition
0	Over-current error on channel x or channel y
1	Operating current of channel x and y within allowable limits

Table 7. Over-Current Error Conditions

4.5.2 Thermal Warning, Thermal Error, and Under-Voltage Error

Table 8 shows the behavior of the TWR and ERRUVTE pins. When the junction temperature exceeds the junction thermal warning trigger point, the TWR pin is set low. If the junction temperature continues to increase beyond the junction thermal error trigger point, the ERRUVTE pin will be set low. If the voltage on VP falls below the VP under-voltage error trigger point, ERRUVTE will be set low.

When the thermal error or VP under-voltage trigger point is crossed, all power outputs will be set in a high-impedance state until the error condition has been removed and both the RST12 and RST34 signals have been toggled from low to high.

TWR	ERRUVTE	Reported Condition
0	0	Thermal warning and thermal error and/or under-voltage error
0	1	Thermal warning only
1	0	Under-voltage error
1	1	Junction temperature and VP voltage within normal limits

Table 8. Thermal and Under-Voltage Error Conditions

5. POWER SUPPLY, GROUNDING, AND PCB LAYOUT

5.1 Power Supply and Grounding

The CS4412A requires careful attention to power supply and grounding arrangements if its potential performance is to be realized.

Extensive use of power and ground planes, ground plane fill in unused areas, and surface mount decoupling capacitors are recommended. It is necessary to decouple the power supply by placing capacitors directly between the power and ground of the CS4412A. Decoupling capacitors should be as close to the pins of the CS4412A as possible. The lowest value ceramic capacitor should be closest to the pin and should be mounted on the same side of the board as the CS4412A to minimize inductance effects. The CRD4412A reference design demonstrates the optimum layout and power supply arrangements.

5.1.1 Integrated VD Regulator

The CS4412A includes an internal linear regulator to provide a fixed 2.5 V supply from the VD supply voltage for its internal digital logic. The LVD pin must be set to indicate the voltage present on the VD pin as shown in Table 9 below.

VD Connection	VD_REG Connection	LVD Connection
5 V Supply	Bypass Capacitors Only	VD
3.3 V Supply	Bypass Capacitors Only	GND
2.5 V Supply	VD and Bypass Capacitors	GND

Table 9. Power Supply Configuration and Settings

The output of the digital regulator is presented on the VD_REG pin and may be used to provide an external device with up to 3 mA of current at its nominal output voltage of 2.5 V.

If a nominal supply voltage of 2.5 V is used as the VD supply (see the Recommended Operating Conditions table on page 5), the VD and VD_REG must be connected to the VD supply source. In this configuration, the internal regulator is bypassed and the external supply source is used to directly drive the internal digital logic.

5.2 QFN Thermal Pad

The CS4412A is available in a compact QFN package. The underside of the QFN package reveals a large metal pad that serves as a thermal relief to provide for maximum heat dissipation. This pad must mate with an equally dimensioned copper pad on the PCB and must be electrically connected to ground. A series of thermal vias should be used to connect this copper pad to one or more larger ground planes on other PCB layers; the copper in these ground planes will act as a heat sink for the CS4412A. The CRD4412A reference design demonstrates the optimum thermal pad and via configuration.

6. PARAMETER DEFINITIONS

Dynamic Range (DYR)

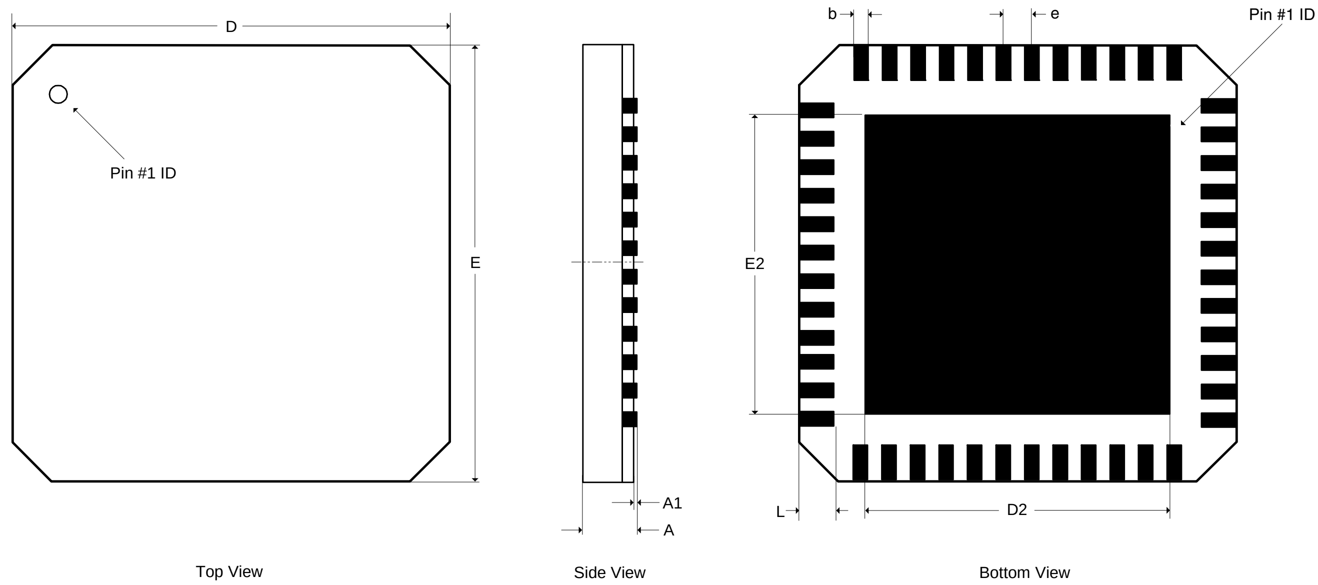
The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth, typically 20 Hz to 20 kHz. Dynamic Range is a signal-to-noise ratio measurement over the specified band width made with a -60 dBFS signal; then, 60 dB is added to the resulting measurement to refer the measurement to full-scale. This technique ensures that the distortion components are below the noise level and do not effect the measurement. This measurement technique has been accepted by the Audio Engineering Society, AES17-1991, and the Electronic Industries Association of Japan, EIAJ CP-307. Expressed in decibels.

Total Harmonic Distortion + Noise (THD+N)

The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified band width (typically 10 Hz to 20 kHz), including distortion components. Expressed in decibels. Measured at -1 and -20 dBFS as suggested in AES17-1991 Annex A.

7. PACKAGE DIMENSIONS

48L QFN (9 × 9 MM BODY) PACKAGE DRAWING



	INCHES			MILLIMETERS			NOTE
DIM	MIN	NOM	MAX	MIN	NOM	MAX	
A	--	--	0.0354	--	--	0.90	1
A1	0.0000	--	0.0020	0.00	--	0.05	1
b	0.0118	0.0138	0.0157	0.30	0.35	0.40	1,2
D		0.3543 BSC			9.00 BSC		1
D2	0.2618	0.2677	0.2736	6.65	6.80	6.95	1
E		0.3543 BSC			9.00 BSC		1
E2	0.2618	0.2677	0.2736	6.65	6.80	6.95	1
e		0.0256 BSC			0.65 BSC		1
L	0.0177	0.0217	0.0276	0.45	0.55	0.70	1

JEDEC #: MO-220

Controlling Dimension is Millimeters.

Notes:
1. Dimensioning and tolerance per ASME Y4.5M - 1994.
2. Dimensioning lead width applies to the plated terminal and is measured between 0.20 mm and 0.25 mm from the terminal tip.

8. THERMAL CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Units
Junction to Case Thermal Impedance	θ_{JC}	-	1	-	°C/Watt

8.1 Thermal Flag

This device is designed to have the metal flag on the bottom of the device soldered directly to a metal plane on the PCB. To enhance the thermal dissipation capabilities of the system, this metal plane should be coupled with vias to a large metal plane on the backside (and inner ground layer, if applicable) of the PCB.

In either case, it is beneficial to use copper fill in any unused regions inside the PCB layout, especially those immediately surrounding the CS4412A. In addition to improving in electrical performance, this practice also aids in heat dissipation.

The heat dissipation capability required of the metal plane for a given output power can be calculated as follows:

$$\theta_{CA} = [(T_{J(MAX)} - T_A) / P_D] - \theta_{JC}$$

where,
θ_{CA} = Thermal resistance of the metal plane in °C/Watt
$T_{J(MAX)}$ = Maximum rated operating junction temperature in °C, equal to 150°C
T_A = Ambient temperature in °C
P_D = RMS power dissipation of the device, equal to $0.15*P_{IN,RMS}$ or $0.177*P_{OUT,RMS}$ (assuming 85% efficiency)
θ_{JC} = Junction-to-case thermal resistance of the device in °C/Watt

9. ORDERING INFORMATION

Product	Description	Package	Pb-Free	Grade	Temp Range	Container	Order#
CS4412A	30 W Quad Half-Bridge Digital Amplifier Power Stage	48-QFN	Yes	Commercial	-10°C to +70°C	Rail	CS4412A-CNZ
						Tape and Reel	CS4412A-CNZR
CRD4412A	4 Layer / 3oz. Copper Reference Design Daughter Card	-	-	-	-	-	CRD4412A
CRD4525-Q1	4 Layer / 1oz. Copper Reference Design Main Board	-	-	-	-	-	CRD4525-Q1

10.REVISION HISTORY

Release	Changes
A1	Initial Release
A2	The following items were update: "PWM Power Output Characteristics" on page 6 Section 4.4.1 "Half-Bridge Output Filter" on page 16 Section 4.4.2 "Full-Bridge Output Filter (Stereo or Parallel)" on page 18 Section 8.1 "Thermal Flag" on page 23 Section 9. "Ordering Information" on page 23

Contacting Cirrus Logic Support

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.
To find one nearest you, go to www.cirrus.com.

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