AD9887 Evaluation Board

EVAL-AD9887EB

GENERAL DESCRIPTION

The EVAL- AD9887EB may be used both to demonstrate the performance of the AD9887 and to serve as an implementation example for design and layout of the device. To aid in real-world evaluation, the EVAL-AD9887EB was designed to be connected as easily as possible into another PCB, (such as a graphics controller board).

REQUIREMENTS

The EVAL-AD9887EB requires a 5 V power supply, a graphics signal (through the 15-pin VGA connector), and a means to program the internal chip registers. Hardware and software are provided for programming the internal chip register.

TYPICAL CONFIGURATION

In most cases, this evaluation board will be used to digitize an analog RGB graphics signal and pass the data on to another board. To do this, connect the graphics signal to the 15-pin VGA connector, supply 5 V to the board, and program the internal serial register. Supplying power and programming the chip are described later in this data sheet. The digitized data, generated clock signals, and control signals are passed off the board through the right-side connector.

POWER

The EVAL-AD9887EB contains three 3.3 V voltage regulators, which supply power to the AD9887. There are three regulators to match the three power supplies on the AD9887. Best performance can be achieved by the AD9887 when the analog supply (V_D) and the PLL supply (P_{VD}) have their own regulators. The three regulators work nominally when supplied with 5 V, but will work with a range of voltages. Power is applied to the board through the right-side connector. Typically, power is supplied from another board, as is the case when using an SXGA panel driver board.

CHIP REGISTER NAMING CONVENTION

There are several references in this data sheet to specific control registers in the AD9887. The convention used in this data sheet is to specify the register number in hex, followed by an "h" and by the bit number within the register. For example, [12h7] means Register 12, Bit 7.

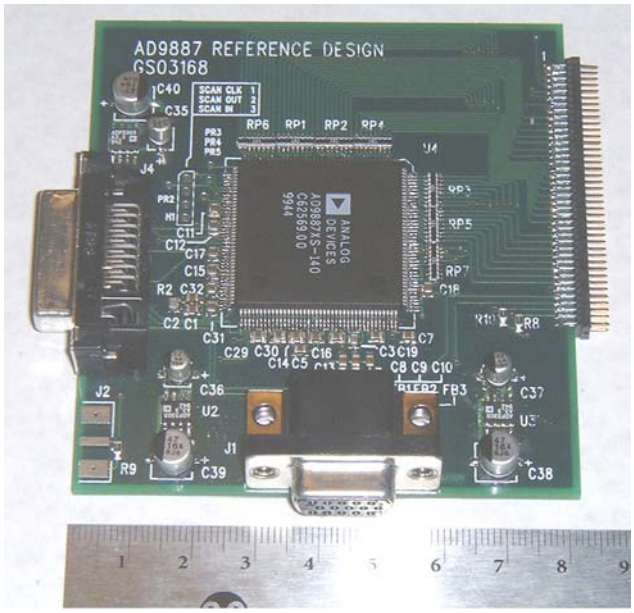

Figure 1. The AD9887 Evaluation Board (in Centimeters)

PROGRAMMING THE INTERNAL CHIP REGISTERS

Hardware and software are provided for programming the AD9887's internal registers. The hardware consists of a standard printer cable and a receiver chip located on the panel driver board. The programming signals come onto the EVAL-AD9887EB through Pins 38 and 39 on Connector J3. The software is included on the installation diskettes or CD-ROM and is described in the Setup Software section.

SETUP SOFTWARE

The Display Electronics Product Line (DEPL) evaluation software is a Visual Basic® program requiring Windows® 95 or newer. The software comes on a self-installing CD-ROM included with the evaluation board. When performing the software installation, always use the most recent Windows files (e.g., .dll or .ocx) if prompted by the install software (these files may already be on your system). The AD9887 register setup screen shown in Figure 2 is displayed at program execution after installation. The DEPL evaluation software can be used to control any DEPL AD988x device. It also includes the display interface board configuration software and a PLL divisor calculator.

Rev. 0

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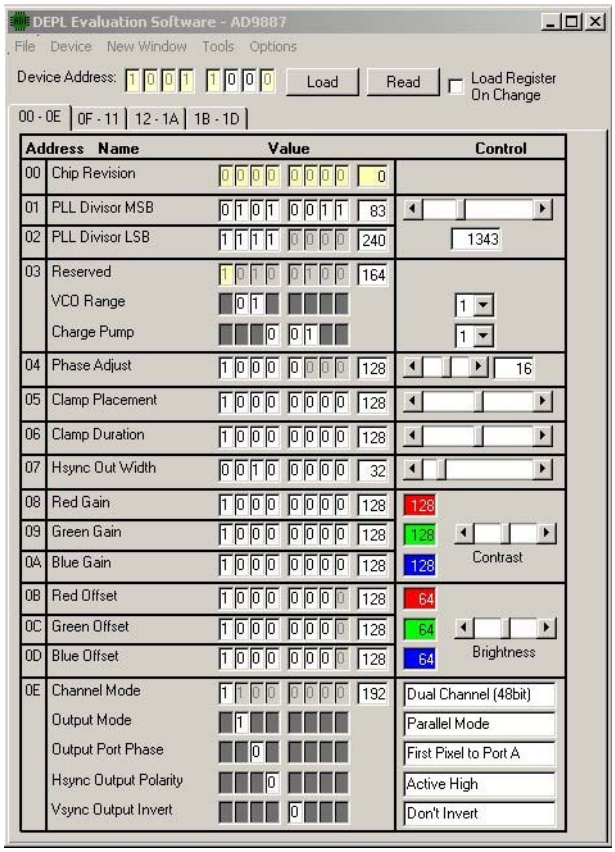

Figure 2. AD9887 Register Setup Screen

SOFTWARE CONTROL

To select the AD9887 as the DEPL evaluation software's target device, select AD9887 from the Device pull-down menu. From the AD9887 register setup screen (shown in Figure 2), the user can control every bit within the AD9887. A detailed, bit-by-bit functional description is provided in the AD9887 Data Sheet. Unless the Load Register On Change box is checked, the user must click the Load button at the top of the window in order to update the AD9887's registers. If Load Register On Change is checked, the appropriate register is updated as soon as any change is made in the window. The four tabs within this control window enable the selection of groups of registers to be displayed. The selections are 00–0E, 0F–11, 12–1A, or 1B–1D. Click on the appropriate tab to view /or control the desired register.

Software Interface

Before communication with the AD9887 registers can begin, the proper software interface must be selected. Click Device Interface from the Options pull-down menu and select either I2C Over Parallel or USB (see Figure 3). This will allow you to use either the PC's parallel printer port or a USB port to communicate with the AD9887. If using the display interface board as the hardware interface to the EVAL-AD9887EB, Jumpers W17 to W21 must be positioned appropriately for the selected interface. For USB operation, the appropriate SUB drivers must be installed. Refer to the EVAL-AD988xEB Display Interface Board documentation for details on these two items.

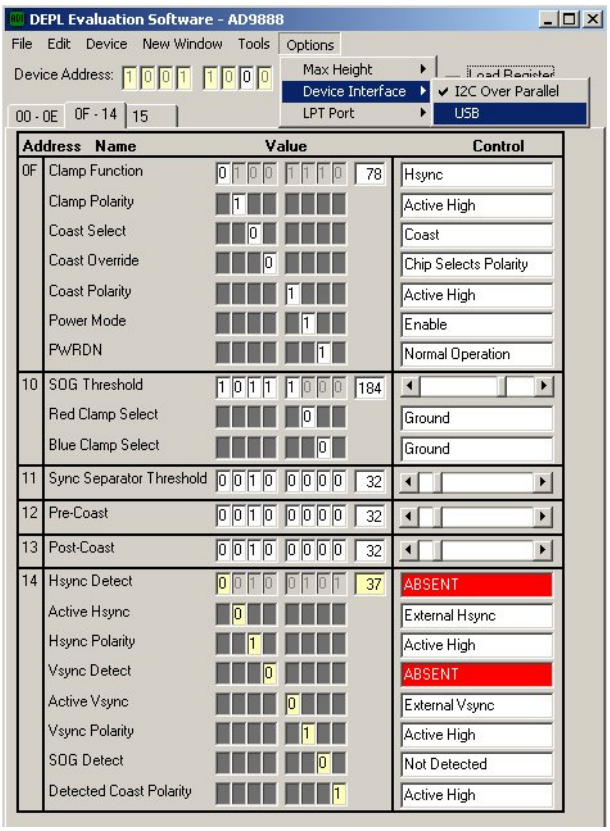

Figure 3. Choosing the Software Interface

PLL Settings

The PLL settings are contained in Registers 01h to 04h. The PLL Divisor setting (12 bits) can be set bit-by-bit (the value toggles when clicking on the bit), by setting a value (in decimal) for Registers 01h and 02h, by setting the 12-bit value (in decimal), or by moving the control bar right or left to increase or decrease the value. When changing the value using one of these methods, the change is reflected in the other three. The values are not written to the AD9887 until the Load button is clicked. The VCO Range and Charge Pump settings in Register 03h can be set bit-by-bit, by register, or by pull-down menu selection. The 5-bit Phase Adjust in Register 04h can be altered in the same manner as the PLL Divisor.

Clamp and Hsync Out Settings

Clamp Placement, Clamp Duration, and Hsync Out Width controls are contained in Registers 05h to 07h and can be changed bit-by-bit, by setting a value for the registers (decimal value), or by moving the control bar right or left to increase or decrease the value. When changing the value using one of these methods, the change is reflected in the other two. Again, unless Load Register On Change is checked, these changes are not loaded into the AD9887 until the Load button is clicked.

Gain and Offset Settings

Gain for the Red, Green, and Blue video channels is controlled via all eight bits of Registers 08h to 0Ah and can be changed bit-by-bit, by setting a value for the registers (decimal value), or by moving the control bar right or left to increase or decrease the value. The 7-bit offset control for the red, green, and blue channels is contained in Registers 0Bh to 0Dh. These can be set in the same manner as Gain, with the additional option of setting the 7-bit decimal value. Note that using the gain and offset control bars will change all three channels by the same amount, regardless of their setting. For example, if, in order to achieve color balance, the offset settings are 60, 70, and 80 for R, G, and B, respectively, then the minimum settings are 0, 10, and 20. The maximum offset settings are then 107, 117, and 127.

Interface, Sync, and Coast Select, Power-Down

Register 12h contains bits for controlling the Hsync source, Vsync source, and Coast source. To toggle a bit, simply click on it. When set to 0, Bit 0 will put the AD9887 in Power-Down mode. The bit's resulting state is reflected in the box to the right of that bit. In order to fully control the Hsync and Coast polarity of the AD9887, Bits 0 and 1 of Register 14h must also be considered. Refer to the AD9887 Data Sheet for a functional description of these bits.

SOG Control

Register13h contains bits for adjusting the Sync separator threshold. Register 16h contains bits for controlling the SOG threshold. The Sync separator threshold can be changed bit-by-bit, by setting a value for the register (decimal value), or by moving the control bar right or left to increase or decrease the value. The 5-bit (7:3) SOG threshold can be modified bit-by-bit or by changing the 5-bit (decimal) value. The resulting state of the bits is reflected in the box to the right of each bit. See the AD9887 Data Sheet for a functional description of these bits.

Status Registers

Register 11h is a read-only register that indicates the state of the autodetect circuitry for Hsync, Vsync, SOG, and DVI clock. The status of the interface selection and Hsync and Vsync source selection is also indicated. Register 15h is also a read-only register that indicates the state of the autodetect circuitry for Hsync, Vsync, and Coast Polarity. The resulting state of the bit is reflected in the box to the right of each bit. Refer to the AD9887 Data Sheet for a functional description of these bits.

Pre-Coast and Post-Coast

Registers 17h and 18h contain the bits for controlling Pre-Coast and Post-Coast. The 8-bit Pre-Coast and 8-bit Post-Coast can be modified bit-by-bit or by changing the 8-bit (decimal) value. The resolution of this adjustment is in Hsync periods. These adjustments apply to the AD9887's internal Coast function and do not alter an external Coast signal. Refer to the AD9887 Data Sheet for a functional description of these bits.

Reserved Registers

In order for the AD9887 to operate correctly in all modes, the reserved registers should be set as follows:

Register	Setting
1Ah	41h
1Bh	00h
1Ch	6Fh

OTHER SOFTWARE FEATURES

Display Interface Configuration

The display interface board requires a software interface. This software is installed when the DEPL evaluation software is installed and can be accessed via by selecting Display Interface Board from the Tools pull-down menu. Refer to the EVAL-AD988xEB Display Interface Board documentation for details on using this software.

PLL Divisor Calculator

A PLL divisor calculator, which provides a quick and easy way to calculate the analog PLL Divisor based on the input horizontal and pixel frequencies, is also available in the Tools pull-down menu. Select PLL Divisor Calculator from the Tools pull-down menu and the PLL Divisor Calculator will open up in a new window (see Figure 4).

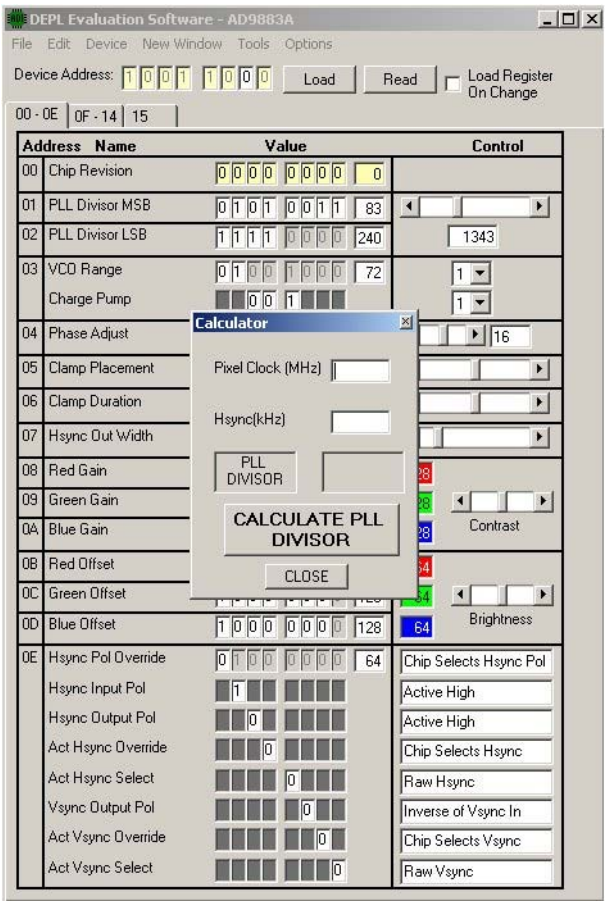

Figure 4. PLL Divisor Calculator

SCHEMATICS AND LAYOUT

The schematics and layout for this board are included in separate files, which can be found on Installation Disk 2 or on the CD-ROM.

CONTACT INFORMATION

If you have questions or would like more information, email us directly at flatpanel_apps@analog.com, visit our website at http://www.analog.com/flatpanel, or call the Analog Devices help line at 1-800-AnalogD (1-800-262-5643).

Table 1. Sample Settings for the EVAL-AD9887EB

PLL Timing Chart							
		Horizontal Sync					
Mode	Resolution	Nominal Frequency (kHz)	Polarity	PLL Divider[1] N + 1	Nominal Pixel Clock (MHz)	VCO Range[2]	Charge Pump Current[2]
VGA	640 × 480 @ 60 Hz	31.469	N	800	25.175	00	000
	640 × 480 @ 72 Hz	37.861	N	832	31.500	00	000
	640 × 480 @ 75 Hz	37.500	N	840	31.500	00	000
	640 × 480 @ 85 Hz	43.269	N	832	36.000	00	001
SVGA	800 × 600 @ 56 Hz	35.156	N/P	1024	36.000	00	001
	800 × 600 @ 60 Hz	37.879	P	1056	40.000	00	001
	800 × 600 @ 72 Hz	48.077	P	1040	50.000	00	010
	800 × 600 @ 75 Hz	46.875	P	1056	49.500	00	001
	800 × 600 @ 85 Hz	53.674	P	1048	56.250	01	010
XGA	1024 × 768 @ 60 Hz	48.363	N	1344	65.000	01	010
	1024 × 768 @ 70 Hz	56.476	N	1328	75.000	01	011
	1024 × 768 @ 75 Hz	60.023	P	1312	78.750	01	011
	1024 × 768 @ 80 Hz	64.000	P	1336	85.500	10	011
	1024 × 768 @ 85 Hz	68.677	P	1376	94.50	10	011
SXGA	1280 × 1024 @ 60 Hz	60.020	P	1688	108.000	10	011
	1280 × 1024 @ 75 Hz	79.976	P	1688	135.000	11	100

[1] The PLL divisor to the chip should be an odd integer. Chip divide ratio = Input N + offset of 1.
[2] The VCO range and charge pump current settings are preliminary and may need slight adjustments.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

ORDERING GUIDE

Model	Package Description
AD9887/PCB	Evaluation Board

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