



512K × 8 CMOS FLASH MEMORY WITH LPC INTERFACE

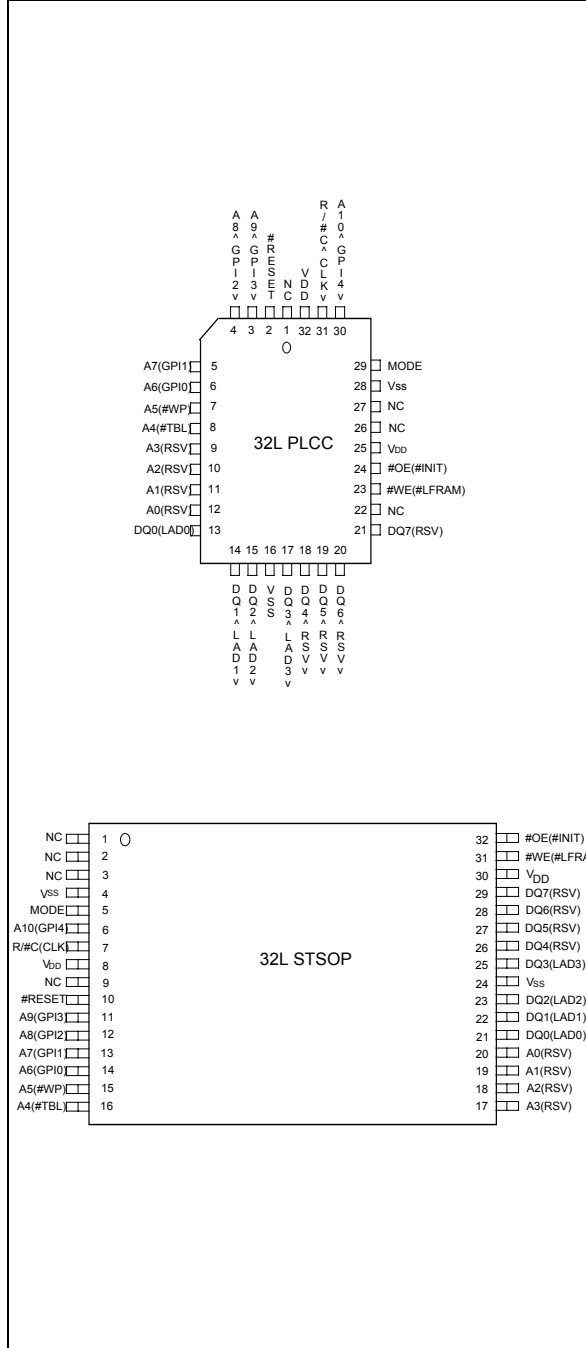
1. GENERAL DESCRIPTION

The W39V040A is a 4-megabit, 3.3-volt only CMOS flash memory organized as 512K × 8 bits. For flexible erase capability, the 4Mbits of data are divided into 8 uniform sectors of 64 Kbytes, which are composed of 16 smaller even pages with 4 Kbytes. The device can be programmed and erased in-system with a standard 3.3V power supply. A 12-volt VPP is not required. The unique cell architecture of the W39V040A results in fast program/erase operations with extremely low current consumption. This device can operate at two modes, Programmer bus interface mode and LPC bus interface mode. As in the Programmer interface mode, it acts like the traditional flash but with a multiplexed address inputs. But in the LPC interface mode, this device complies with the Intel LPC specification. The device can also be programmed and erased using standard EPROM programmers.

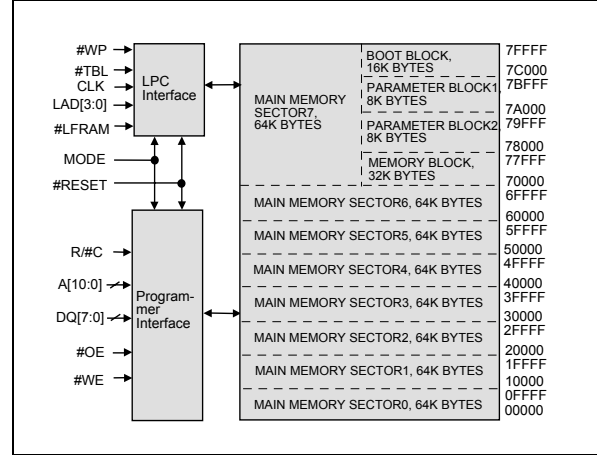
2. FEATURES

- Single 3.3-volt Operations:
 - 3.3-volt Read
 - 3.3-volt Erase
 - 3.3-volt Program
- Fast Program Operation:
 - Byte-by-Byte programming: 35 μS (typ.)
- Fast Erase Operation:
 - Chip erase 100 mS (max.)
 - Sector erase 25 mS (max.)
 - Page erase 25 mS (max.)
- Fast Read access time: Tkq 11 nS
- Endurance: 10K cycles (typ.)
- Twenty-year data retention
- 8 Even sectors with 64K bytes each, which is composed of 16 flexible pages with 4K bytes
- Any individual sector or page can be erased
- Hardware protection:
 - Optional 16K byte or 64K byte Top Boot Block with lockout protection
 - #TBL & #WP support the whole chip hardware protection
- Flexible 4K-page size can be used as Parameter Blocks
- Low power consumption
 - Active current: 12.5 mA (typ. for LPC mode)
- Automatic program and erase timing with internal VPP generation
- End of program or erase detection
 - Toggle bit
 - Data polling
- Latched address and data
- TTL compatible I/O
- Available packages: 32L PLCC, 32L STSOP

3. PIN CONFIGURATIONS



4. BLOCK DIAGRAM



5. PIN DESCRIPTION

| SYM. | INTERFACE | | PIN NAME |
|----------|-----------|-----|--------------------------|
| | PGM | LPC | |
| MODE | * | * | Interface Mode Selection |
| #RESET | * | * | Reset |
| #INIT | | * | Initialize |
| #TBL | | * | Top Boot Block Lock |
| #WP | | * | Write Protect |
| CLK | | * | CLK Input |
| GPI[4:0] | | * | General Purpose Inputs |
| ID[3:0] | | * | Identification Inputs |
| LAD[3:0] | | * | Address/Data Inputs |
| #LFRAM | | * | LPC Cycle Initial |
| R/#C | * | | Row/Column Select |
| A[10:0] | * | | Address Inputs |
| DQ[7:0] | * | | Data Inputs/Outputs |
| #OE | * | | Output Enable |
| #WE | * | | Write Enable |
| VDD | * | * | Power Supply |
| VSS | * | * | Ground |
| RSV | * | * | Reserve Pins |
| NC | * | * | No Connection |



6. FUNCTIONAL DESCRIPTION

Interface Mode Selection And Description

This device can be operated in two interface modes, one is Programmer interface mode, and the other is LPC interface mode. The MODE pin of the device provides the control between these two interface modes. These interface modes need to be configured before power up or return from #RESET. When MODE pin is set to high position, the device is in the Programmer mode; while the MODE pin is set to low position, it is in the LPC mode. In Programmer mode, this device just behaves like traditional flash parts with 8 data lines. But the row and column address inputs are multiplexed. The row address is mapped to the higher internal address A[18:11]. And the column address is mapped to the lower internal address A[10:0]. For LPC mode, It complies with the LPC Interface Specification Revision 1.0. Through the LAD[3:0] and #LFRAM to communicate with the system chipset .

Read(Write) Mode

In Programmer interface mode, the read(write) operation of the W39V040A is controlled by #OE (#WE). The #OE (#WE) is held low for the host to obtain(write) data from(to) the outputs(inputs). #OE is the output control and is used to gate data from the output pins. The data bus is in high impedance state when #OE is high. As in the LPC interface the "bit 1 of CYCLE TYPE+DIR" determines mode, the read or write. Refer to the timing waveforms for further details.

Reset Operation

The #RESET input pin can be used in some application. When #RESET pin is at high state, the device is in normal operation mode. When #RESET pin is at low state, it will halt the device and all outputs will be at high impedance state. As the high state re-asserted to the #RESET pin, the device will return to read or standby mode, it depends on the control signals.

Boot Block Operation and Hardware Protection at Initial - #TBL and #WP

There are two alternatives to set the boot block. Either 16K-byte or 64K-byte in the top location of this device can be locked as boot block, which can be used to store boot codes. It is located in the last 16K/64K bytes of the memory with the address range from 7C000(hex)/70000(hex) to 7FFFF(hex).

See Command Codes for Boot Block Lockout Enable for the specific code. Once this feature is set the data for the designated block cannot be erased or programmed (programming lockout), other memory locations can be changed by the regular programming method.

Besides the software method, there is a hardware method to protect the top boot block and other sectors. Before power on programmer, tie the #TBL pin to low state and then the top boot block will not be programmed/erased. If #WP pin is tied to low state before power on, the other sectors will not be programmed/erased.

In order to detect whether the boot block feature is set on or not, users can perform software command sequence: enter the product identification mode (see Command Codes for Identification/Boot Block Lockout Detection for specific code), and then read from address 7FFF2(hex). If the DQ0/DQ1 output data is "1," the 64Kbytes/16Kbytes boot block programming lockout feature will be activated; if the DQ0/DQ1 output data is "0," the lockout feature will be inactivated and the boot block can be erased/programmed. But the hardware protection will override the software lock setting, i.e., while the #TBL pin is trapped at low state, the top boot block cannot be programmed/erased whether the output data, DQ0/DQ1 at the address 7FFF2, is "0" or "1". The #TBL will lock the whole 64Kbytes top boot



block, it will not partially lock the 16Kbytes boot block. You can check the DQ2/DQ3 at the address 7FFF2 to see whether the #TBL/#WP pin is in low or high state. If the DQ2 is "0", it means the #TBL pin is tied to high state. In such condition, whether boot block can be programmed/erased or not will depend on software setting. On the other hand, if the DQ2 is "1", it means the #TBL pin is tied to low state, then boot block is locked no matter how the software is set. Like the DQ2, the DQ3 inversely mirrors the #WP state. If the DQ3 is "0", it means the #WP pin is in high state, then all the sectors except the boot block can be programmed/erased. On the other hand, if the DQ3 is "1", then all the sectors except the boot block are programmed/erased inhibited.

To return to normal operation, perform a three-byte command sequence (or an alternate single-byte command) to exit the identification mode. For the specific code, see Command Codes for Identification/Boot Block Lockout Detection.

Chip Erase Operation

The chip-erase mode can be initiated by a six-byte command sequence. After the command loading cycle, the device enters the internal chip erase mode, which is automatically timed and will be completed within fast 100 mS (max). The host system is not required to provide any control or timing during this operation. If the boot block programming lockout is activated, only the data in the other memory sectors will be erased to FF(hex) while the data in the boot block will not be erased (remains as the same state before the chip erase operation). The entire memory array will be erased to FF(hex) by the chip erase operation if the "boot block programming lockout feature" is not activated. The device will automatically return to normal read mode after the erase operation completed. Data polling and/or Toggle Bits can be used to detect end of erase cycle.

Sector/Page Erase Operation

Sector/page erase is a six-bus cycles operation. There are two "unlock" write cycles, followed by writing the "set-up" command. Two more "unlock" write cycles then follows by the sector/page erase command. The sector/page address (any address location within the desired sector/page) is latched on the rising edge of R/C, while the command (30H/50H) is latched on the rising edge of #WE in programmer mode.

Sector/page erase does not require the user to program the device prior to erase. When erasing a sector/page or sectors/pages the remaining unselected sectors/pages are not affected. The system is not required to provide any controls or timings during these operations.

The automatic sector/page erase begins after the erase command is completed, right from the rising edge of the #WE pulse for the last sector/page erase command pulse and terminates when the data on DQ7, Data Polling, is "1" at which time the device returns to the read mode. Data Polling must be performed at an address within any of the sectors/pages being erased.

Refer to the Erase Command flow Chart using typical command strings and bus operations.

Program Operation

The W39V040A is programmed on a byte-by-byte basis. Program operation can only change logical data "1" to logical data "0." The erase operation, which changed entire data in main memory and/or boot block from "0" to "1", is needed before programming.

The program operation is initiated by a 4-byte command cycle (see Command Codes for Byte Programming). The device will internally enter the program operation immediately after the byte-program command is entered. The internal program timer will automatically time-out (50 μ S max. - TBP) once it is completed and then return to normal read mode. Data polling and/or Toggle Bits can be used to detect end of program cycle.



Hardware Data Protection

The integrity of the data stored in the W39V040A is also hardware protected in the following ways:

- (1) Noise/Glitch Protection: A #WE pulse of less than 15 nS in duration will not initiate a write cycle.
- (2) VDD Power Up/Down Detection: The programming and read operation is inhibited when VDD is less than 1.5V typical.
- (3) Write Inhibit Mode: Forcing #OE low or #WE high will inhibit the write operation. This prevents inadvertent writes during power-up or power-down periods.
- (4) VDD power-on delay: When VDD has reached its sense level, the devices will automatically time-out 5 mS before any write (erase/program) operation.

Data Polling (DQ7)- Write Status Detection

The W39V040A includes a data polling feature to indicate the end of a program or erase cycle. When the W39V040A is in the internal program or erase cycle, any attempts to read DQ7 of the last byte loaded will receive the complement of the true data. Once the program or erase cycle is completed, DQ7 will show the true data. Note that DQ7 will show logical "0" during the erase cycle, and become logical "1" or true data when the erase cycle has been completed.

Toggle Bit (DQ6)- Write Status Detection

In addition to data polling, the W39V040A provides another method for determining the end of a program cycle. During the internal program or erase cycle, any consecutive attempts to read DQ6 will produce alternating 0's and 1's. When the program or erase cycle is completed, this toggling between 0's and 1's will stop. The device is then ready for the next operation.

Multi-Chip Operation

Multiple devices can be wired on the single LPC bus. There are four ID pins can be used to support up to 16 devices. But in order not to violate the BIOS ROM memory space defined by Intel, Winbond W39V040A will only used 3 ID pins to allow up to 8 devices, 4Mbytes for BIOS code and 4Mbytes for registers memory space.

Register

There are two kinds of registers on this device, the General Purpose Input Registers and Product Identification Registers. Users can access these registers through respective address in the 4Gbytes memory map. There are detail descriptions in the sections below.

General Purpose Inputs Register

This register reads the states of GPI[4:0] pins on the W39V040A. This is a pass-through register, which can be read via memory address FFBxE100(hex). The "x" in the addresses represents the ID [3:0] pin straps. Since it is pass-through register, there is no default value.



GPI Register

| BIT | FUNCTION |
|-------|----------------------|
| 7 – 5 | Reserved |
| 4 | Read GPI4 pin status |
| 3 | Read GPI3 pin status |
| 2 | Read GPI2 pin status |
| 1 | Read GPI1 pin status |
| 0 | Read GPI0 pin status |

Product Identification Registers

There is an alternative software method (six commands bytes) to read out the Product Identification in both the Programmer interface mode and the LPC interface mode. Thus, the programming equipment can automatically matches the device with its proper erase and programming algorithms.

In the software access mode, a six-byte (or JEDEC 3-byte) command sequence can be used to access the product ID for programmer interface mode. A read from address 0000(hex) outputs the manufacturer code, DA(hex). A read from address 0001(hex) outputs the device code, 3D(hex).” The product ID operation can be terminated by a three-byte command sequence or an alternate one-byte command sequence (see Command Definition table for detail).

Identification Input Pins ID[3:0]

These pins are part of mechanism that allows multiple parts to be used on the same bus. The boot device should be 0000b. And all the subsequent parts should use the up-count strapping. Note that a 1M byte ROM will occupy two Ids. For example: a 1MByte ROM's ID is 0000b, the next ROM's ID is 0010b. These pins all are pulled down with internal resistor.

Memory Address Map

There are 8M bytes space reserved for BIOS Addressing. The 8M bytes are mapped into a single 4M system address by dividing the ROMs into two 4M byte pages. For accessing the 4M byte BIOS storage space, the ID[2:0] pins are inverted in the ROM and are compared to address lines [21:19]. ID[3] can be used as like active low chip-select pin.

The 32Mbit address space is as below:

| BLOCK | LOCK | ADDRESS RANGE |
|------------------|------|--------------------------|
| 4M Byte BIOS ROM | None | FFFF, FFFFh: FFC0, 0000h |

The ROM responds to 640K (top 512K + bottom 128K) byte pages based on the ID pins strapping according to the following table:

| ID[2:0] PINS | ROM BASED ADDRESS RANGE |
|--------------|--|
| 000 | FFFF, FFFFh: FFF8, 0000h & 000F, FFFFh: 000E, 00000h |
| 001 | FFF7, FFFFh: FFF0, 0000h |
| 010 | FFEF, FFFFh: FFE8, 0000h |
| 011 | FFE7, FFFFh: FFE0, 0000h |



Continued

| | |
|-----|--------------------------|
| 100 | FFDF, FFFFh: FFD8, 0000h |
| 101 | FFD7, FFFFh: FFD0, 0000h |
| 110 | FFCF, FFFFh: FFC8, 0000h |
| 111 | FFC7, FFFFh: FFC0, 0000h |

Table of Operating Modes

Operating Mode Selection - Programmer Mode

| MODE | PINS | | | | |
|----------------|-----------------|-----------------|-----------------|---------|-------------|
| | #OE | #WE | #RESET | ADDRESS | DQ. |
| Read | V _{IL} | V _{IH} | V _{IH} | AIN | Dout |
| Write | V _{IH} | V _{IL} | V _{IH} | AIN | Din |
| Standby | X | X | V _{IL} | X | High Z |
| Write Inhibit | V _{IL} | X | V _{IH} | X | High Z/DOUT |
| | X | V _{IH} | V _{IH} | X | High Z/DOUT |
| Output Disable | V _{IH} | X | V _{IH} | X | High Z |

Operating Mode Selection - LPC Mode

Operation modes in LPC interface mode are determined by "cycle type" when it is selected. When it is not selected, its outputs (LAD[3:0]) will be disable. Please reference to the "Standard LPC Memory Cycle Definition".

Standard LPC Memory Cycle Definition

| FIELD | NO. OF CLOCKS | DESCRIPTION |
|------------------|---------------|--|
| Start | 1 | "0000b" appears on LPC bus to indicate the initial |
| Cycle Type & Dir | 1 | "010Xb" indicates memory read cycle; while "011xb" indicates memory write cycle. "X" mean don't have to care. |
| TAR | 2 | Turned Around Time |
| Addr. | 8 | Address Phase for Memory Cycle. LPC supports the 32 bits address protocol. The addresses transfer most significant nibble first and least significant nibble last. (i.e. Address[31:28] on LAD[3:0] first, and Address[3:0] on LAD[3:0] last.) |
| Sync. | N | Synchronous to add wait state. "0000b" means Ready, "0101b" means Short Wait, "0110b" means Long Wait, "1001b" for DMA only, "1010b" means error, other values are reserved. |
| Data | 2 | Data Phase for Memory Cycle. The data transfer least significant nibble first and most significant nibble last. (i.e. DQ[3:0] on LAD[3:0] first, then DQ[7:4] on LAD[3:0] last.) |

Table of Command Definition

| COMMAND DESCRIPTION | NO. OF Cycles | 1ST CYCLE | 2ND CYCLE | 3RD CYCLE | 4TH CYCLE | 5TH CYCLE | 6TH CYCLE |
|---|------------------|----------------------------------|------------|------------|---------------------------------|------------|----------------------|
| | | Addr. Data | Addr. Data | Addr. Data | Addr. Data | Addr. Data | Addr. Data |
| Read | 1 | A _{IN} D _{OUT} | | | | | |
| Chip Erase | 6 | 5555 AA | 2AAA 55 | 5555 80 | 5555 AA | 2AAA 55 | 5555 10 |
| Sector Erase | 6 | 5555 AA | 2AAA 55 | 5555 80 | 5555 AA | 2AAA 55 | SA ⁽³⁾ 30 |
| Page Erase | 6 | 5555 AA | 2AAA 55 | 5555 80 | 5555 AA | 2AAA 55 | PA ⁽⁴⁾ 50 |
| Byte Program | 4 | 5555 AA | 2AAA 55 | 5555 A0 | A _{IN} D _{IN} | | |
| Top Boot Block Lockout – 64K/16KByte | 6 | 5555 AA | 2AAA 55 | 5555 80 | 5555 AA | 2AAA 55 | 5555 40/70 |
| Product ID Entry | 3 | 5555 AA | 2AAA 55 | 5555 90 | | | |
| Product ID Exit ⁽¹⁾ | 3 | 5555 AA | 2AAA 55 | 5555 F0 | | | |
| Product ID Exit ⁽¹⁾ | 1 | XXXX F0 | | | | | |

Notes:

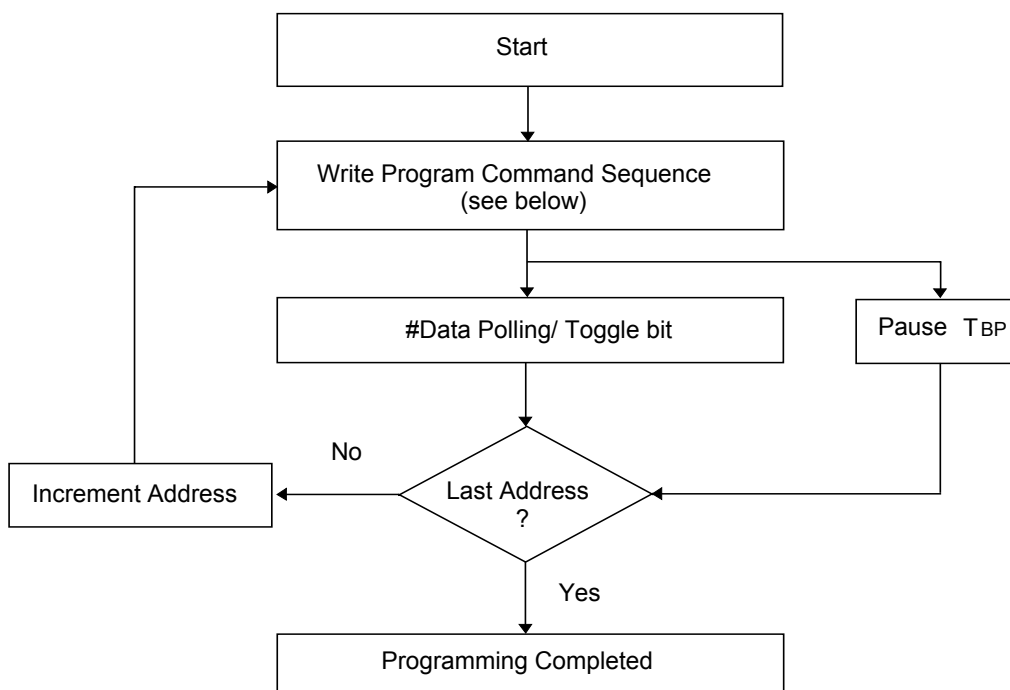
1. The cycle means the write command cycle not the LPC clock cycle.
2. The Column Address / Row Address are mapped to the Low / High order Internal Address. i.e. Column Address A[10:0] are mapped to the internal A[10:0], Row Address A[7:0] are mapped to the internal A[18:11]
3. Address Format: A14 – A0 (Hex); Data Format: DQ7 – DQ0 (Hex)
4. Either one of the two Product ID Exit commands can be used.
5. SA: Sector Address

| | |
|--|--------------------------------|
| SA = 7XXXXh for Unique Sector7 (Boot Sector) | SA = 3XXXXh for Unique Sector3 |
| SA = 6XXXXh for Unique Sector6 | SA = 2XXXXh for Unique Sector2 |
| SA = 5XXXXh for Unique Sector5 | SA = 1XXXXh for Unique Sector1 |
| SA = 4XXXXh for Unique Sector4 | SA = 0XXXXh for Unique Sector0 |

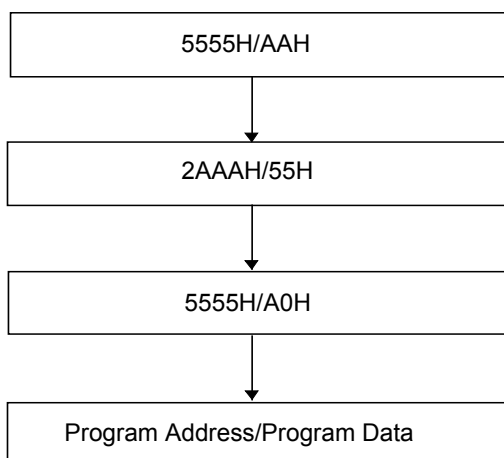
6. PA: Page Address

| | | | | | | | |
|-------------------------------------|------------|------------|------------|------------|------------|------------|------------|
| PA = 7FXXXh for Page 15 in Sector 7 | PA = | PA = | PA = | PA = | PA = | PA = | PA = |
| PA = 7EXXXh for Page 14 in Sector 7 | 6FXXXh | 5FXXXh | 4FXXXh | 3FXXXh | 2FXXXh | 1FXXXh | 0FXXXh |
| PA = 7DXXXh for Page 13 in Sector 7 | to | to | to | to | to | to | to |
| PA = 7CXXXh for Page 12 in Sector 7 | 60XXXh | 50XXXh | 40XXXh | 30XXXh | 20XXXh | 10XXXh | 00XXXh |
| PA = 7BXXXh for Page 11 in Sector 7 | for | for | for | for | for | for | for |
| PA = 7AXXXh for Page 10 in Sector 7 | Page 15 | Page 15 | Page 15 | Page 15 | Page 15 | Page 15 | Page 15 |
| PA = 79XXXh for Page 9 in Sector 7 | to | to | to | to | to | to | to |
| PA = 78XXXh for Page 8 in Sector 7 | Page 0 | Page 0 | Page 0 | Page 0 | Page 0 | Page 0 | Page 0 |
| PA = 77XXXh for Page 7 in Sector 7 | In | In | In | In | In | In | In |
| PA = 76XXXh for Page 6 in Sector 7 | Sector 6 | Sector 5 | Sector 4 | Sector 3 | Sector 2 | Sector 1 | Sector 0 |
| PA = 75XXXh for Page 5 in Sector 7 | (Reference | (Reference | (Reference | (Reference | (Reference | (Reference | (Reference |
| PA = 74XXXh for Page 4 in Sector 7 | to the | to the | to the | to the | to the | to the | to the |
| PA = 73XXXh for Page 3 in Sector 7 | first | first | first | first | first | first | first |
| PA = 72XXXh for Page 2 in Sector 7 | column) | column) | column) | column) | column) | column) | column) |
| PA = 71XXXh for Page 1 in Sector 7 | | | | | | | |
| PA = 70XXXh for Page 0 in Sector 7 | | | | | | | |

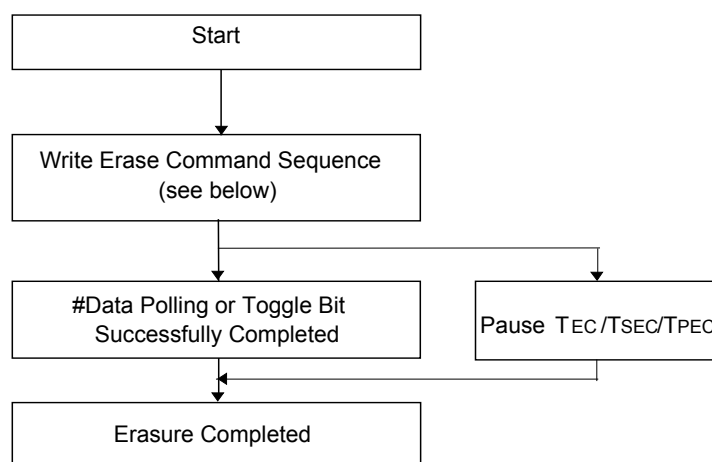
Embedded Programming Algorithm



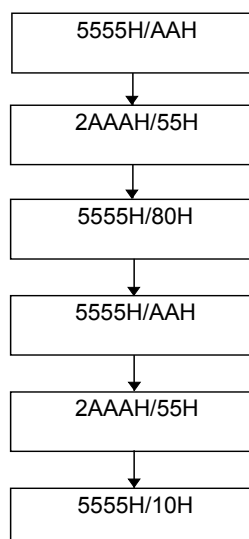
Program Command Sequence (Address/Command):



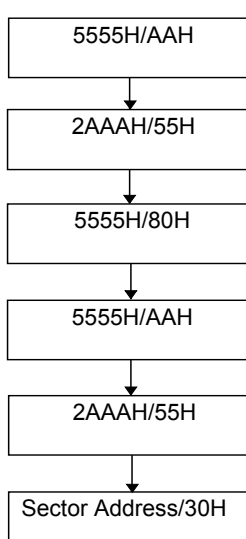
Embedded Erase Algorithm



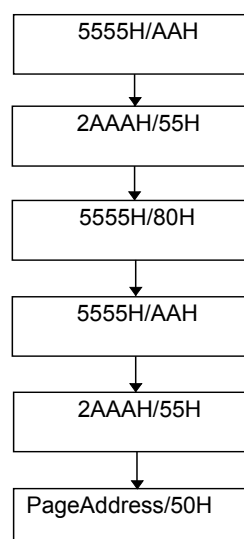
Chip Erase Command Sequence (Address/Command):



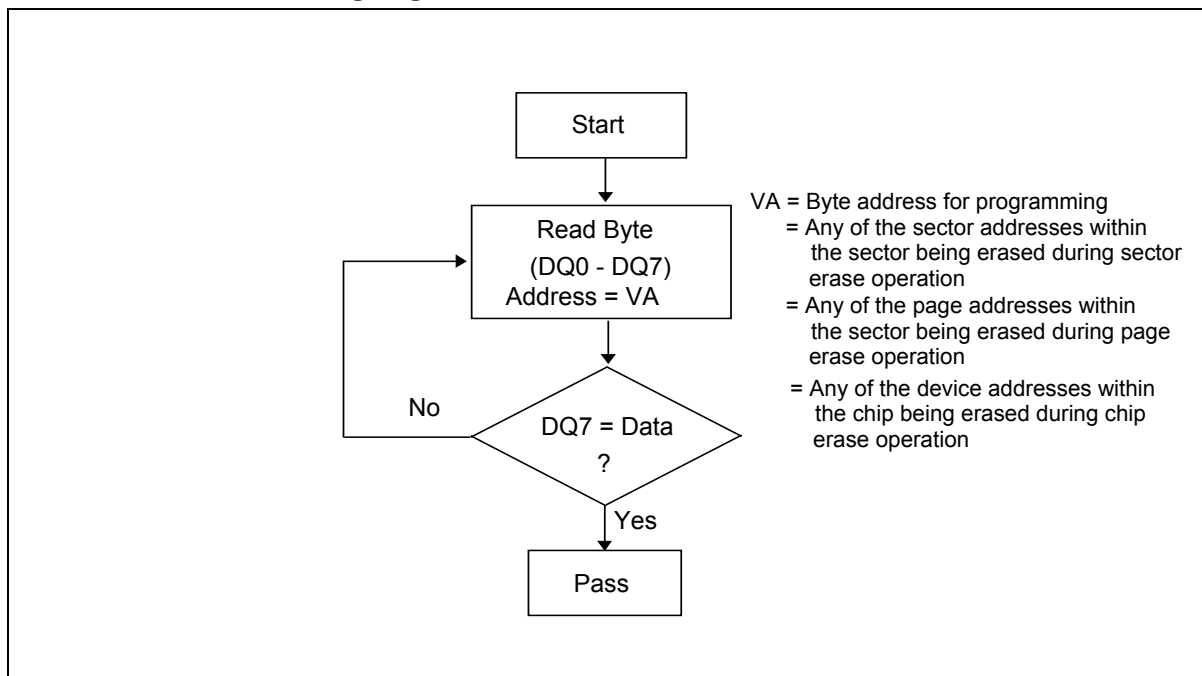
Individual Sector Erase Command Sequence (Address/Command):



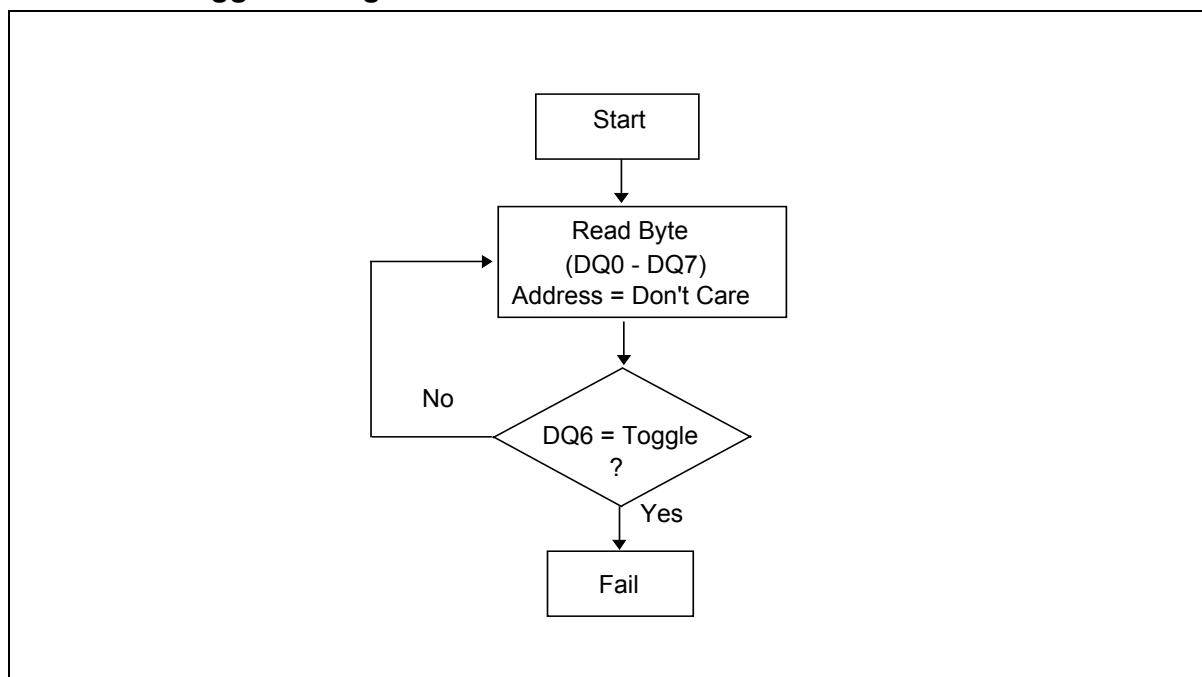
Individual Page Erase Command Sequence (Address/Command):



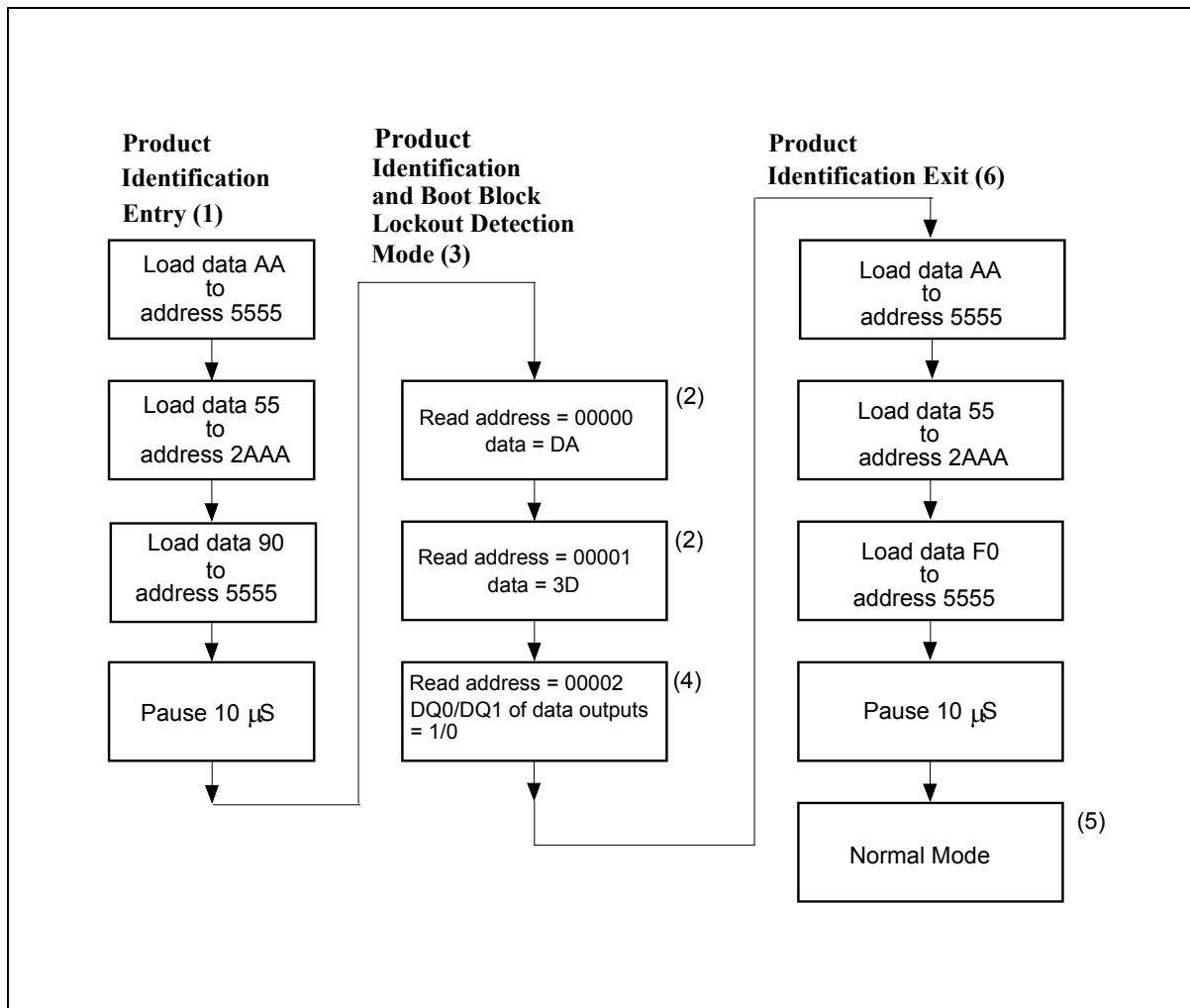
Embedded #Data Polling Algorithm



Embedded Toggle Bit Algorithm



Software Product Identification and Boot Block Lockout Detection Acquisition Flow

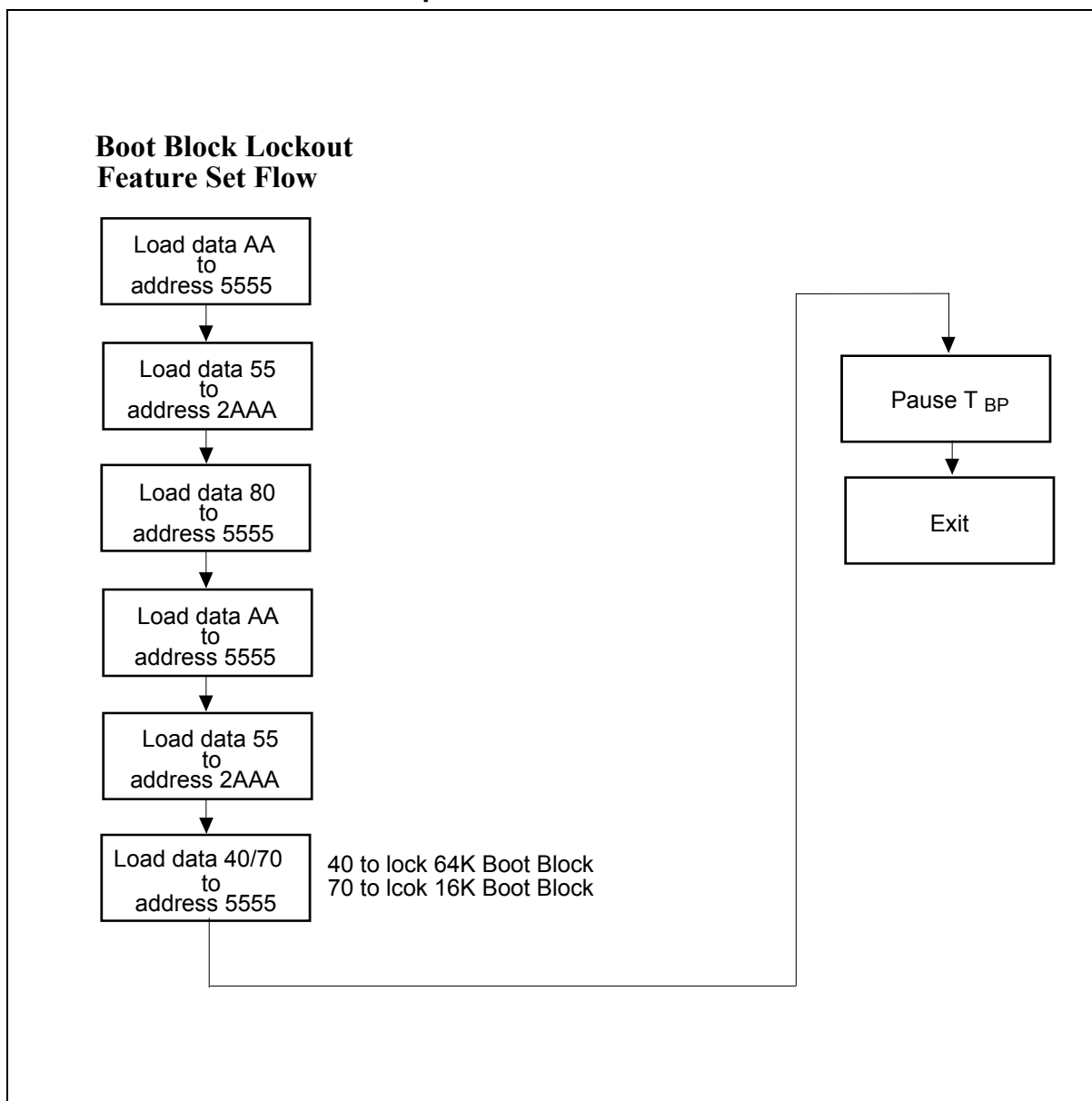


Notes for software product identification/boot block lockout detection:

- (1) Data Format: DQ7 – DQ0 (Hex); Address Format: A14 – A0 (Hex)
- (2) A1 – A18 = V_{IL}; manufacture code is read for A0 = V_{IL}; device code is read for A0 = V_{IH}.
- (3) The device does not remain in “identification and boot block lockout detection” mode if power down.
- (4) The DQ[3:0] to indicate the sectors protect status as below:

| | DQ0 | DQ1 | DQ2 | DQ3 |
|---|--|--|--|--|
| 0 | 64Kbytes Boot Block Unlocked by Software | 16Kbytes Boot Block Unlocked by Software | 64Kbytes Boot Block Unlocked by #TBL hardware trapping | Whole Chip Unlocked by #WP hardware trapping Except Boot Block |
| 1 | 64Kbytes Boot Block Locked by Software | 16Kbytes Boot Block Locked by Software | 64Kbytes Boot Block Locked by #TBL hardware trapping | Whole Chip Locked by #WP hardware trapping Except Boot Block |

- (5) The device returns to standard operation mode.
- (6) Optional 1-write cycle (write F0 hex at XXXX address) can be used to exit the “product identification/boot block lockout detection.”

Boot Block Lockout Enable Acquisition Flow



7. DC CHARACTERISTICS

Absolute Maximum Ratings

| PARAMETER | RATING | UNIT |
|---|------------------|------|
| Power Supply Voltage to Vss Potential | -0.5 to +4.6 | V |
| Operating Temperature | 0 to +70 | °C |
| Storage Temperature | -65 to +150 | °C |
| D.C. Voltage on Any Pin to Ground Potential | -0.5 to VDD +0.5 | V |
| Transient Voltage (<20 nS) on Any Pin to Ground Potential | -1.0 to VDD +0.5 | V |

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

Programmer Interface Mode DC Operating Characteristics

(VDD = 3.3V ± 0.3V, VSS = 0V, TA = 0 to 70° C)

| PARAMETER | SYM. | TEST CONDITIONS | LIMITS | | | UNIT |
|------------------------|------|---|--------|------|----------|------|
| | | | MIN. | TYP. | MAX. | |
| Power Supply Current | ICC | In Read or Write mode, all DQs open Address inputs = 3.0V/0V, at f = 3 MHz | - | 10 | 20 | mA |
| Input Leakage Current | ILI | VIN = VSS to VDD | - | - | 90 | μA |
| Output Leakage Current | ILO | VOUT = VSS to VDD | - | - | 90 | μA |
| Input Low Voltage | VIL | - | -0.3 | - | 0.8 | V |
| Input High Voltage | VIH | - | 2.0 | - | VDD +0.5 | V |
| Output Low Voltage | VOL | IOL = 2.1 mA | - | - | 0.45 | V |
| Output High Voltage | VOH | IOH = -0.1mA | 2.4 | - | - | V |



LPC Interface Mode DC Operating Characteristics

(V_{DD} = 3.3V ± 0.3V, V_{SS} = 0V, T_A = 0 to 70° C)

| PARAMETER | SYM. | TEST CONDITIONS | LIMITS | | | UNIT |
|---------------------------------|------------------|--|---------------------|------|----------------------|------|
| | | | MIN. | TYP. | MAX. | |
| Power Supply Current | I _{CC} | All I _{out} = 0A, CLK = 33 MHz, in LPC mode operation. | - | 12.5 | 20 | mA |
| CMOS Standby Current | I _{sb1} | #LFRAM = 0.9 V _{DD} , CLK = 33 MHz, all inputs = 0.9 V _{DD} / 0.1 V _{DD} | - | 5 | 25 | μA |
| TTL Standby Current | I _{sb2} | #LFRAM = 0.1 V _{DD} , CLK = 33 MHz, all inputs = 0.9 V _{DD} / 0.1 V _{DD} | - | 3 | 10 | mA |
| Input Low Voltage | V _{IL} | - | -0.5 | - | 0.3 V _{DD} | V |
| Input Low Voltage of #INIT Pin | V _{ILI} | - | -0.5 | - | 0.2 V _{DD} | V |
| Input High Voltage | V _{IH} | - | 0.5 V _{DD} | - | V _{DD} +0.5 | V |
| Input High Voltage of #INIT Pin | V _{IHI} | - | 1.35V | - | V _{DD} +0.5 | V |
| Output Low Voltage | V _{OL1} | I _{OL} = 1.5 mA | - | - | 0.1 V _{DD} | V |
| Output High Voltage | V _{OH1} | I _{OH} = -0.5 mA | 0.9 V _{DD} | - | V _{DD} | V |

Power-up Timing

| PARAMETER | SYMBOL | TYPICAL | UNIT |
|-----------------------------|-------------------------|---------|------|
| Power-up to Read Operation | T _{PU} . READ | 100 | μS |
| Power-up to Write Operation | T _{PU} . WRITE | 5 | mS |

Capacitance

(V_{DD} = 3.3V, T_A = 25° C, f = 1 MHz)

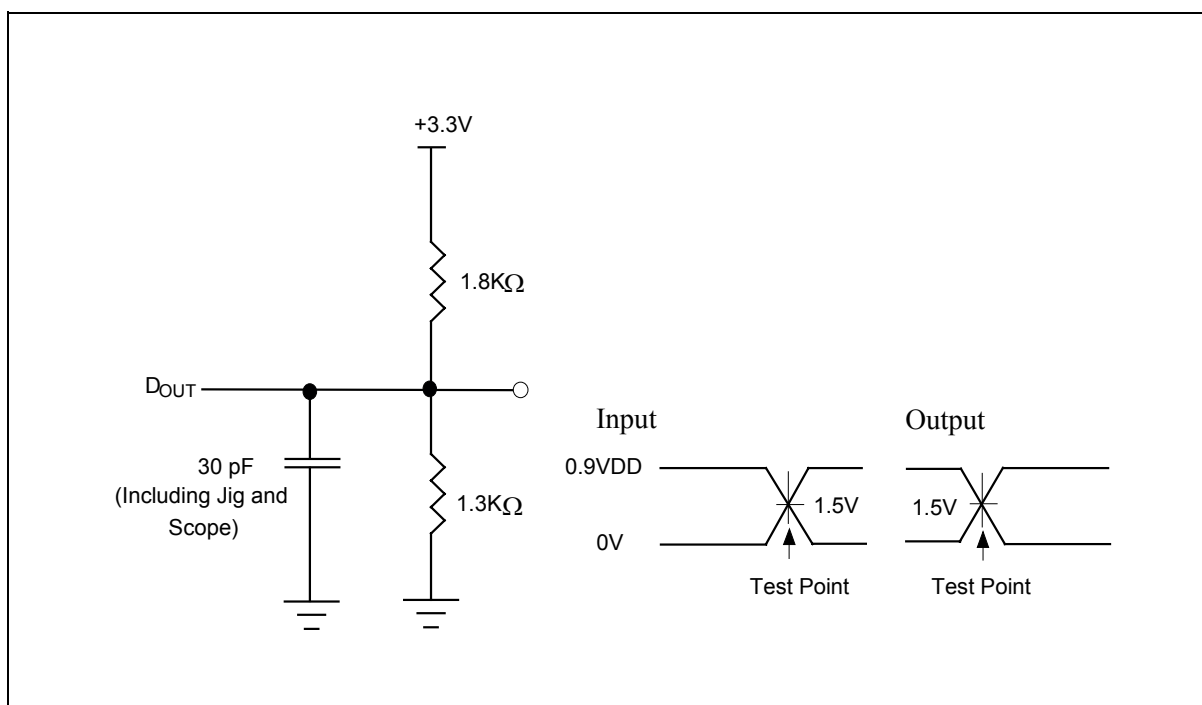
| PARAMETER | SYMBOL | CONDITIONS | MAX. | UNIT |
|---------------------|------------------|-----------------------|------|------|
| I/O Pin Capacitance | C _{I/O} | V _{I/O} = 0V | 12 | pF |
| Input Capacitance | C _{IN} | V _{IN} = 0V | 6 | pF |

8. PROGRAMMER INTERFACE MODE AC CHARACTERISTICS

AC Test Conditions

| PARAMETER | CONDITIONS |
|---------------------------|---------------------------------------|
| Input Pulse Levels | 0V to 0.9 V _{DD} |
| Input Rise/Fall Time | < 5 nS |
| Input/Output Timing Level | 1.5V/1.5V |
| Output Load | 1 TTL Gate and C _L = 30 pF |

AC Test Load and Waveform





AC Characteristics

Read Cycle Timing Parameters

(V_{DD} = 3.3V ±0.3V, V_{SS} = 0V, T_A = 0 to 70° C)

| PARAMETER | SYMBOL | W39V040A | | UNIT |
|---------------------------------|--------|----------|------|------|
| | | MIN. | MAX. | |
| Read Cycle Time | TRC | 300 | - | nS |
| Row/Column Address Set Up Time | TAS | 50 | - | nS |
| Row/Column Address Hold Time | TAH | 50 | - | nS |
| Address Access Time | TAA | - | 175 | nS |
| Output Enable Access Time | TOE | - | 75 | nS |
| #OE Low to Act Output | TOLZ | 0 | - | nS |
| #OE High to High-Z Output | TOHZ | - | 35 | nS |
| Output Hold from Address Change | TOH | 0 | - | nS |

Write Cycle Timing Parameters

| PARAMETER | SYMBOL | MIN. | TYP. | MAX. | UNIT |
|--------------------------------|--------|------|------|------|------|
| Reset Time | TRST | 1 | - | - | μS |
| Address Setup Time | TAS | 50 | - | - | nS |
| Address Hold Time | TAH | 50 | - | - | nS |
| R/#C to Write Enable High Time | TCWH | 50 | - | - | nS |
| #WE Pulse Width | TWP | 100 | - | - | nS |
| #WE High Width | TWPH | 100 | - | - | nS |
| Data Setup Time | TDS | 50 | - | - | nS |
| Data Hold Time | TDH | 50 | - | - | nS |
| #OE Hold Time | TOEH | 0 | - | - | nS |
| Byte Programming Time | TBP | - | 35 | 50 | μS |
| Sector/Page Erase Cycle Time | TPEC | - | 20 | 25 | mS |
| Chip Erase Cycle Time | TEC | - | 75 | 100 | mS |

Note: All AC timing signals observe the following guidelines for determining setup and hold times:

(a) High level signal's reference level is input high and (b) low level signal's reference level is input low.

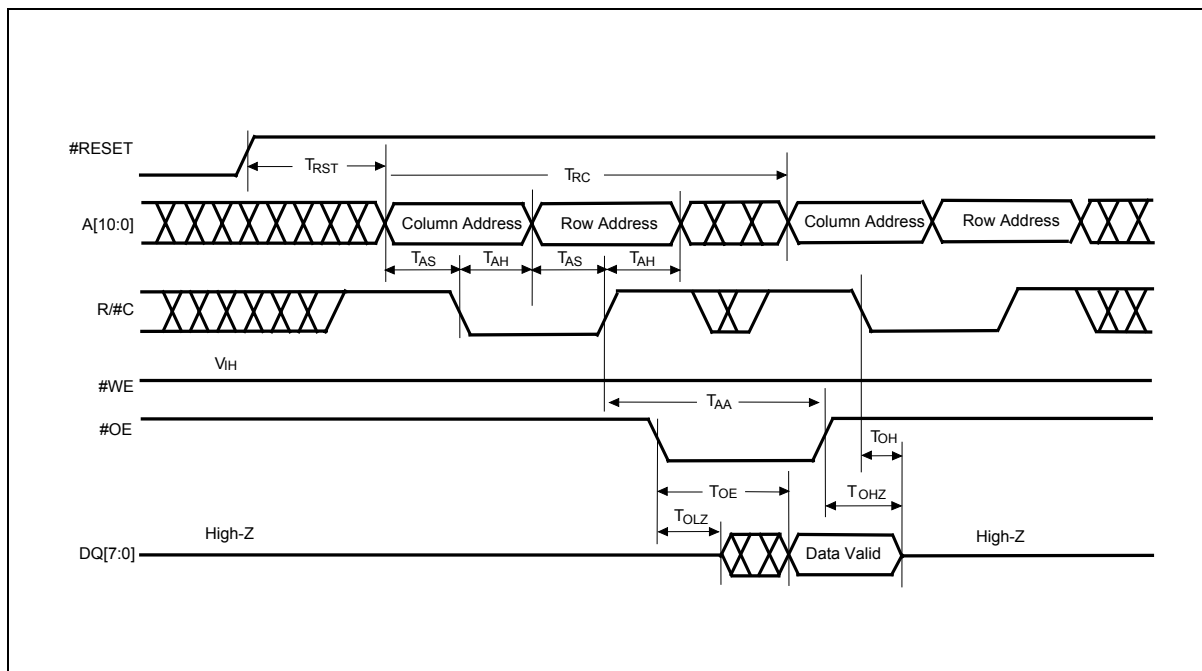
Ref. to the AC testing condition.

Data Polling and Toggle Bit Timing Parameters

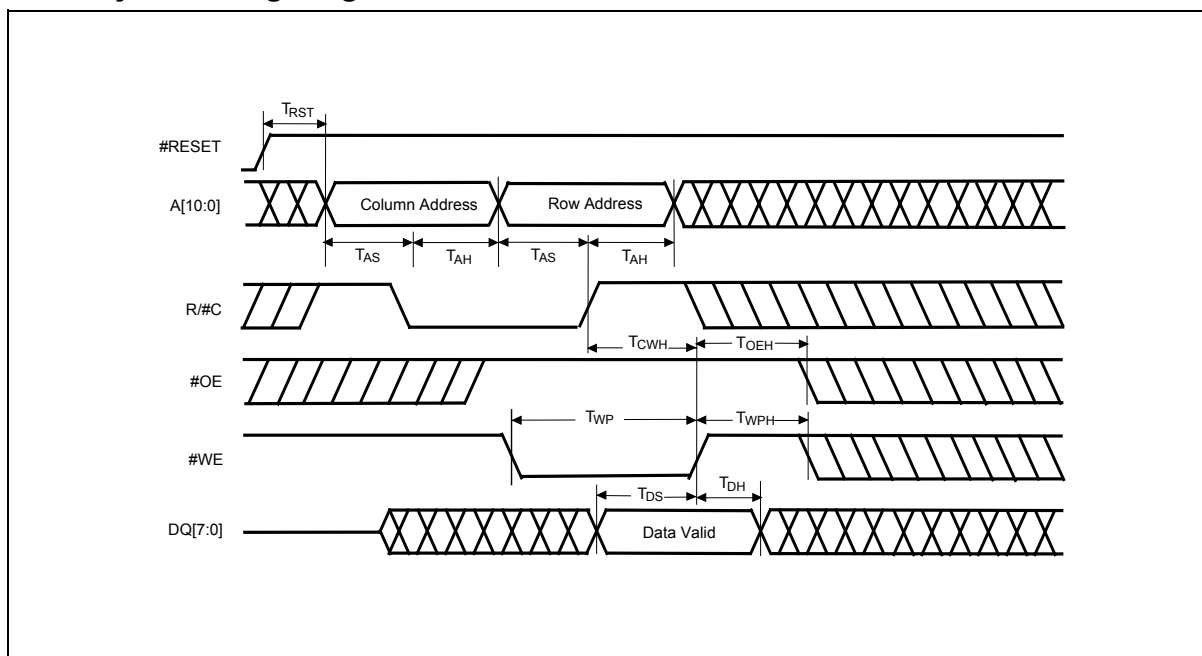
| PARAMETER | SYMBOL | W39V040A | | UNIT |
|----------------------------------|--------|----------|------|------|
| | | MIN. | MAX. | |
| #OE to Data Polling Output Delay | TOEP | - | 40 | nS |
| #OE to Toggle Bit Output Delay | TOET | - | 40 | nS |

9. TIMING WAVEFORMS FOR PROGRAMMER INTERFACE MODE

Read Cycle Timing Diagram



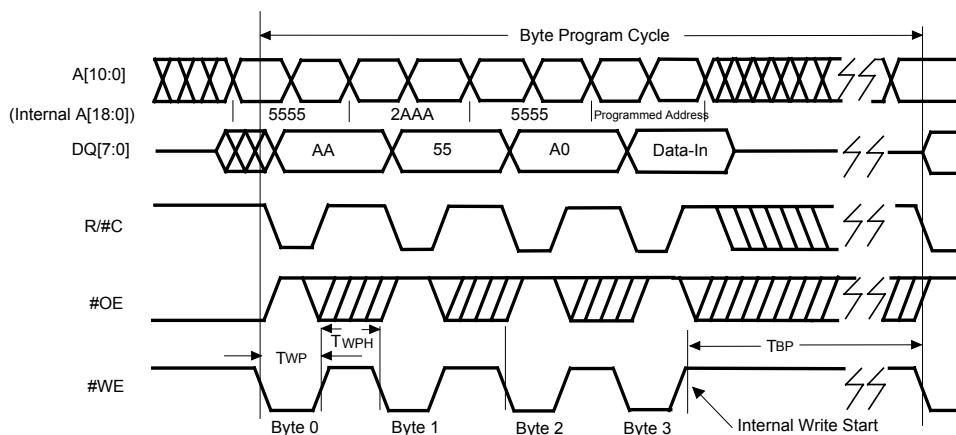
Write Cycle Timing Diagram





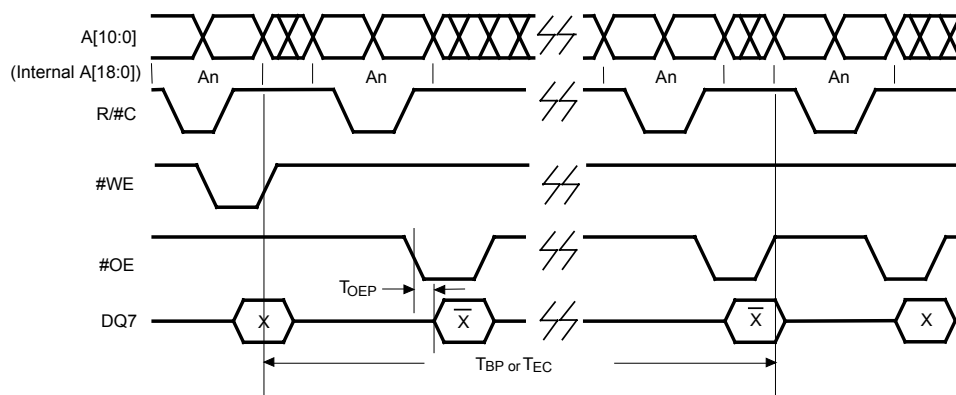
Timing Waveforms for Programmer Interface Mode, continued

Program Cycle Timing Diagram

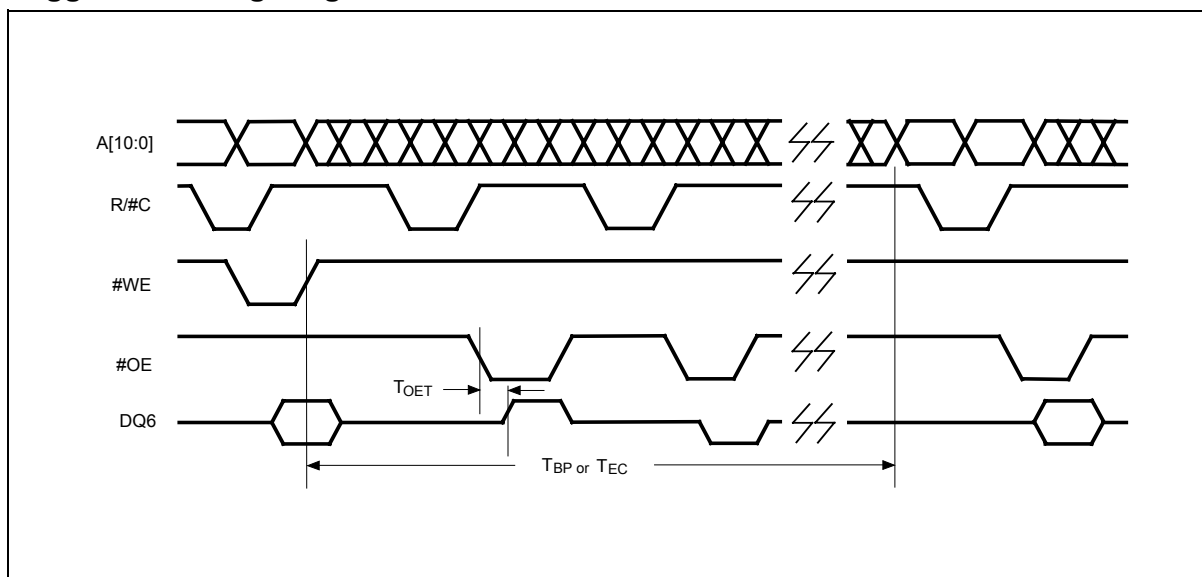
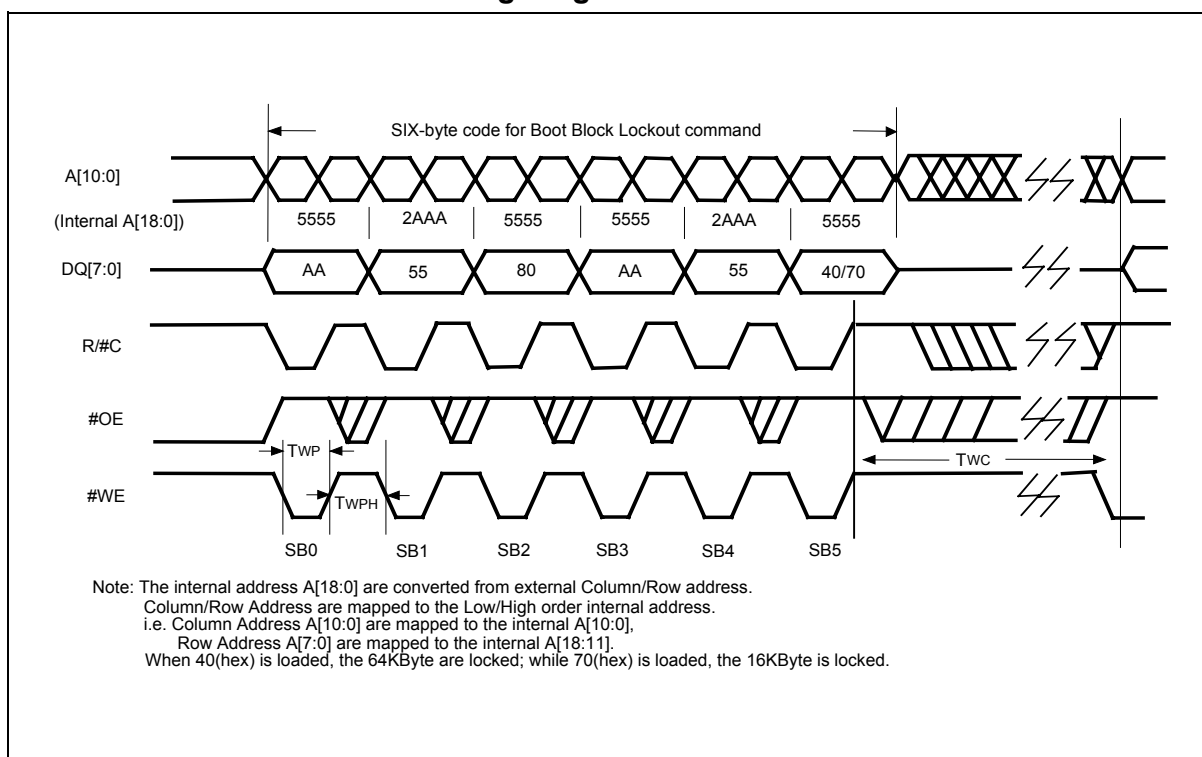


Note: The internal address A[18:0] are converted from external Column/Row address:
 Column/Row Address are mapped to the Low/High order internal address.
 i.e. Column Address A[10:0] are mapped to the internal A[10:0],
 Row Address A[7:0] are mapped to the internal A[18:11].

#DATA Polling Timing Diagram

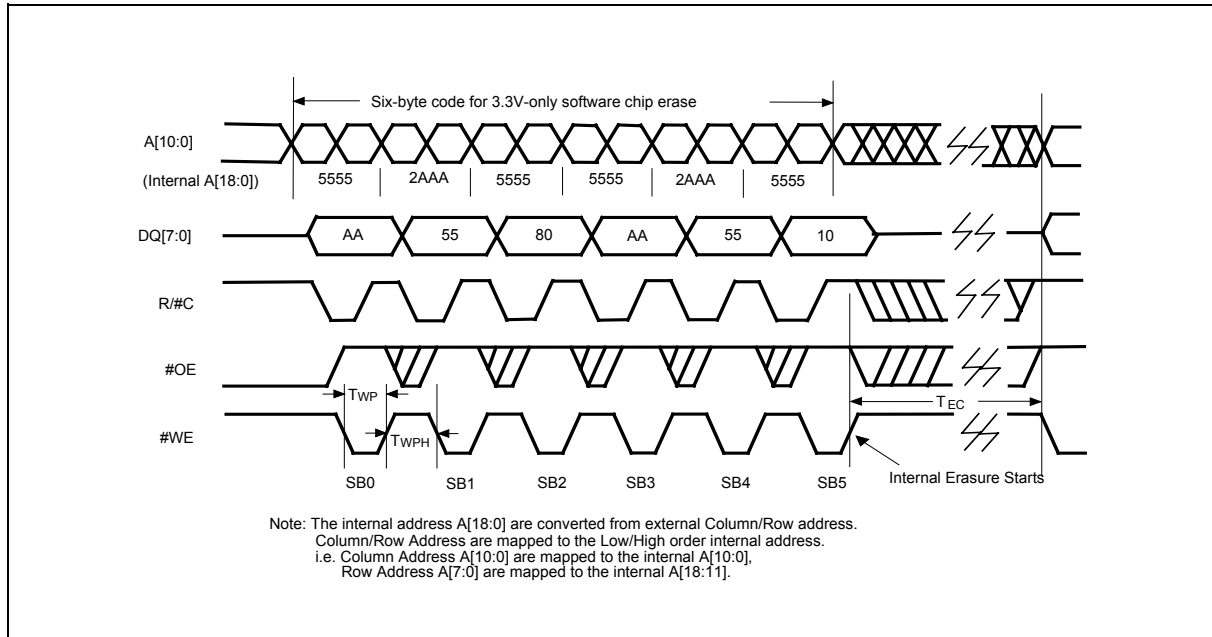


Timing Waveforms for Programmer Interface Mode, continued

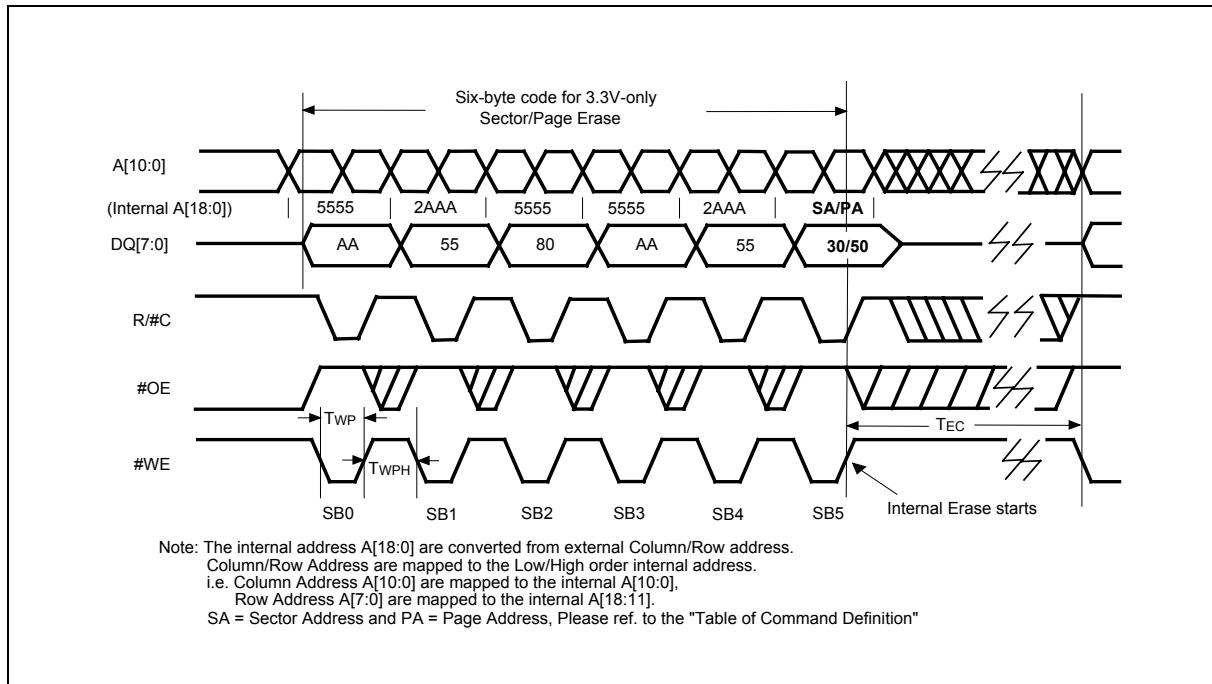
Toggle Bit Timing Diagram**Boot Block Lockout Enable Timing Diagram**

Timing Waveforms for Programmer Interface Mode, continued

Chip Erase Diagram



Sector/Page Erase Timing Diagram





10. LPC INTERFACE MODE AC CHARACTERISTICS

AC Test Conditions

| PARAMETER | CONDITIONS |
|---------------------------|--|
| Input Pulse Levels | 0.6 V _{DD} to 0.2 V _{DD} |
| Input Rise/Fall Slew Rate | 1 V/nS |
| Input/Output Timing Level | 0.4 V _{DD} / 0.4 V _{DD} |
| Output Load | 1 TTL Gate and C _L = 10 pF |

Read/Write Cycle Timing Parameters

(V_{DD} = 3.3V ±0.3V, V_{SS} = 0V, T_A = 0 to 70° C)

| PARAMETER | SYMBOL | W39V040A | | UNIT |
|---------------------|--------|----------|------|------|
| | | MIN. | MAX. | |
| Clock Cycle Time | TCYC | 30 | - | nS |
| Input Set Up Time | TSU | 7 | - | nS |
| Input Hold Time | THD | 0 | - | nS |
| Clock to Data Valid | TKQ | 2 | 11 | nS |

Note: Minimum and Maximum time has different loads. Please refer to PCI specification.

Reset Timing Parameters

| PARAMETER | SYMBOL | MIN. | TYP. | MAX. | UNIT |
|--|--------|------|------|------|------|
| V _{DD} Stable to Reset Active | TPRST | 1 | - | - | mS |
| Clock Stable to Reset Active | TKRST | 100 | - | - | μS |
| Reset Pulse Width | TRSTP | 100 | - | - | nS |
| Reset Active to Output Float | TRSTF | - | - | 50 | nS |
| Reset Inactive to Input Active | TRST | 1 | - | - | μS |

Note: All AC timing signals observe the following guidelines for determining setup and hold times:

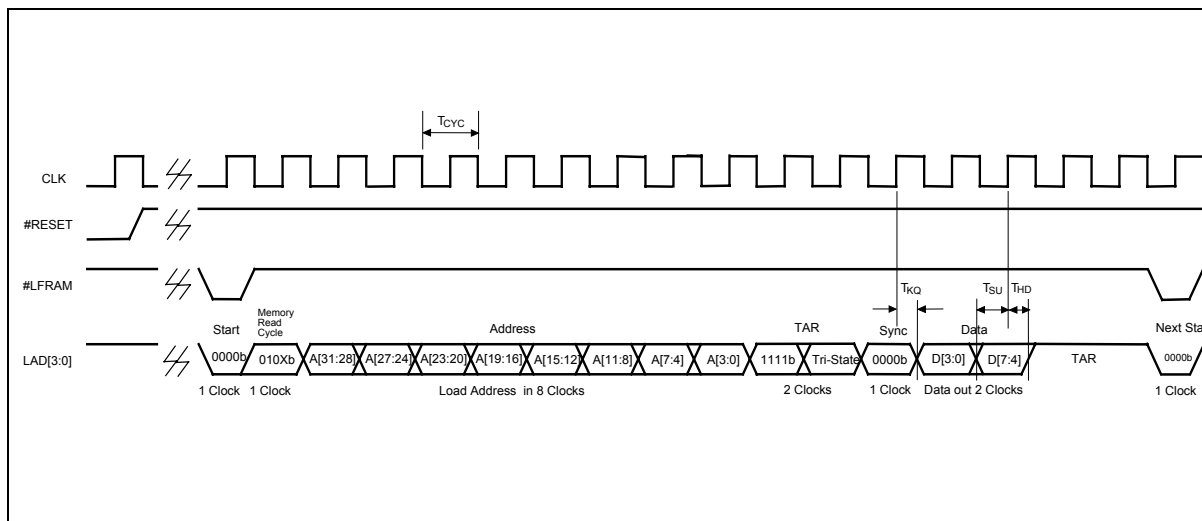
(a) High level signal's reference level is input high and (b) low level signal's reference level is input low.

Ref. to the AC testing condition.

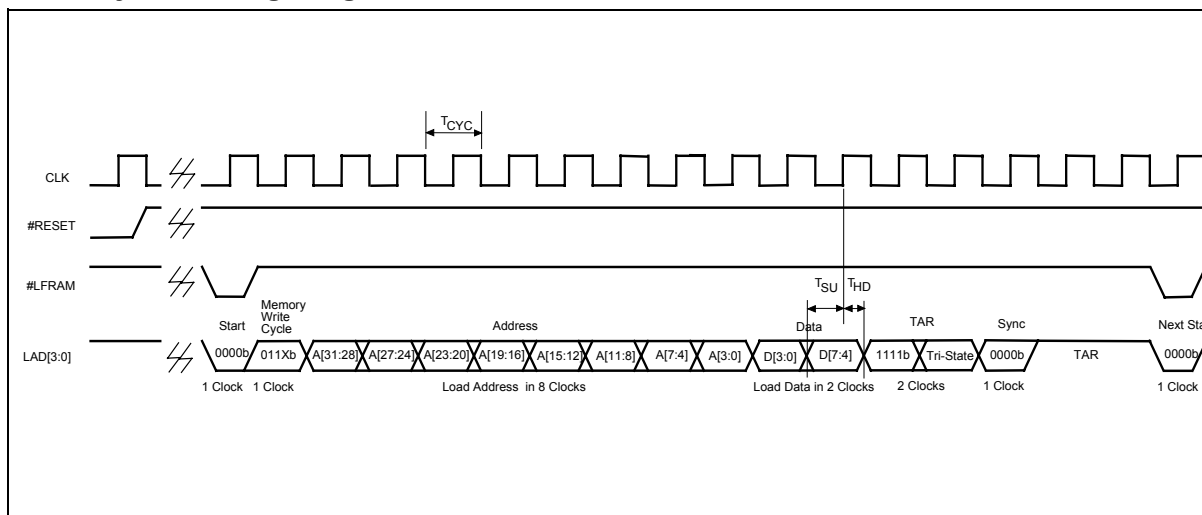


11. TIMING WAVEFORMS FOR LPC INTERFACE MODE

Read Cycle Timing Diagram

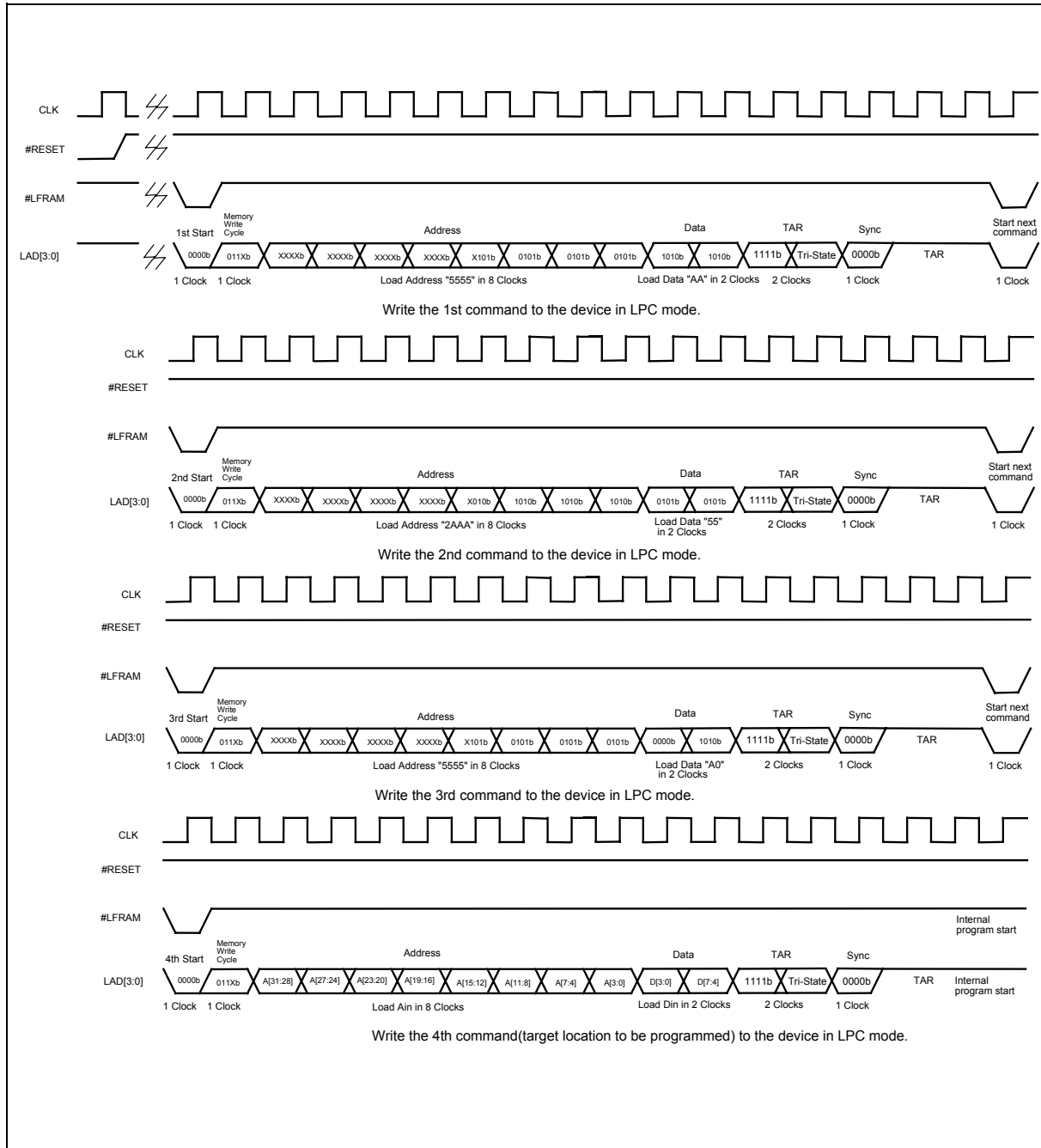


Write Cycle Timing Diagram



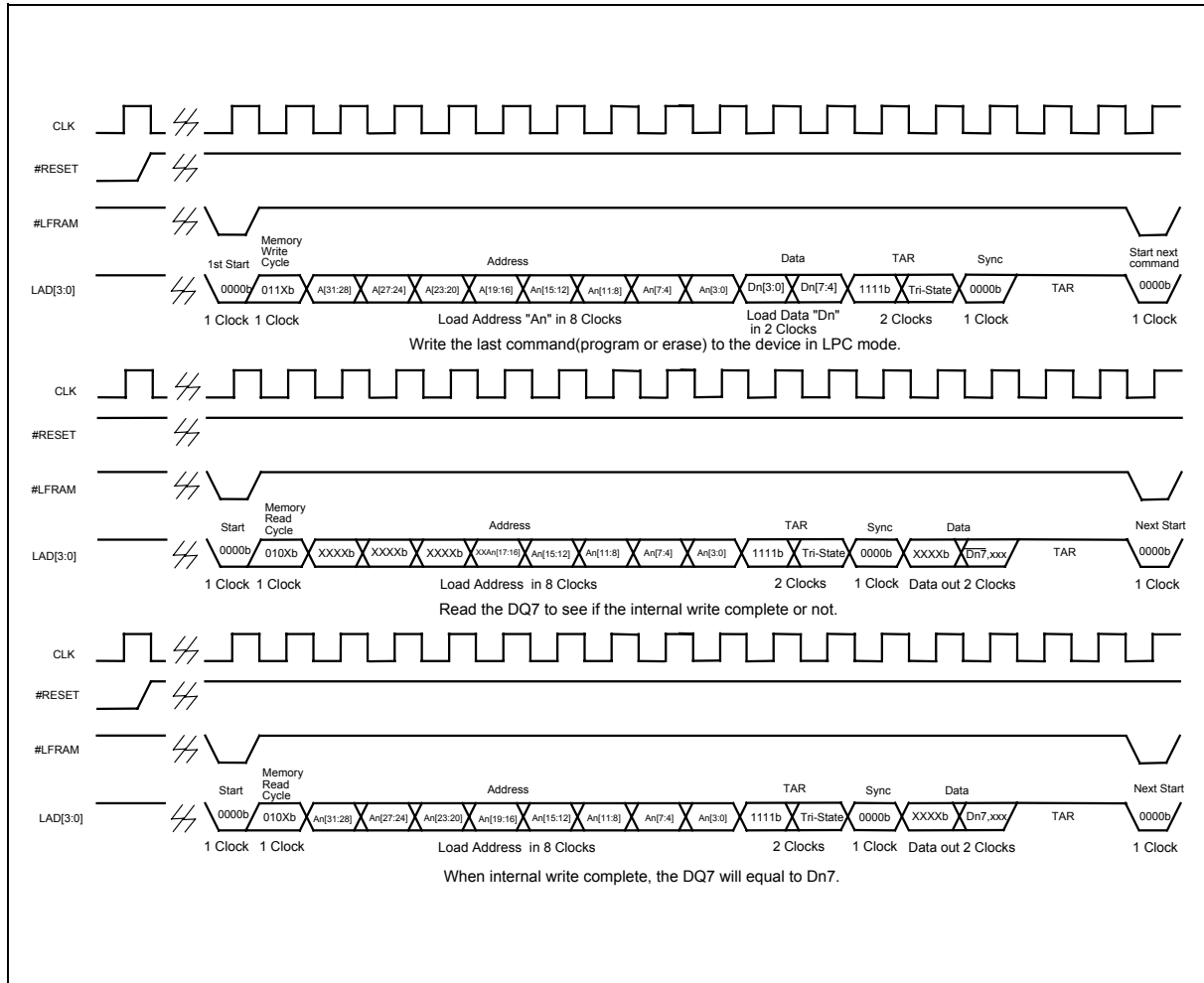
Timing Waveforms for LPC Interface Mode, continued

Program Cycle Timing Diagram



Timing Waveforms for LPC Interface Mode, continued

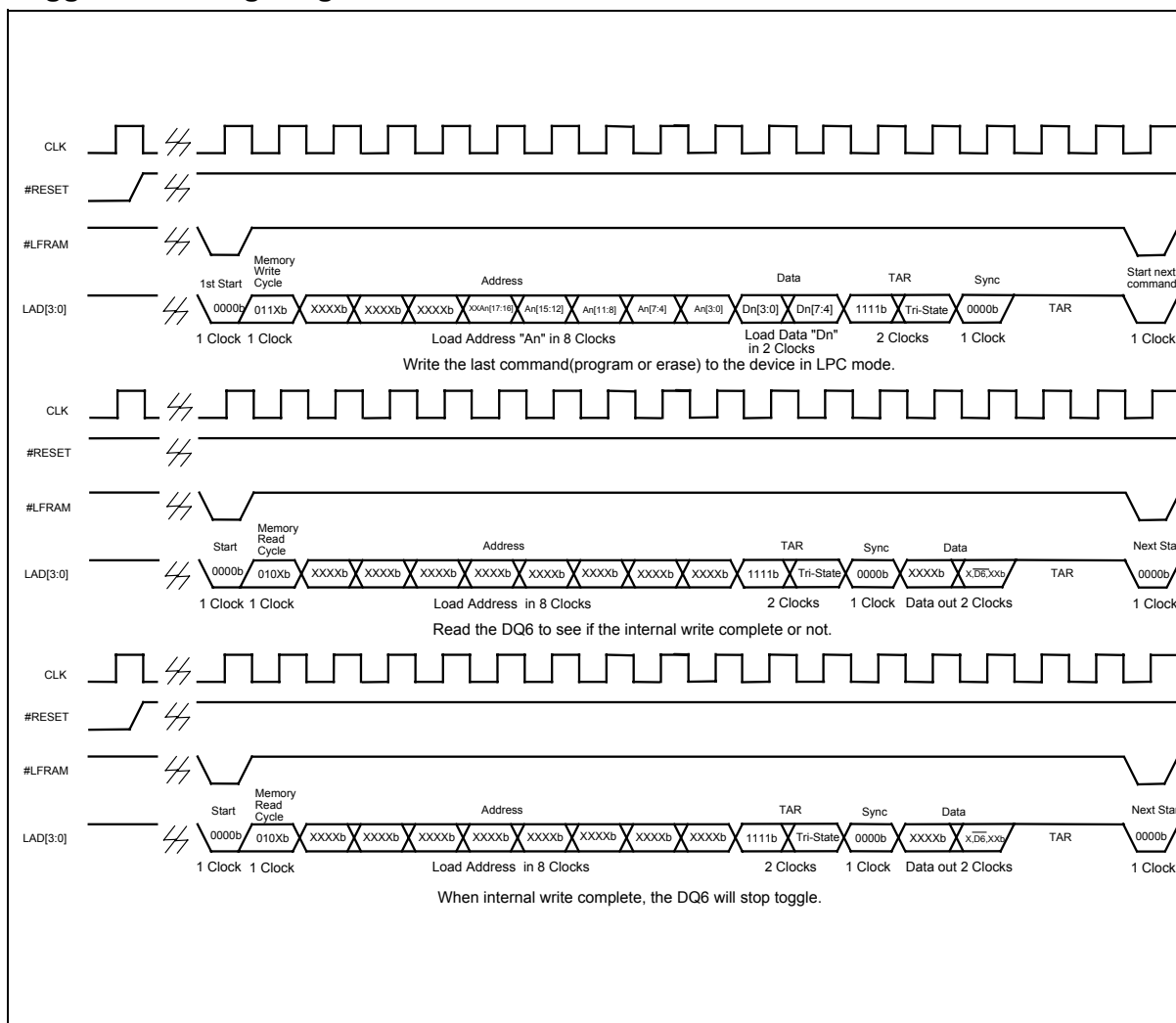
#DATA Polling Timing Diagram





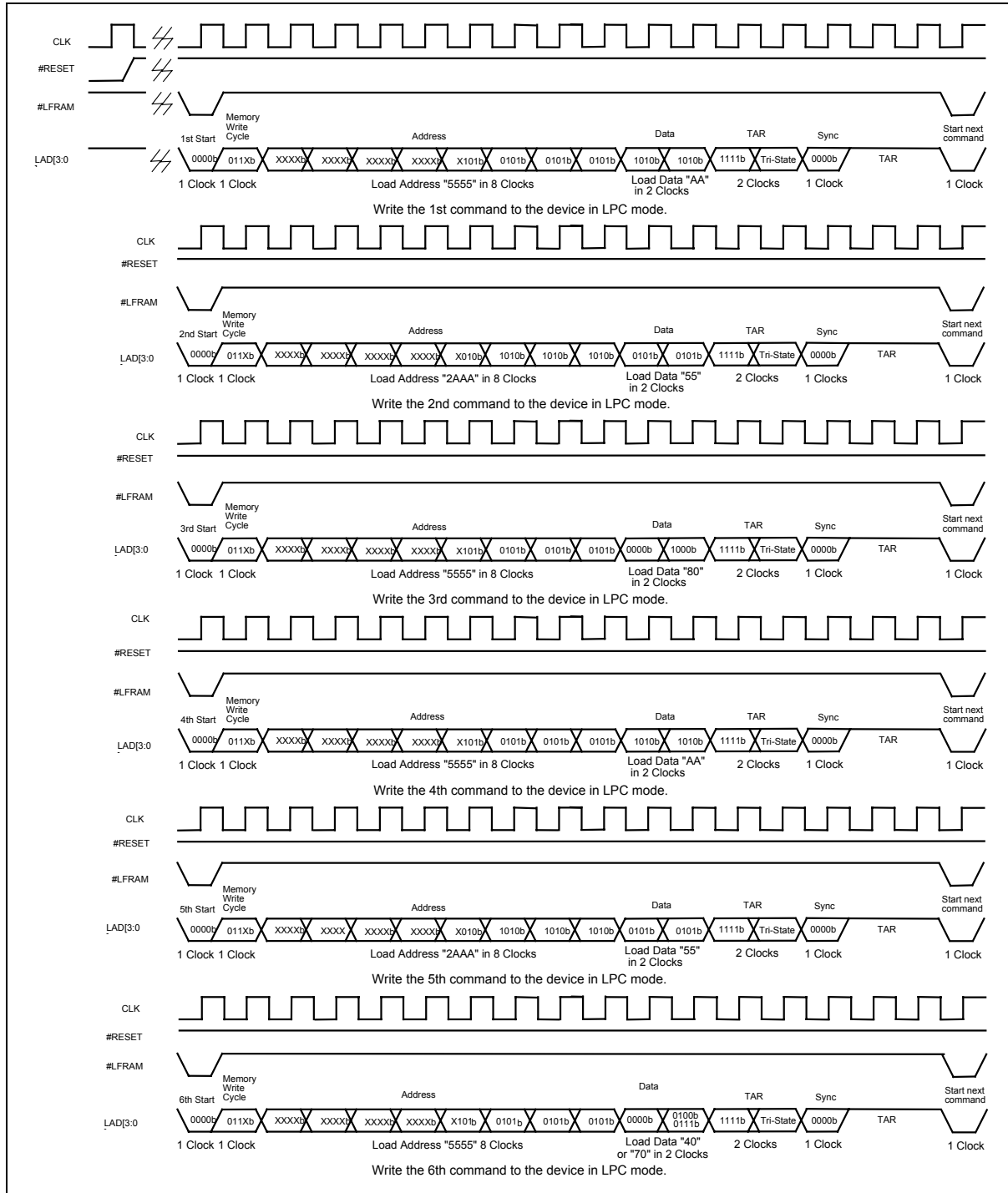
Timing Waveforms for LPC Interface Mode, continued

Toggle Bit Timing Diagram



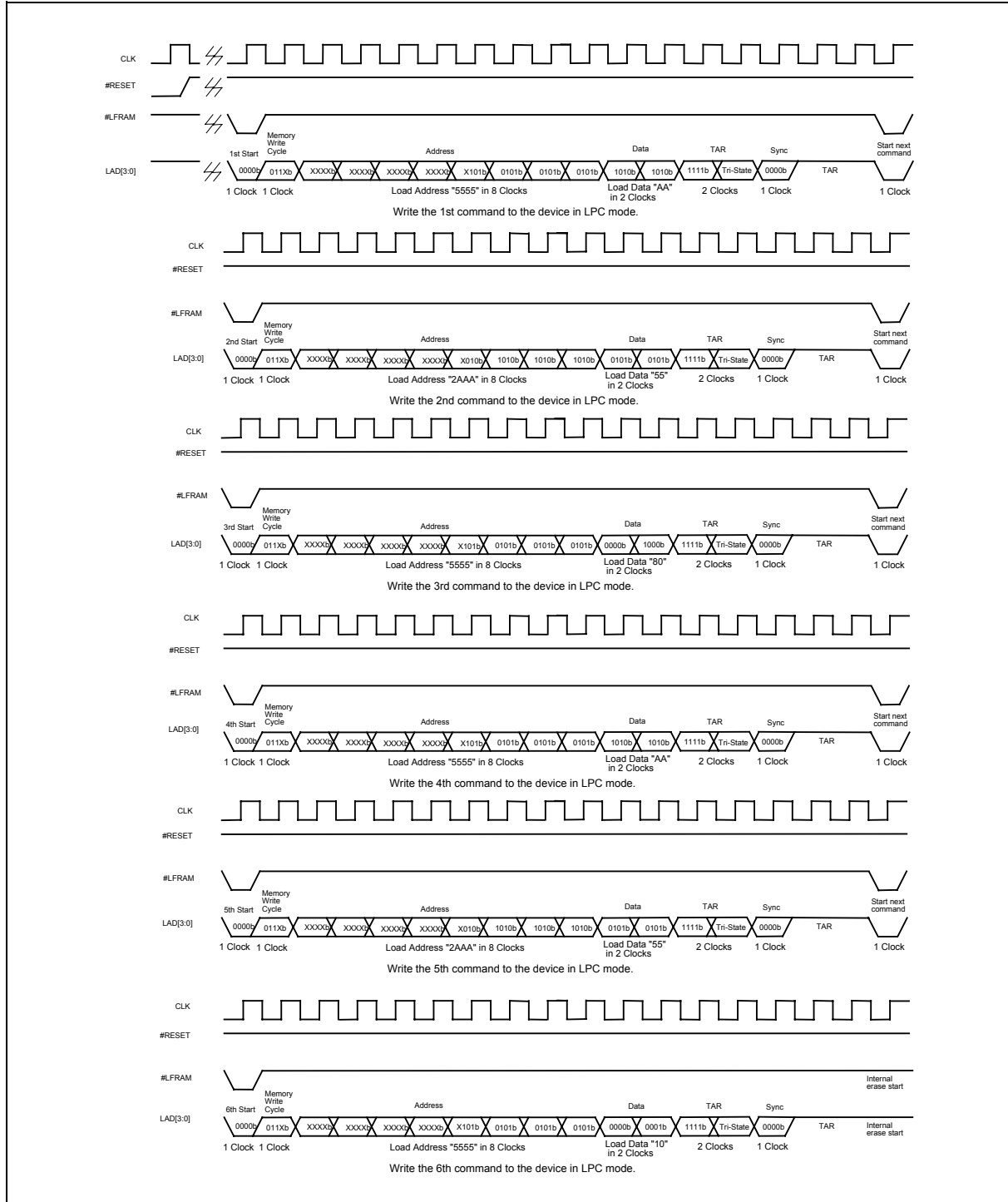
Timing Waveforms for LPC Interface Mode, continued

Boot Block Lockout Enable Timing Diagram



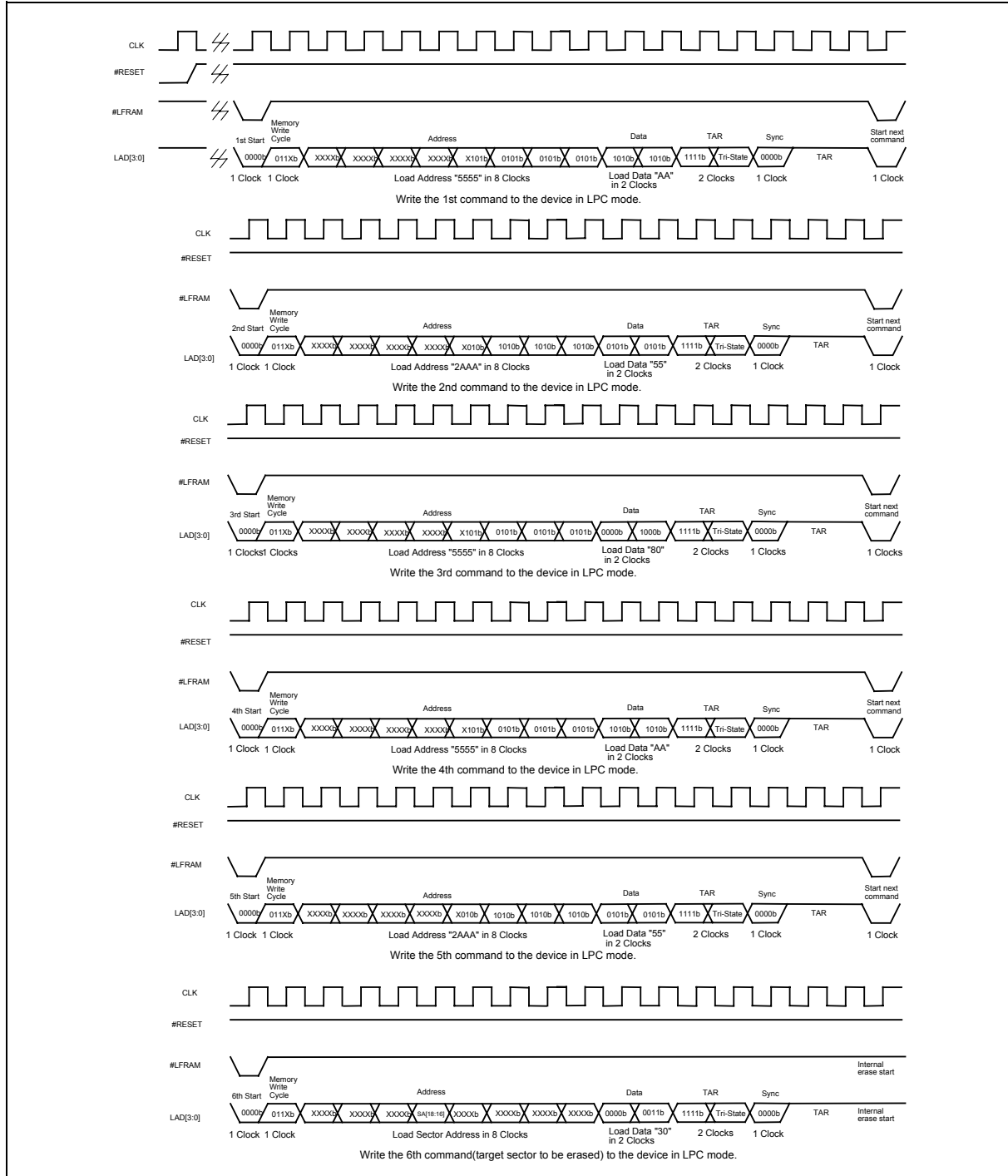
Timing Waveforms for LPC Interface Mode, continued

Chip Erase Timing Diagram



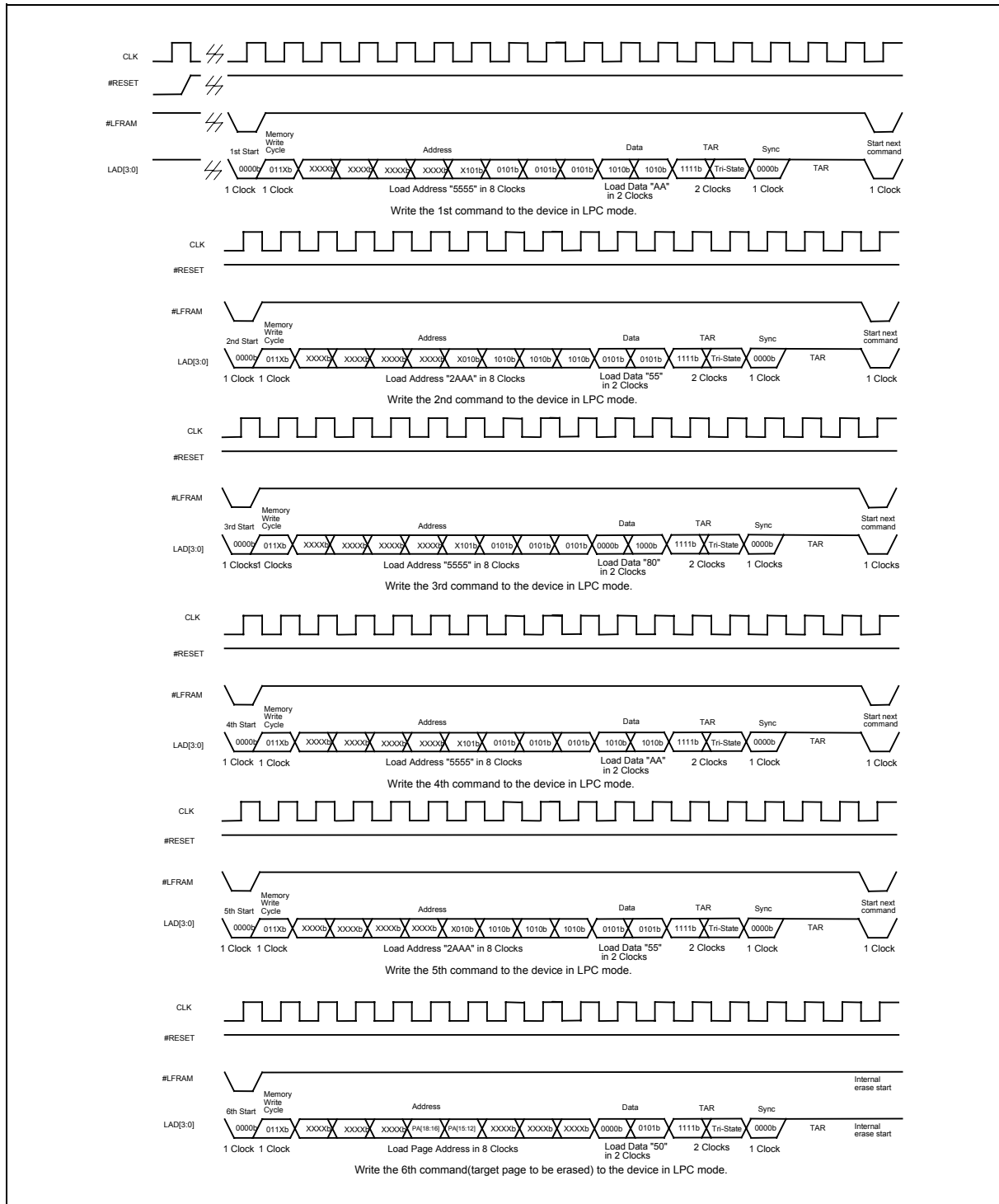
Timing Waveforms for LPC Interface Mode, continued

Sector Erase Timing Diagram



Timing Waveforms for LPC Interface Mode, continued

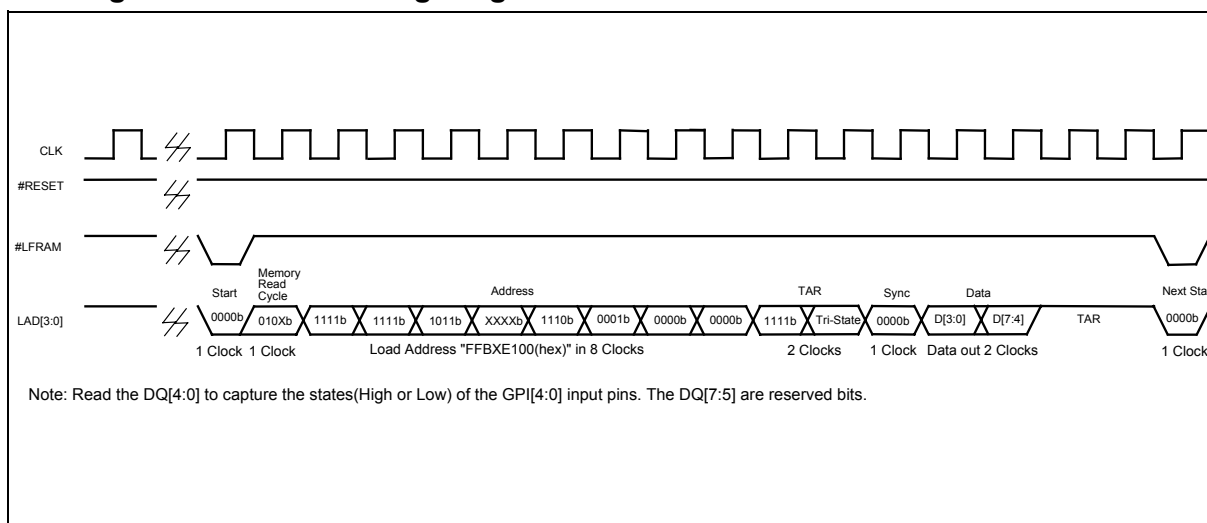
Page Erase Timing Diagram



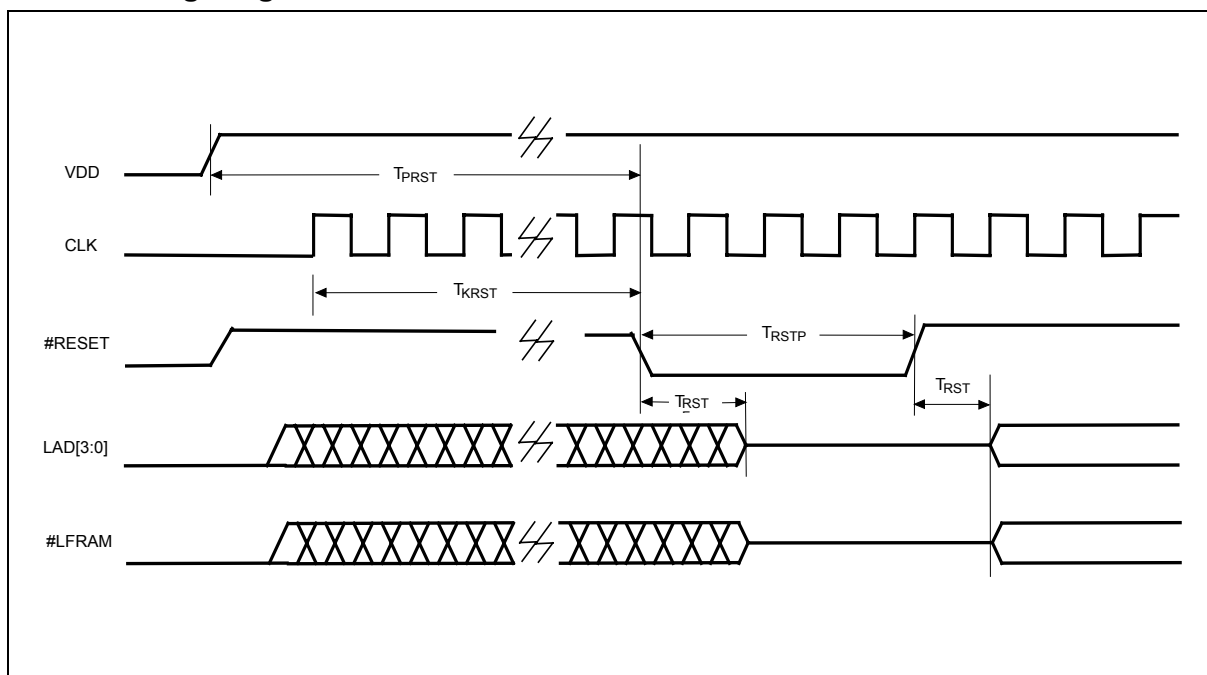


Timing Waveforms for LPC Interface Mode, continued

GPI Register Readout Timing Diagram



Reset Timing Diagram





12. ORDERING INFORMATION

| PART NO. | ACCESS TIME (nS) | POWER SUPPLY CURRENT MAX. (mA) | STANDBY V _{DD} CURRENT MAX. (mA) | PACKAGE |
|-----------|---------------------|-----------------------------------|--|-----------|
| W39V040AP | 11 | 20 | 10 | 32L PLCC |
| W39V040AQ | 11 | 20 | 10 | 32L STSOP |

Notes:

1. Winbond reserves the right to make changes to its products without prior notice.
2. Purchasers are responsible for performing appropriate quality assurance testing on products intended for use in applications where personal injury might occur as a consequence of product failure.

13. HOW TO READ THE TOP MARKING

Example: The top marking of 32-pin STSOP W39V040AQ



1st line: Winbond logo

2nd line: the part number: W39V040AQ

3rd line: the lot number

4th line: the tracking code: 149 O B SA

149: Packages made in '01, week 49

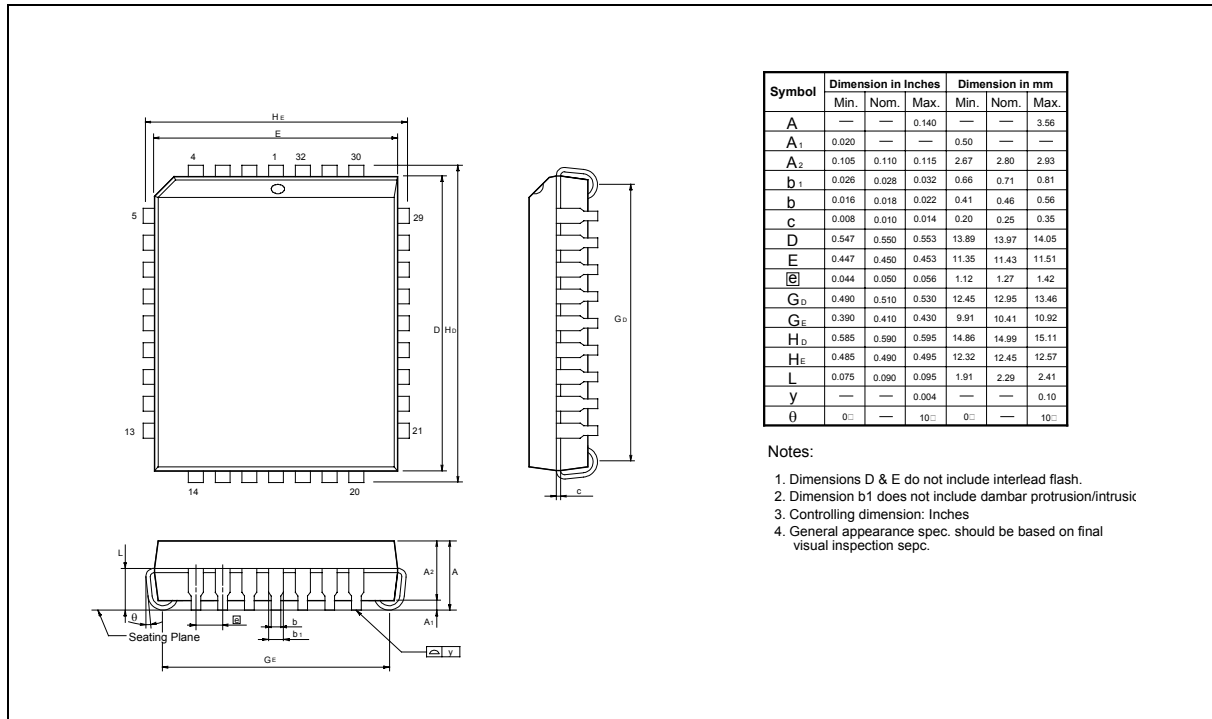
O: Assembly house ID: A means ASE, O means OSE, ... etc.

B: IC revision; A means version A, B means version B, ... etc.

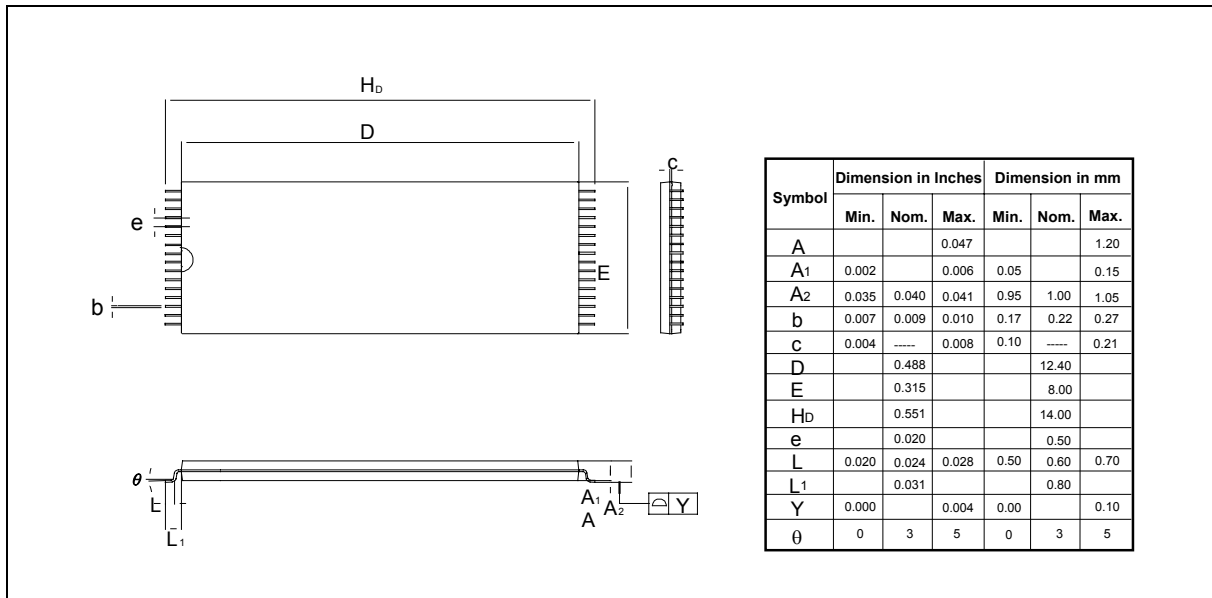
SA: Process code

14. PACKAGE DIMENSIONS

32L PLCC



32L STSOP





15. VERSION HISTORY

| VERSION | DATE | PAGE | DESCRIPTION |
|---------|-----------------|-----------|--|
| A1 | October 8, 2002 | - | Initial Issued |
| A2 | Dec. 19, 2002 | 14 | Modify PGM mode power supply current (Icc) parameter from 20 mA (typ.) to 10 mA (typ.) and 30 mA (max.) to 20 mA (max.) |
| | | 1, 15, 32 | Modify LPC mode power supply current (Icc) parameter from 40 mA (typ.) to 12.5 mA (typ.) and 60 mA (max.) to 20 mA (max.) |
| | | 15 | Modify CMOS standby current (I _{sb1}) parameter from 20 μ A (typ.) to 5 μ A (typ.) and 100 μ A (max.) to 25 μ A (max.) |



Headquarters

No. 4, Creation Rd. III,
Science-Based Industrial Park,
Hsinchu, Taiwan
TEL: 886-3-5770066
FAX: 886-3-5665577
<http://www.winbond.com.tw/>

Taipei Office

9F, No.480, Rueiguang Rd.,
Neihu District, Taipei, 114,
Taiwan, R.O.C.
TEL: 886-2-8177-7168
FAX: 886-2-8751-3579

Winbond Electronics Corporation America

2727 North First Street, San Jose,
CA 95134, U.S.A.
TEL: 1-408-9436666
FAX: 1-408-5441798

Winbond Electronics Corporation Japan

7F Daini-ueno BLDG, 3-7-18
Shinyokohama Kohoku-ku,
Yokohama, 222-0033
TEL: 81-45-4781881
FAX: 81-45-4781800

Winbond Electronics (Shanghai) Ltd.

27F, 2299 Yan An W. Rd. Shanghai,
200336 China
TEL: 86-21-62365999
FAX: 86-21-62365998

Winbond Electronics (H.K.) Ltd.

Unit 9-15, 22F, Millennium City,
No. 378 Kwun Tong Rd.,
Kowloon, Hong Kong
TEL: 852-27513100
FAX: 852-27552064

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